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Design and Implementation of FIR filter using Carry Select Adder

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Abstract: ***Carry Select Adder (CSLA) is a basic building blocks used in data processing processor to carry out fast arithmetic functions. As a scale of integration keeps growing, signal processing systems is being implemented on a VLSI chip to a greater extent which demand not only high computation capacity but also consume large amount of energy. While performance and area remain to be the two major design parameters, power consumption is become a critical task in today's VLSI system design. To reduce the power consumption of data processing processor we need to reduce number of transistors of the adder. So, there is a chance to reduce the power and delay in the CSLA structure. The proposed design uses D-latch instead of using RCA cascade structure for cin=1or cin=0. This CSLA is implemented in the adder of FIR filter. The proposed design achieves the two folded advantages in terms of delay and power.***

Keywords: CSLA, RCA, D-Latch, low power, high speed

1. Introduction

Adders are widely used in electronics applications, such as multipliers, DSP to design various algorithms like DFT, FFT, FIR and IIR. Advancement in mobile computing and multimedia applications insists for highly efficient VLSI Digital Signal Processing (DSP) systems. As nanometer process technology has advanced, chip density and operating frequency has increased, resulting in power consumption in battery-operated devices. For non portable devices, power consumption is important because of cooling costs and increased packaging. Thus, the main design aim for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increasingly important.

In well known adder architecture, ripple carry adder is composed by cascading full adder blocks in series. The carry out of one stage is fed directly to the carry in of next stage. For an n-bit parallel adder it requires n full adders. It is not very efficient when large numbers of bit are used. Delay increases linearly with bit length. Latch is an electronic device that can be used to store one bit of information. The D latch is used to latch the logic level which is present on data line when clock input is high. If the input on data line changes state while clock pulse is high, then the output, Q, follows input, D. When clock input falls to logic 0, the last state of D input is trapped and held in the latch.

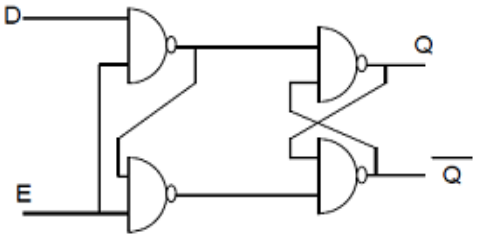

Figure 1: D-Latch.

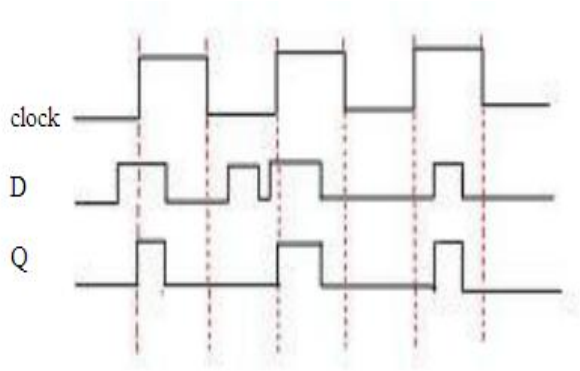

Figure 2:Timing diagram of D-Latch.

Finite impulse response (FIR) filtering is one of the most widely used operations in DSP. The several proposed technique achieves high performance with reduced area & power. Finite Impulse Response (FIR) filter has been designed by considering the power consumption in adder unit. So, we design a adder with less delay and consumes less power.

The Paper is organized as follows- Section 2 explains an regular carry select adder. Section 3 gives an introduction to the proposed a carry select adder using D-Latch. Section 4 deals with an implementation of FIR filter. Section 5 discusses about the comparisons between the adders in term of delay and power. The conclusion is given in the further section.

2. Regular Carry Select Adder using RCA

Parallel computation is the basic operation of CSLA. Many carriers and partial sums are generated by CSLA. The CSLA comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming carry input as 1 and 0 prior the carry inputs comes. When actual carry input arrives, the actual

calculated values of sum and carry are selected using a multiplexer. The carry out calculated from the last stage is used to select the actual calculated values of output carry and sum. The selection is done by using a multiplexer. The structure of 16-bit CSLA is shown below:

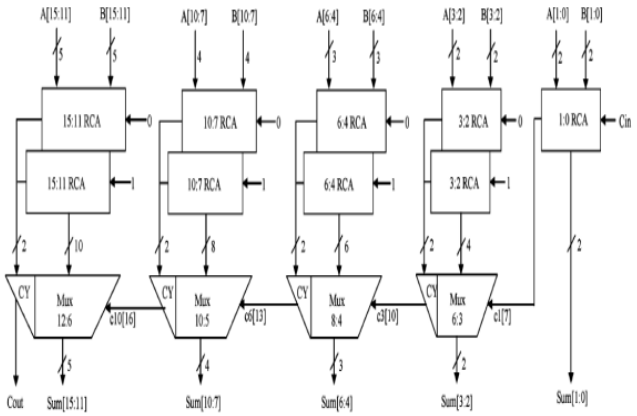

Figure 3: 16-bit regular Carry Select Adder.

The CSLA structure consists of pair of Ripple Carry Adders (RCA). Initially Cin=0 is used in one RCA and Cin=1 is used in another RCA. Using multiple pairs of RCA complexity of the circuit gets increased. The main disadvantage of RCA is its propagation delay. Therefore it is necessary to reduce power & delays of existing CSLA structure.

3. Modified carry select adder using D-Latch

This method replaces RCA with cin=1or cin=0 by D-latch with enable signal, where enable signal is clock signal. Latches are used to store one bit information. Their outputs are constantly affected according to their inputs as long as enable signal is asserted. The architecture of proposed 16-b CSLA is shown in Figure 4.

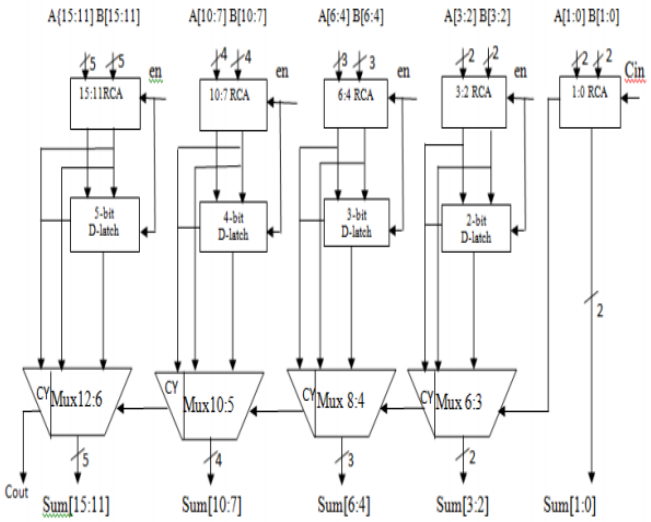

Figure 4: 16-bit modified Carry Select Adder

It has five groups of different bit size RCA and D-Latch. Instead of using two separate adders as used in regular CSLA, here only one adder is used to reduce power consumption and delay. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which LSB (least significant bit) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e, MSB (most significant bit) is 14- bit wide which work according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself.

Initially when en=1, the output of the RCA is fed as input to the D-Latch and the output of the D-latch follows the input and given as an input to the multiplexer. When en=0, the last state of D input is trapped and held in the Latch and therefore the output from the RCA is directly given as an input to the mux without any delay. Now the mux selects the sum bit according to the input carry which is the selection bit and the inputs of the mux are the outputs obtained when en=1 and en=0.

4. Implementation of FIR filter using CSLA

Finite impulse response (FIR) filtering is one of the mostly used operations in DSP. The main building block in FIR filter is Multiplier-Accumulator (MAC) unit. In MAC unit full adder mainly affect the efficiency of system. Therefore, power reduction in adder circuit is necessary for low power application. So there is need to design high speed adders. The FIR Filter is implemented using these both CSLA and then comparing both results in terms of delay and power.

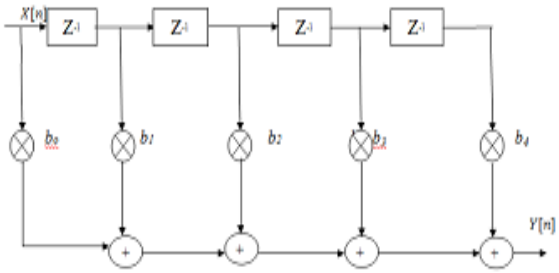

Figure 5: FIR Filter.

The adder part of FIR Filter is replaced with the regular and modified CSLA. Here we use a 4-tap FIR Filter implementation using regular and modified CSLA [7].

5. Simulation and Synthesis results

The design proposed in this paper has been developed using VHDL and synthesized using Xilinx PlanAhead 14.2. This design was implemented in Spartan3E kit. The simulation and synthesis of the adder is performed and results are summarized. The similar design flow is followed for both the regular and modified CSLA.

Figure 6: Simulation output of 16-bit Regular CSLA.

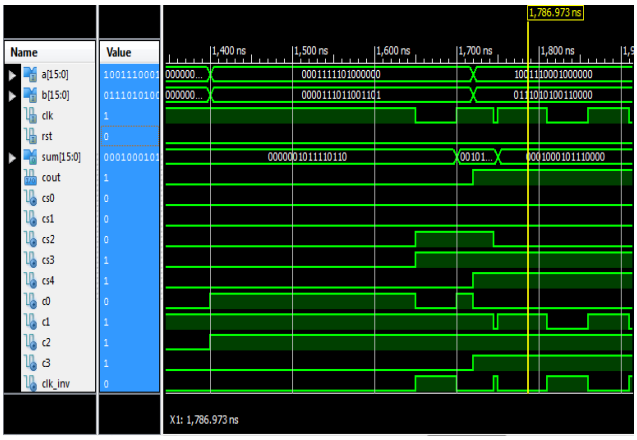

Figure 7: Simulation output of 16-bit Modified CSLA.

After the observation of simulation waveforms, synthesis is performed for the calculation of delay and thereby the power of the CSLA's are calculated. Table 1 exhibits the simulation results of both CSLA structures in terms of delay and power.

Table 1: Comparison of Regular and Modified CSLA

Parameters	*Regular CSLA*	*Modified CSLA*
Delay (ns)	19.853	10.464
Power(mW)	185	143

From the above table, we can say that delay and power of an Modified CSLA is reduced by 9.389 ns and 42 mW respectively as compared to Regular CSLA. Thus, a CSLA with D-latch is a High Speed Carry Select Adder.

We now analysis the performance of the CSLA by implementing an FIR filter using Regular Carry Select Adder and Modified Carry Select Adder in the adder part of filter and then both results of filter are compared in term of delay and power.

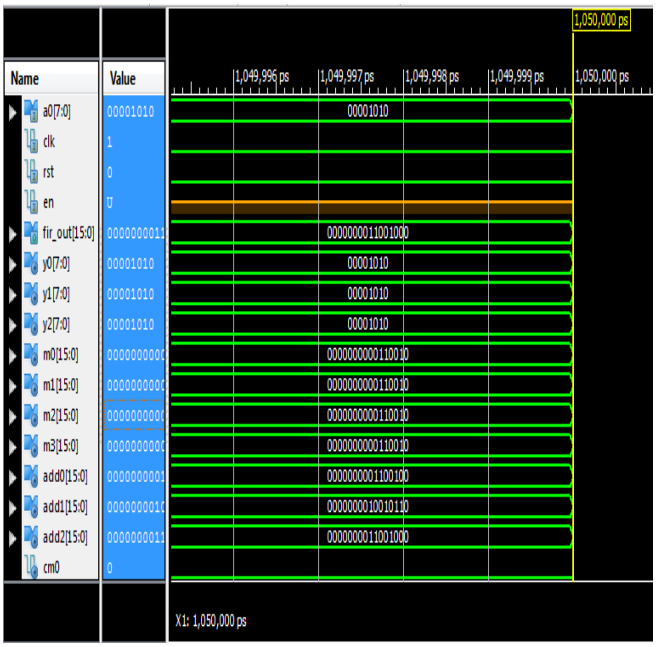

Figure 8: Simulation output of FIR Filter using Regular CSLA

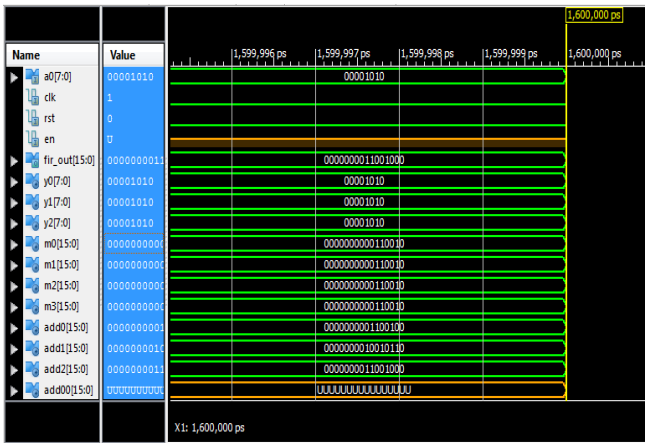

Figure 9: Simulation output of FIR Filter using Modified CSLA

Table 2: Comparison of Regular and Modified CSLA implemented in FIR filter

Parameters	*FIR filter using Regular CSLA*	*FIR filter using Modified CSLA*
Delay(ns)	22.539	13.778
Power(mW)	114	110s

From the above table, we can see that delay and power are reduced when the FIR Filter is implemented with an Modified CSLA with D-latch rather than an FIR Filter that is implemented with a Regular CSLA. Thus a high speed and low power FIR filter can be designed using a Modified CSLA with D-latch. Thus a CSLA designed with a D-latch is a High Speed Carry Select Adder.

6. Conclusion

This paper presented a unique approach to reduce the delay and power of CSLA architecture. Here, we show the design of CSLA implemented by using D-Latch and compared with Regular CSLA. The result shows that CSLA with D-Latch is

a high speed and low power carry select adder. All these adders are implemented on Spartan 3E Kit and performance of this CSLA is evaluated in terms of delay and power by using CSLA in the adder part of FIR filter and it proves to be high speed and low power carry select adder .

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