

Wide Range Enable Level Shifter for Multi-Supply Voltage Designs

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Abstract: *In the current SoC design methodologies, the multi supply voltage and power gating techniques are used widely which require special cells in design. A new enable level shifter is designed which comprises the function of level shifter and isolation cell. The voltage level shifting is achieved by the use of modified Wilson current mirror circuits, which gives wide range of input voltage. In the given ELS, the output will be clamped to ground when the enable signal is high i.e. during the power domain shut down. This avoids the false triggering of transistors in the subsequent blocks. The proposed ELS is designed using SPICE model of 32nm technology and simulated. The ELS can reliably convert 100mV input voltage to 0.9V, with the delay of 5ns. The power consumption of the cell is 100nW at 0.9V input voltage.*

Keywords: multi voltage supply design, dynamic voltage scaling, power gating, isolation cells, modified Wilson current mirror, ELS, SPICE.

1. Introduction

The System-on-chip design methodologies are continuously changing as the designs are getting more complex. Now millions of gates can be implemented on relatively smaller die area. This leads to increase in power density and the total power consumption of design. Design engineers have biggest challenge to reduce the power consumption while meeting the desired specifications [1]. Dynamic Voltage Scaling Techniques are extensively used which needs special characterized circuits that can operate on wide range of supply voltages. Ultra-low power consumption of such circuits facilitates the development of new crucial applications [2].

The benefit of voltage scaling is apparent when the main sources of power dissipation on a chip are considered. Power on the chip is consumed both when the circuit is active and also when it is inactive. Dynamic power is associated with switching of nets and cells and can be calculated using the formula.

$$P_{DYN} = \alpha C_L V^2 f$$

That dynamic power varies with the square of the supply voltage explains the obvious interest in voltage reduction in a design wherever possible. But as the supply voltage reduces, the performance of the system degrades, hence the system fails at higher speed, so in order to maintain the performance we need to go for multi-voltage which encapsulates the benefits of both low power and high speed.

For proper functionality of multi-voltage low power designs, special cells are required during implementation. These cells are used for function needs for multi-voltage designs where some areas may optionally be powered down. A signal net which connects an output of a cell in a shutdown area to a cell in an active area requires an isolation cell to prevent crowbar

current and spurious signal propagation [3].

Multi-voltage systems impose many challenges on designers, one of which is the design and insertion of level shifters and isolation cells between components running at different voltage domains. There are low-to-high and high-to-low level shifters. High-to-low level shifter is simply a buffer driven by the high voltage level (VDDH) and has the low voltage level (VDDL) as power supply. In practice, its use is recommended for having accurate timing closure and is not needed for the correct operation [4].

Enable level shifter performs the function of both isolation cell and level shifter cell when voltage scaling technique is implemented and it has voltage areas which can go to power down state.

Due, in part, to the proliferation of multiple voltage domains on a chip, numerous level converters exist for strong inversion operation, but subthreshold conversion differs from the conventional scenario [5].

This paper deals with the design of Enable Level Shifter which can operate at subthreshold regions and perform the function of isolation cell. The ELS is designed with 32nm technology using the PTM model and simulation has been done using the HSPICE tool.

This paper is organized as follows. Section 2 gives the related work to level shifter. Section 3 gives details of Modified Wilson current mirror and proposed ELS. Results and Conclusions are discussed in Section 4 and 5 respectively.

2. Related work

There are a few conventional level shifters circuits, some those are compared in [6]. One of the most commonly used level shifter is shown in Figure 1. In this circuit, there are two cross coupled PMOS transistors M1 and M3, two NMOS transistors. The inverter is connected to supply VDDL and ground and provides the complementary signal of input. The PMOS transistor acts as load to the circuit. When the input is 0V, the M2 will be turned off and the M4 will be turned on. This will cause M1 to turn on and M3 to turn off. The input of output inverter will be grounded and it will give the output voltage of VDDH.

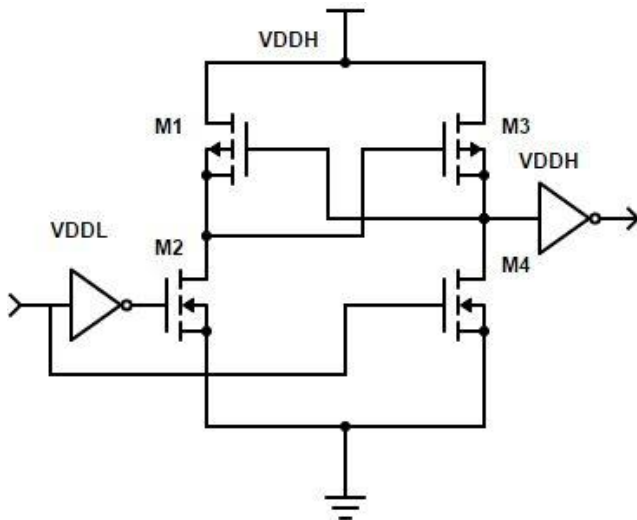


Figure 1: Conventional level shifter.

However, a high amount of quiescent current occurs when the input voltage is suprathreshold. This high power consumption limits the use of the conventional level shifter. Since a level shifter circuit consumes power and has a considerable delay, its optimization for delay performance, low power and low area is important [7].

The ELS presented in [8] is Bypassing Enabled Level Shifter (BELS) implements a bypass function, which is used when supply voltage in designs switches between two voltage values.

3. Modified Wilson Current Mirror Circuit and Proposed ELS

3.1 Modified Wilson current mirror

The modified Wilson current mirror is shown in Figure 2(a). It consists of four transistors, two of which are gate-drain shorted (M2 and M3). As all current mirrors are basically designed to do, reference current flowing in one branch of circuit is mirrored in other branch.

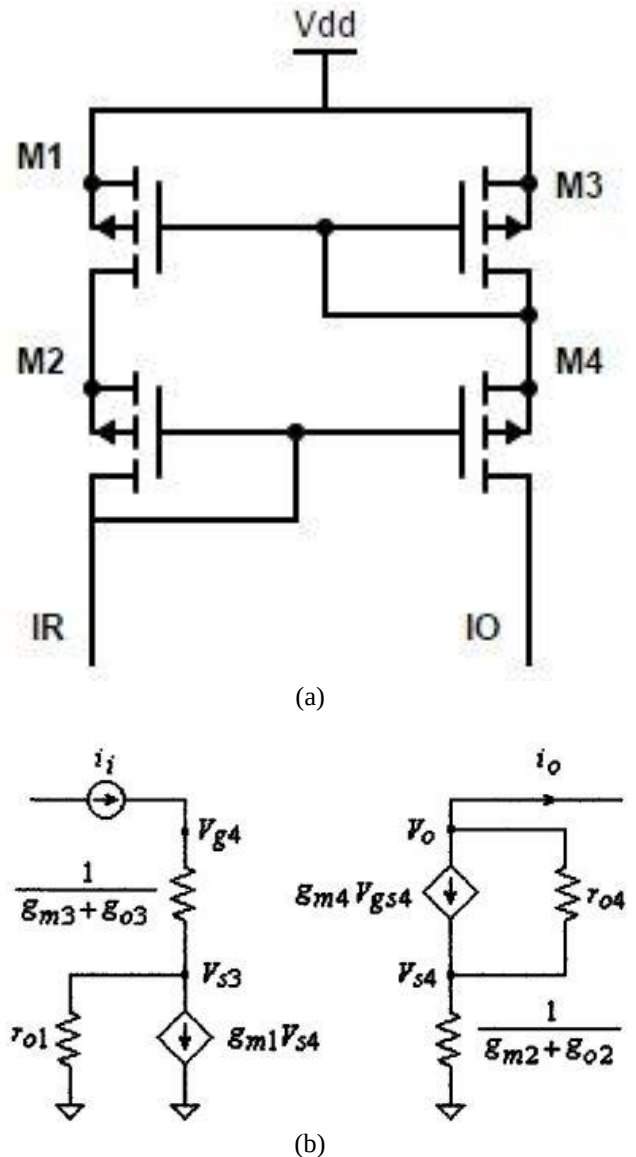


Figure 3: (a) Modified Wilson current mirror, (b) Small signal analysis of modified Wilson current mirror.

For small signal analysis of modified Wilson current mirror is shown in Figure 2 (b). Transistor M3 is approximated as a resistor with a value of $(g_{m3} + g_{o3})$, where g_{m3} and g_{o3} are the transconductance and output conductance of M3, respectively, and M1 is modeled as a voltage controlled current source with a transconductance gain of g_{m1} and output resistance r_{o1} [9].

For improved Wilson current mirror the increase in the output resistance is paid for by a reduction in the output dynamic range. The minimum output voltage for modified Wilson current mirror is given by equation (1).

$$V_{out\ min} = V_{TH} + 2.V_{DSAT} \quad (1)$$

3.2 Proposed ELS

The proposed enable level shifter structure is as shown in Figure 4. This consist of modified Wilson current mirror and a NOR structures. The Wilson current mirror ensures the very low static current in transistors [10]. The MWCM structure balances the rising and falling delay and performs the

function of level shifting. The inverter path is designed to reduce the rising delay due to PMOS transistors and to maintain a moderate duty cycle. The complementary OR structure gives the faster switching by comparing the two input given to it. Finally the NOR structure is given to buffer the output and to perform the function of isolation cell. The level shifter is transparent when the enable signal (EN) is at 0V, but it pulls down the output whenever the enable is at VDDL.

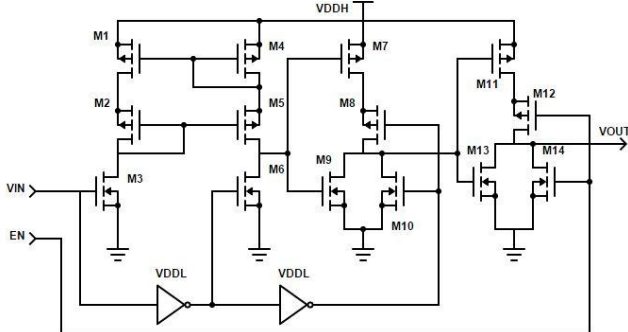


Figure 4: Proposed enable level shifter.

To analyze the proposed circuit we will consider both conditions of input signal. When the input is switching low-to-high and enable signal is at low, the M3 is turned on and M6 is turned off. The gate of the M7 and M9 charges through current mirror output and the transistors M10 and M8 are charged through inverter path. One of these two signals, which rises faster will switch the output complementary OR structure. The similar analysis can be done when input switches high-to-low. When the enable signal is high the output is pulled down to zero.

Table 1: Transistors sizes

Transistors	W/L [μm]
ELS PMOS	0.3/0.15
ELS NMOS	0.2/0.6
Inverter PMOS	0.3/0.6
Inverter NMOS	0.2/0.15

Table I gives the transistors size of ELS are reported. Transistors with a channel length of $0.15\mu\text{m}$ were used in the voltage conversion stage and the output complementary OR structure, to reduce sub-threshold leakage currents. On the contrary, since the leakage current is a minor issue for the input inverter, it has been made with minimum channel length devices, thus improving the speed.

4. Results and Discussions

Simulations are performed using Synopsys HSPICE tool. The MOSFET model used is PTM model with level 54 and typical operating process corner. For the simulation of delay and power analysis, input voltage transition time and the output load capacitance are varied.

The MOSFET model used at typical process and 25°C operating temperature. The proposed ELS can operate wide range of input voltage. The ELS is bi-directional which means it is capable of converting voltage levels HIGH-to-

LOW as well as LOW-to-HIGH. Existing single-supply level shifters are either unidirectional, have high leakage current or are functional to limited range of input and output supply voltage [11]. The DC analysis of ELS is shown in the Figure 5. It is seen that output voltage switches when 0.2V this is because delay due to low voltage. The output voltage remains at nominal operating voltage 0.9V even if the input voltage increases more than 1.5V.

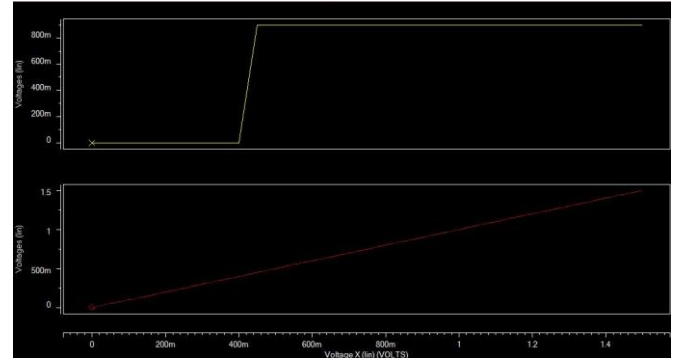
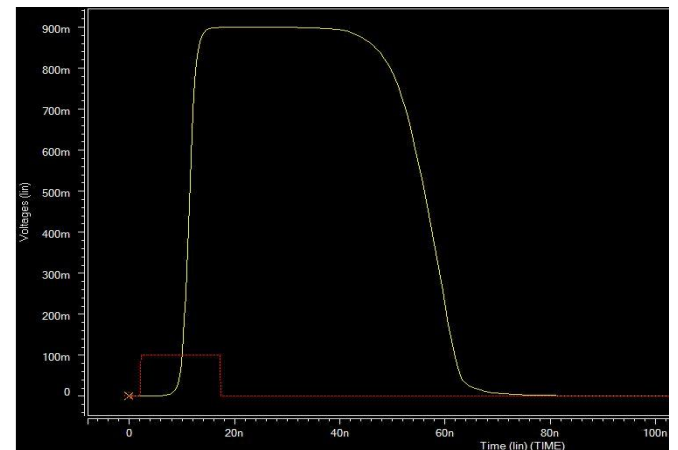
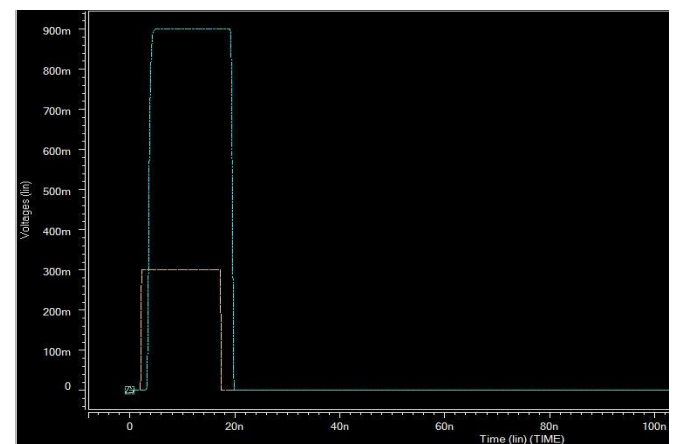


Figure 5: DC analysis of proposed ELS.

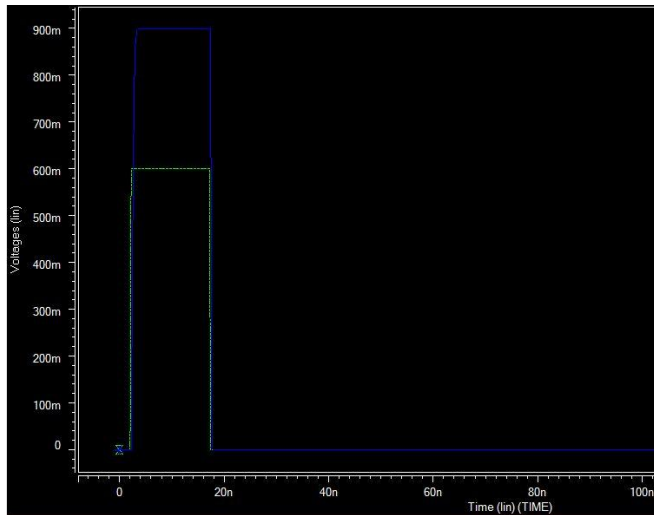
The level shifting function can be seen in the Figure 6. The input voltages ranging from 0.1V to 1.2V are given to the ELS. Even at the lower voltages the modified Wilson current mirror works, but at the cost of increased delay. The level shifter output is maintained at 0.9V.



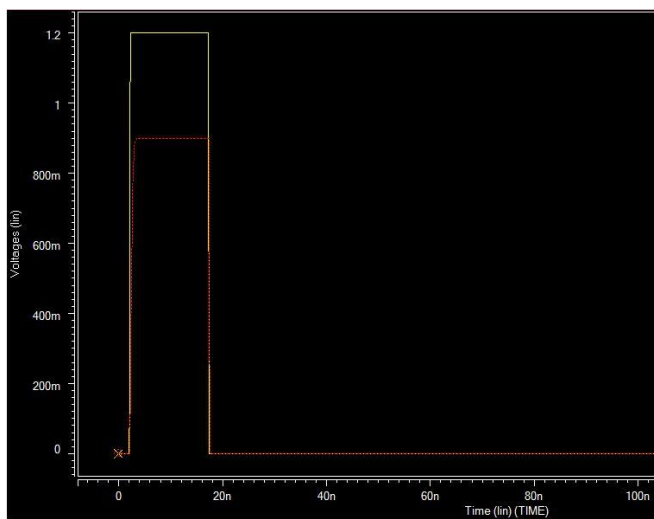
(a)



(b)



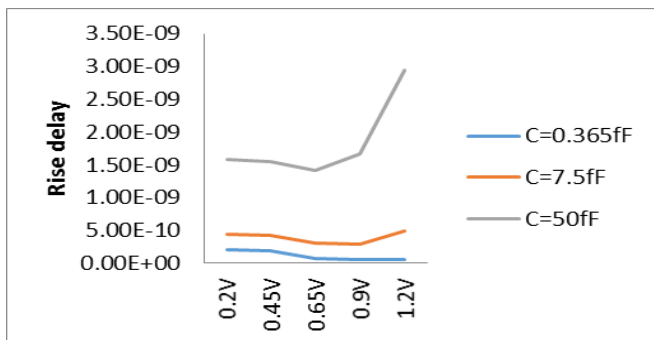
(c)



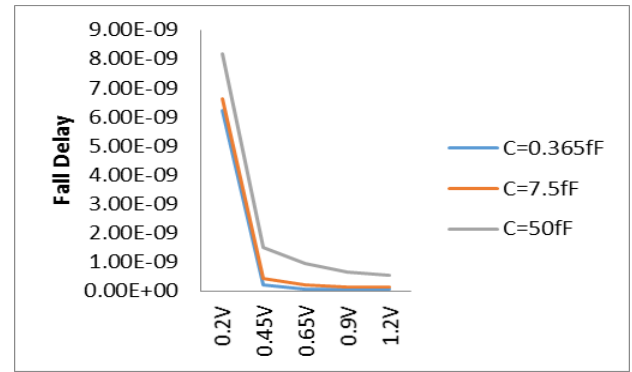
(d)

Figure 6: (a) Level shifting 0.1V to 0.9V, (b) Level shifting 0.3V to 0.9V, (c) Level shifting 0.6V to 0.9V, (d) Level shifting 1.2V to 0.9V.

The delay analysis has done using the transition time of 0.2ns. The load capacitance is varied in the range of 0.365fF to 50fF and the input voltage also varied from 0.2V to 1.2V. The result is shown in Figure 7.



(a)

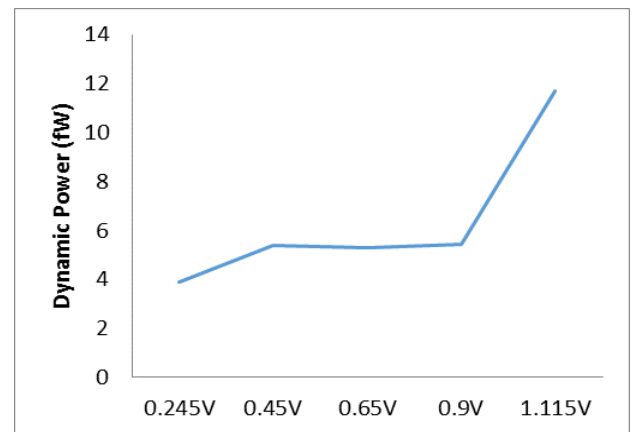


(b)

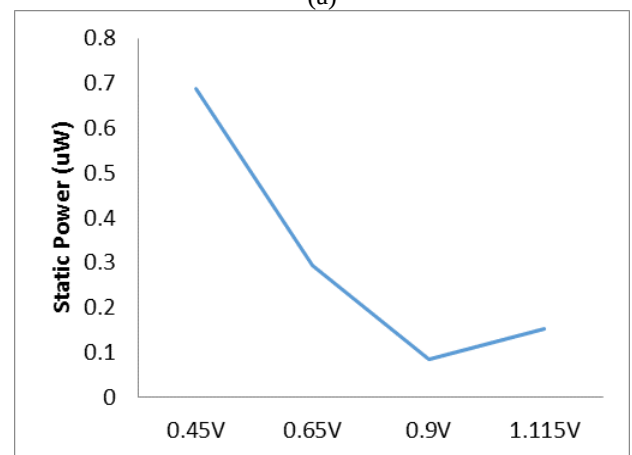
Figure 7: (a) Rise delay, (b) Fall delay

It can be observed from the graph that the delay of the cell is minimum at the nominal operating voltages. It is also observed that the transition time of the input signal affect delay significantly only when it is more than 1ns, so effect of transition time is not considered.

Similarly we have power analysis for the ELS. The power analysis is done using standard load capacitance of 7.5fF and transition time of 9.2ns. The power consumption data of the proposed ELS can be seen in Figure 8. The static and dynamic power consumption is least in the normal operating voltages.



(a)



(b)

Figure8: (a) Dynamic power consumption, (b) Static power consumption.

5. Conclusions

We have presented new ELS suitable for robust logic voltage shifting from near/sub-threshold to above threshold domain and isolating the shutdown region from the active region. The proposed ELS is designed for wide range of operating voltages. The circuit exploits the strategy to give the wide operating voltage at delay values less than 0.5ns at nominal operating voltage. It is also optimized for low power consumption, dynamic power consumption is 5fF and the static power consumption is near 100nW.

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