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A Review on Advancements beyond Conventional Transistor Technology

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Abstract: ***As continuous geometric scaling of conventional metal oxide semiconductor field effect transistors(MOSFETs) are facing many fundamental challenges, therefore, new alternatives has to be introduced to provide high performance integrated chips. This paper gives insight on various recent innovations in device engineering for microelectronics and nanoelectronics. The recent developments are mainly based on new materials and new structures which include strained Si, high-K/metal gate, SOI technology, multiple gates. In the proposed paper concepts beyond CMOS, carbon nanotube FET (CNTFET) and tunnel FET (TFET) are examined which brings a revolutionary change to semiconductor industry.***

Keywords: MOSFETs, Strained Si, SOI, multiple gates, CNTFET, TFET.

1. Introduction

Over the past four decades, the semiconductor industry has been providing the continuously improved performance of the systems. The basic principle behind delivering the improved systems by the semiconductor industry lies with Moore's law which states that number of transistors per IC doubled every two years [1]. The persistent scaling of MOSFET's has enabled increase in transistor density and speed of the ICs. Moving towards nanometre technology regime i.e. below 30nm constant shrinking of conventional MOSFET needs technological evolution and revolutions to reduce physical barriers raised due to fundamental physics. On the other hand, in deeply scaled MOSFET electrostatic integrity and device variability are highly affected. The challenges faced by the conventional MOSFET's are excessive gate and substrate leakage, high on-off current ratio due to the doping profile in channel and source/drain region, quantum-mechanical tunnelling of carriers, channel mobility degradation which limits speed of system, gate stack reliability, exponential increase in source to drain sub-threshold leakage current. In order to overcome these problems, device engineers are introducing new materials and modified transistor structures. To lessen some problems related with scaling some advanced CMOS approaches such as stained Si, high-K/metal gate, SOI technology and multigate transistors have been studied. From long term perspective, around 5nm technology all these advanced CMOS approaches will not be able to prevent running into physical limitations [2]. In this case, shift occurs from conventional microelectronics technology to nanotechnology where carbon nanotube field effect transistors (CNTFETs) are realised to deliver higher transistor performance with increasing energy efficiency.

2. Advanced CMOS Approaches

Several advanced techniques are discussed here to reduce the drawbacks of CMOS scaling.

2.1 Strained Si

Strain is the property to enhance the mobility i.e. increases carrier velocity in MOS channels resulting in high drive current (i.e. I_{ON}) under same conditions. This means that lower supply voltage and thicker gate oxide under same drive current reduces the trade-off among current drive, power consumption and short channel effects. Strained silicon is a layer of silicon in which the silicon atoms are stretched beyond their normal inter atomic distance as shown in figure 1.

Strain can be introduced in MOS channel by different ways, either locally or globally. Biaxial tensile strain or global strain is generated by growing thin layer of epitaxial Si on material with larger lattice constant [3], [4] which is mainly responsible for strain production in Si lattice. There are significant disadvantages of this approach like self-heating issue due to the lower thermal conductivity of the thick SiGe layer and close control of dislocation defects in the epitaxial layer. Here, the self-heating characteristics can be improved by reducing the SiGe layer thickness in the MOS structure. The remarkable property is that the electron mobility enhancement exists even at high effective fields where the so-called surface roughness scattering was expected to dominate the mobility. The electron mobility has been enhanced by 70 % leading to a speed improvement around 30 % [5]. The local or uniaxial strain is incorporated in channel at the time of transistor fabrication process via tensile capping layer. The locally induced strain layers increases mobility of both type of carriers, promote thermally grown advanced gate oxides on pure Si as opposed to SiGe and allow use of standard CMOS process with slight modification and low cost.

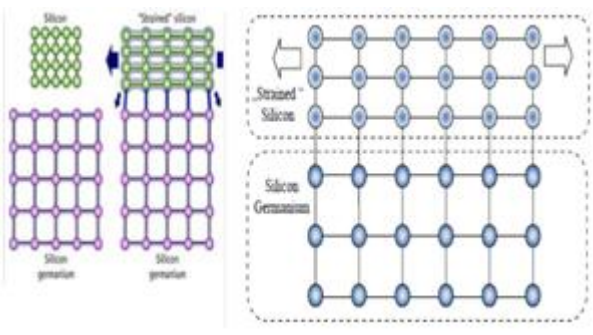


Figure 1: Illustration of straining of silicon by means of silicon germanium

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2.2 High-K/Metal Gate

Constant scaling of device channel length for nanoscale technologies offers scaling of gate oxide which results exponential increase in gate leakage current. In order to suppress the short channel effects in nanometre devices with planar structure without compromising the ON state current of transistor, reduced electrical oxide thickness (EOT) of gate dielectric are required. A gate material having high gate dielectric constant (K) than that of SiO_2 will achieve smaller EOT even with larger physical thickness as compared to SiO_2 shown in figure 2. The high-K gate insulators used are Ta_2O_5, TiO_2, ZrO_2, HfO_2, Y_2O_3, La_2O_3, Al_2O_3, and Gd_2O_3 and their silicates. Fully depleted silicon on insulator (FD-SOI) or thin film SOI such as FINFET has improved short channel control and thus loosens up the requirements for EOT scaling.

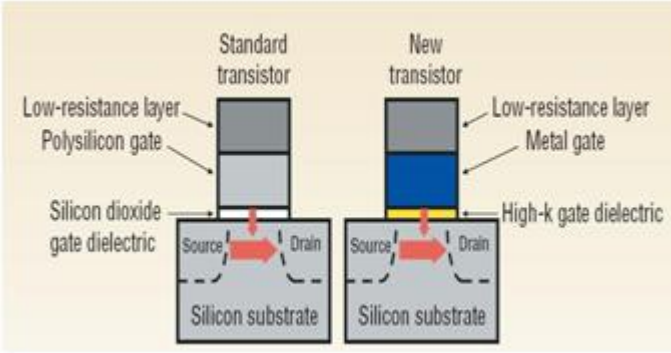


Figure 2: View of Standard transistor and high-K/metal gate transistor

Direct interface between high-K dielectric and poly-silicon gate has some limitation such as photon scattering which degrades the carrier mobility, thermal instability and a direct shoot up in threshold voltage value. To eliminate these limitations, the metal gate electrode is used with the high-K gate insulator. The most important consideration for the gate electrode is work function of the material. Significant research was done to find the metal electrodes with correct work function. Such metals must withstand the high thermal requirements and provides the opportunity to choose the work function of gate and to redesign the device to get the best combination of work function and channel doping. For bulk or partially depleted FETs the work function value for gate electrode lies near the conduction and valence band. For double gate FETs the short channel effects are controlled by the device geometry but the threshold voltage is mainly estimated by the gate work function so selection of gate electrode becomes important in the case of double gate FETs.

2.3 SOI Technology

Contrary to massive Si transistor, Si on insulator (SOI) technology has become attractive way for the fabrication of advanced CMOS IC's because of low supply voltage and minimum power consumption features. The SOI structure is similar to the conventional bulk except the presence of the buried layer which is formed by the implantation of oxygen ions in the Si as shown in figure 3.

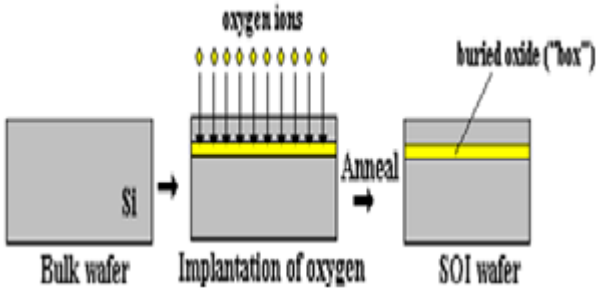


Figure 3: Formation of SOI wafer

The phenomenal SOI technology structure provides full dielectric isolation to active Si layer from the main substrate with the help of buried oxide layer. This allows the selection of relatively high resistivity main substrate .Consequently, usage of high resistivity main substrate provides significant reduction in parasitic [6] and leakage current in substrate. The salient features of SOI technology are excellent device isolated structure, low I_{OFF} or subthreshold leakage and high drive current [7], high reliability and high speed due to elimination of vertical as well as sidewall capacitances .SOI CMOS transistors suffers from self heating effect which appears only when the transistor is in conduction mode. But this effect certainly will not eliminate the global usage of SOI for CMOS IC's.

2.4 Multigate Transistors

Multigate transistors are more promising candidate for enhancing the performance and scaling properties of device. These are used to mitigate short channel effects such as DIBL, threshold voltage roll off and to get the precise control over channel current. DG-MOSFET with aligned planar gate structure provides improved channel control but its fabrication process is more challenging.

Further FinFET and Trigate FETs have emerged dominant owing to their ease of fabrication. FinFET can be built on both bulk as well as SOI. FinFET, a 3D or non planar structure where a thin Si channel is obtained by etching a narrow Si stripe called 'fin' with gate electrodes occupy the sidewalls of Si stripe. Unlike bulk FinFET in which all fins share a common substrate, fins in SOI FinFETs are physically isolated by very shallow trench isolation (VSTI).

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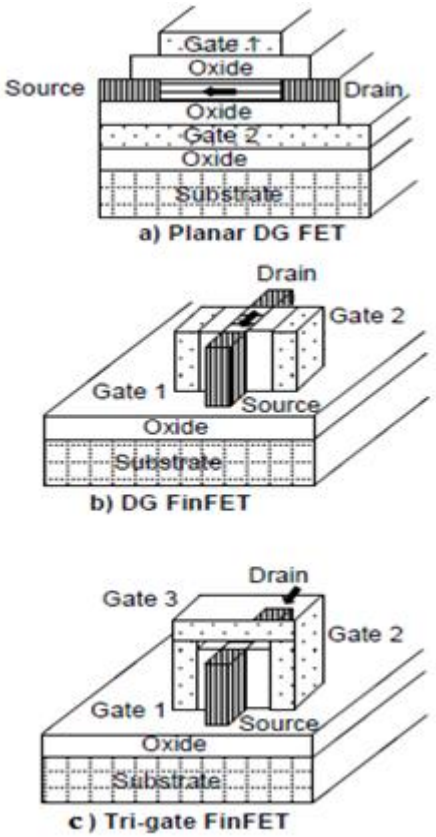


Figure 4: Illustration of multi-gate MOSFETs

FinFETs are classified as shorted gate FinFET (SG-FinFET) and independent gate FinFET (IG-FinFET). In SG-FinFET, both the front and back gates are physically shorted provided with same voltage signal. In DG-FinFET, the gates are isolated with each other. This isolation property offers flexibility of applying different signal to both gates.SG-FinFETs shows high drive current and higher sub threshold leakage (i.e. I_{OFF}) compared to the IG-FinFETs. In Trigate FETs, thickness of dielectric layer placed on the top of fin is reduced in order to create the third gate. Third gate adds process complexity but has some advantages like reduced fringe capacitances and additional transistor width [9].

The more evolutionary segmented FET (SegFET) structure is a hybrid approach that combines the benefits of both planar bulk MOSFETs (i.e. low process complexity) and thin body transistor structure (i.e. low aspect ratio stripes). The fabrication process for SegFET is similar to planar bulk except substrate material. The former uses corrugated Si substrate [8] instead of Si substrate used for planar bulk MOSFETs. MOSFET's on corrugated substrate with precisely spaced stripes provides low leakage and high performance device. The multiple parallel Si segments of equal width on corrugated Si substrate act as channel. Areas between the channels are filled with very shallow trench isolation (VSTI) oxide. Gate control is improved for the SegFET compared to conventional planar MOSFET by fringing electric field through VSTI regions. For further enhancements of gate control, top surface of each Si stripe is wrap up with gate electrode. SegFET structure has superior electrostatic integrity i.e. reduced short channel effects compared to conventional MOSFET structure.

3. Beyond CMOS Approaches

3.1 Carbon Nanotube FET (CNTFET)

CNTFET has emerged as the strongest contender to replace current technologies for a range of electronic application with exceptional mechanical, thermal and electrical properties. Carbon nanotube is viewed as rolled up grapheme sheet with a diameter of nanometre dimensions while the lengths are typically in micrometer regime. In addition, graphene is a 2 dimensional material consisting of a mono atomic layer of carbon atoms that are densely packed in a honeycomb crystal lattice [11]. There are two types of carbon nanotube one is single walled carbon nanotube (SWCNT) and other is multi walled carbon nanotube (MWCNT) shown if figure 5. SWCNT is a most promising type to fabricate CNTFET. CNTFETs uses the semiconducting carbon nanotube as a channel.

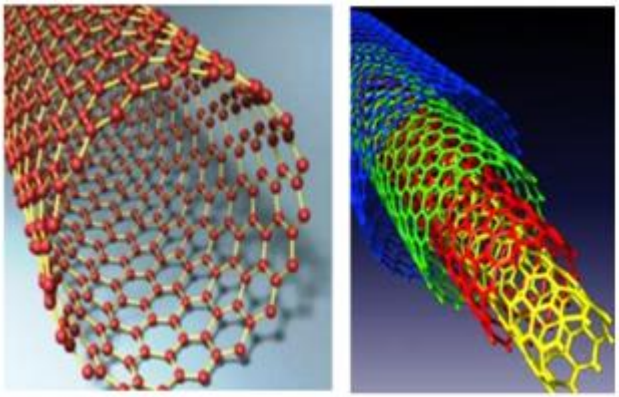


Figure 5: Single walled CNT (SWCNT) and multi walled CNT(MWCNT)

CNTFETs are similar to MOSFETs except with a difference that former uses carbon nanotube as a channel whereas MOSFETs channel is formed with heavily doped Si substrate. Some distinct properties of CNTFET are:

- Carbon nanotube has 1-D nature due to which it supports ballistic transport where mean free path is longer than the path. Thus, scattering probability is reduced to very large extent.
- CNTFETs have potential for low thermal noise due to longer mean free path. Since mean free path is inversely proportional to temperature.
- The nanotubes conducts mainly on its surface where all carbon atoms bonds are saturated resulting no interface states .On other hand, no dandling bonds are present to form interface states. This helps in achieving excellent channel control and higher linearity is obtained due to linear dependence between drain current and gate-substrate voltage above threshold [12].
- CNTFETs offers larger drive current i.e. I_{ON} than Si and SOI MOSFETs. The OFF state current is greatly being reduced in CNTFETs.

CNTFET's has potential to control threshold voltage by changing the chirality vector, or the diameter of the CNT. Chirality vector refers to the angle in which carbon atoms are arranged along the tube. One of the major challenge is growth of metallic tubes during fabrication process of carbon nanotubes resulting unfavourable impact on power, delay and functional yield on CNT based circuits. A further

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challenge for CNTFET technology is the control of the carbon nanotube size, type, and chirality which uniquely determine its electrical properties. Finally, minimizing parasitic resistance and capacitance while developing a fabrication process and device structure are important.

3.2 Tunnel FET (TFET)

Tunnel FET based on gate controlled band to band tunnelling mechanism unlike conventional MOSFETs based on thermionic emission. TFET has gained a lot of recent interest due to features such as their potential for reducing power consumption, extremely small sub-threshold swing over small voltage swing and feasibility of integration with standard CMOS process flow. The common TFET device structure consists of asymmetrical source/drain doping [10] unlike MOSFETs. TFET is a gated p-i-n diode which operates when diode is under reversed biased condition and voltage is applied. In figure 6 the n-i-p configuration of TFET is shown. The 'i' stand for intrinsic region which means equal number of electrons and holes are present in this region. This intrinsic state corresponds to minimum resistivity which also pushes up the energy bands in channel, generating thick energy barrier that charge carriers in source are unlikely to move across through it. In the OFF state, there exists a large potential barrier between the source and channel which prohibits occurrence of tunnelling. On applying gate voltage above threshold voltage, the potential barrier gets narrow enough to allow tunnelling of carriers as shown in figure 6 resulting significant current flow in the device.

For commercial realisation of TFET structure high current density is a key challenge, which is obtained by abrupt doping profile and higher doping levels. One of the technical key challenges in TFET is the alignment of gate to the junction. Like MOSFETs, the gate control is improved by shifting from single gate to double gate geometries.

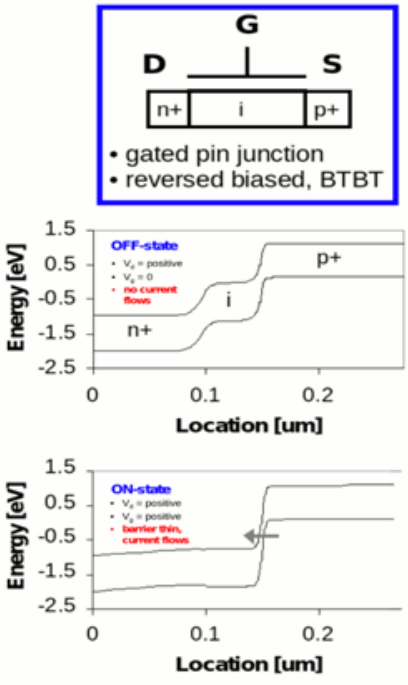


Figure 6: Illustration of N-type TFET and its carrier tunnelling mechanism

4. Conclusion

In this paper, review on various advanced CMOS techniques and nanotechnology based concepts have been done. To extend the roadmap for few decades several advanced CMOS techniques such as strained Si, high K/metal gate, SOI and multi gate transistors have been introduced to reduce the scaling limits. But semiconductor industry has faced various challenges after the employment of new materials. Consequently, new scaled device structures will not allow conventional approach for further use. To overcome these challenges, there has been a paradigm shift from microelectronics to nanotechnology on a time scale of decades. Carbon nanotechnology is seen to be the future of microelectronics beyond CMOS technology. Therefore, CNTFET and TFET are introduced to design and implement reliable and durable high performance devices.

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