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A Control Scheme of Cascaded Multilevel Inverter Based D-STATCOM for Improving the Voltage Control and Reduce Total Harmonics Distortion

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Abstract: ***This paper presents an investigation of Nine -Level Cascaded H - bridge (CHB) Inverter as Distribution Static Compensator (DSTATCOM) in Power System (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses. The DST ATCOM helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL).The battery energy storage is integrated to sustain the real power source under fluctuating wind power. The D-STATCOM control scheme for the grid connected three phase four wire systems for power quality improvement (Reactive power control and harmonics) is simulated using MATLAB/SIMULINK in power system block set. The effectiveness of the proposed scheme relives the main supply source from the reactive power demand of the load. The results are obtained through Mat lab / Simulink package.***

Keywords: DST ATCOM, level shifted pulse width modulation (LSPWM), phase shifted pulse width modulation (PSPWM), proportional-integral (PI) control, CHB multilevel inverter, D-Q reference frame theory

1. Introduction

Modern power systems are of complex networks, where hundreds of generating stations and thousands of load centers are interconnected through long power transmission and distribution networks. Even though the power generation is fairly reliable, the quality of power is not always so reliable. Power distribution system should provide with an uninterrupted flow of energy at smooth sinusoidal voltage at the contracted magnitude level and frequency to their customers. PS especially distribution systems, have numerous non linear loads, which significantly affect the quality of power. Apart from non linear loads, events like capacitor switching, motor starting and unusual faults could also inflict power quality (PQ) problems. PQ problem is defined as any manifested problem in voltage current or leading to frequency deviations that result in failure or mal-operation of customer equipment. Voltage sags and swells are among the many PQ problems the industrial processes have to face. Voltage sags are more severe. During the past few decades, power industries have proved that the adverse impacts on the PQ can be mitigated or avoided by conventional means, and that techniques using fast controlled force commutated power electronics (PE) are even more effective. PQ compensators can be categorized into two main types. One is shunt connected compensation device that effectively eliminates harmonics. The other is the series connected device, which has an edge over the shunt type for correcting the distorted system side voltages and voltage sags caused by power transmission system faults.

The STATCOM used in distribution systems is called D-STATCOM (Distribution-STACOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. This paper presents a D-STATCOM with a proportional integral controller based CHB multilevel inverter for the harmonics and reactive power mitigation of the nonlinear loads.

2. Design of Multilevel Based DSTATCOM

2.1 Principle of DSTATCOM:-

A Distribution STATIC COMPENSATOR (D-STATCOM) is a voltage source converter (VSC)-based power electronic device. Usually, this device is supported by short-term energy stored in a dc capacitor. The D-STATCOM filters distribution bus current such that it meets the specifications for utility connection. If properly utilized, this device can cancel the effect of poor load power factor such that the current drawn from the source has a near unity power factor and the effect of poor voltage regulation. The two main objectives in D-STATCOM connection are:

i. Load compensation of unbalanced systems
ii. Power factor correction

Here is the Source voltage and is the Output voltage and R is the resistance and L is the inductance of the converter. A 9-Level Cascaded H-Bridge inverter is in parallel with the power line through the reactor. By adjusting the phase and

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magnitude of the AC output voltage of the converter, the converter can sent or absorb reactive power that meets the requirements and achieves the dynamic reactive power compensation. This is the basic principle of CHB-D-STATCOM.

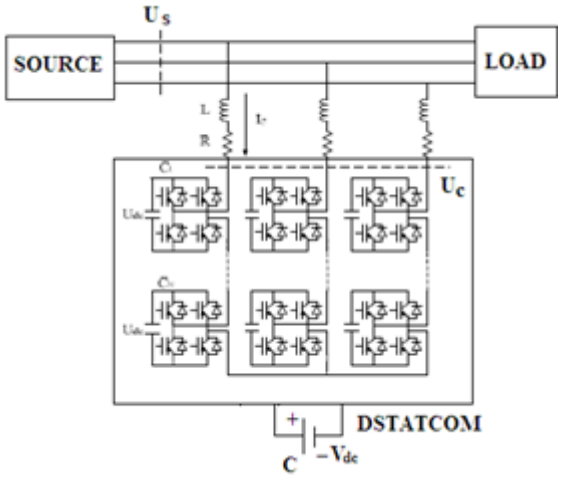

Figure 1: Schematic diagram of DSTATCOM

The voltage drop of the connected reactor has generated by the compensation current it can also filter the some of the high harmonics are generated by the source side. If the phase angle difference of between each cascaded module, no active power is consumed, and the capacitor voltage does not changes. Actually, if the phase angle difference produces minor changes, the active power flow between the compensator and the power grid and then the Dc bus voltage will produce changes. So, by adjusting the output voltage and currents of the H-Bridge modules, the DC Bus voltage can also be corrected. If the DC Bus voltage is controlled the reactive power can also be controlled. The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power
2. Correction of power factor
3. Elimination of current harmonics.

The shunt injected current Ish can be written as,

$$I_{sh}=I_l-I_s=I_l-(V_{th}-V_l)/Z_{th}$$

$$I_{sh}/_^{\eta}=I_l/_^{-\theta}$$

2.2 Control for reactive power compensation:-

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

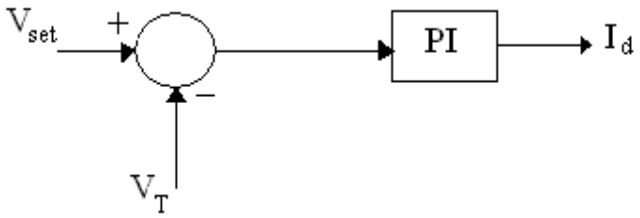

Figure 2: Control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the angle δ, which is provided to the PWM signal generator. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The PI controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

2.3 Control for Harmonics Compensation

The Modified Synchronous Frame method is presented in. It is called the instantaneous current component (id-iq) method. This is similar to the Synchronous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages V(a,b,c) and the available currents (a,b,c) in α-β components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where „θ" represents the instantaneous voltage vector angle.

$$\begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix} = [C] \begin{bmatrix} I_{la} \\ I_{lb} \\ I_{lc} \end{bmatrix}$$

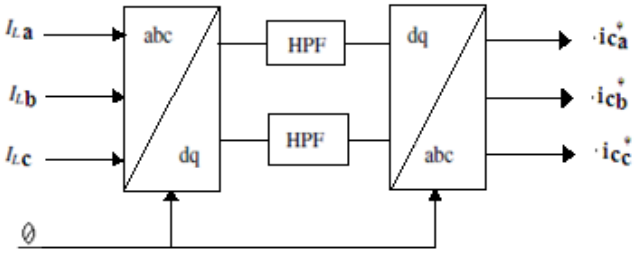

Figure 3: Block diagram of SRF method

Fig. 3 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle θ is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and unbalance; therefore $d\theta/dt$ may not be constant over a mains period.

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2.4 Cascaded H-Bridge multilevel inverter:-

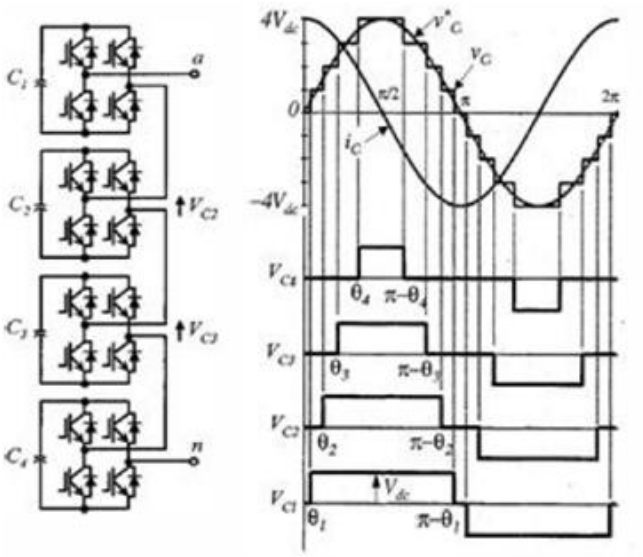

Figure 4: Circuit of the single cascaded H-Bridge inverter

Figure 4 shows the circuit model of a single CHB inverter configuration. By using single R-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+l and voltage step of each level is given by Vdcl2n, where n is number of R-bridges connected in cascaded. The switching table is given in Table 1.

Table 1: Switching table of single CHB inverter

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

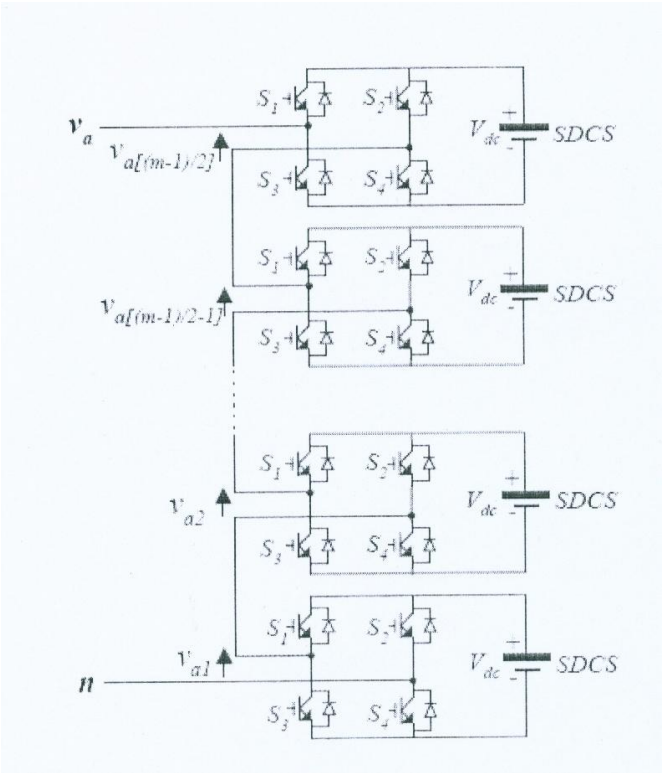

Figure 5: Block digram of 9-level CHB inverter model

The switching mechanism for 9- level CHB inverter is shown in table-2.

Table 2: Switching table of 9-level CHB inverter

SWITCHES TURN ON	VOLTAGE LEVEL
S1, S2	VDC
S1,S2,S5,S6	2VDC
S4,D2,S8,D6	0
S3,S4	-VDC
S3,S4,S7,S8	-2VDC

2.5 Design of Single H-Bridge Cell

2.5.1 Device Current

The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, d = 1/2(l +Kmsinωt), Where, m =modulation index K = + 1 for IGBT, -1 for Diode. For a load current given by

Iph = $\sqrt{2}$ I sin (wt - ¢)

Then the device current can be written as follows.

:. I_{device} = ($\sqrt{2}$ /2)* I *sin(wt - Ø)x (1 + km sin wt)

2.5.2 IGBT Loss Calculation

IGBT loss can be calculated by the sum of switching loss and conduction loss.

The conduction loss can be calculated by,

Pon(IGBT) =Vceo * I avg (igbt) + I2 rms (igbt) * rceo

p on (IGBT) = Vceo * Iavg (igbt) + I2 (igbt) * rceo

Values of Vceo and rceo at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT, as shown in the figure 6.

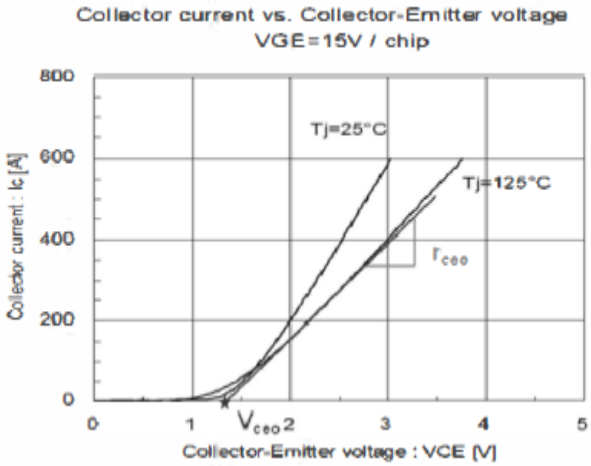

Figure 6: IGBT Output Characteristics

So, the sum of conduction and switching losses is the total losses given by PT(IGBT) = Pon(IGBT) + Psw(IGBT)

2.5.3 Diode Loss Calculation:-

The DIODE switching losses consist of its reverse recovery losses; the tum-on losses are negligible.

$$E_{rec} = a + ci^2$$

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2.5.4 PWM Techniques for CHB inverter:-

The most popular PWM techniques for CHB inverter are 1. Phase Shifted Carrier PWM (PSCPWM), 2. Level Shifted Carrier PWM (LSCPWM).

2.5.4.1 Phase Shifted Carrier PWM (PSCPWM):-

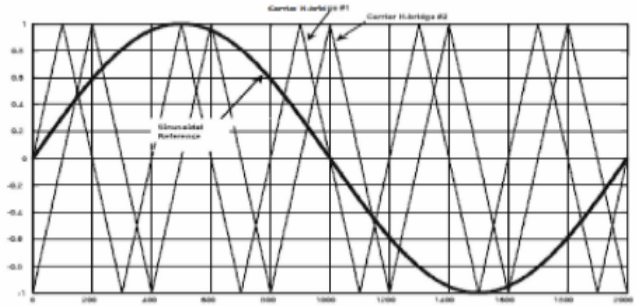

Figure 7: Phase shifted carrier PWM

Figure-7 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 180 /m (No. of levels) for cascaded inverter 1S introduced across the cells to generate the stepped multi level output waveform with lower distortion.

2.5.4.2 Level Shifted Carrier PWM (LSCPWM):-

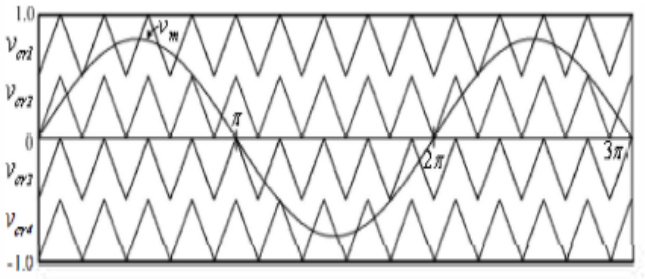

Figure 8: Level shifted carrier PWM

Figure-8 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar width modulation and bipolar pulse pulse width modulation respectively, providing an even power distribution among the cells. A carrier Level shift by 1/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform.

3. Matlab / Simulink Modeling and Simulation Results

Figure-9 shows the Matlab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of llkv, 50 hz AC supply, DC bus capacitance ISSOe-6 F, Inverter series inductance 10 mH, Source resistance of 0.1 ohm and inductance of 0.9 mHo Load resistance and inductance are chosen as 30mH and 60 ohms respectively.

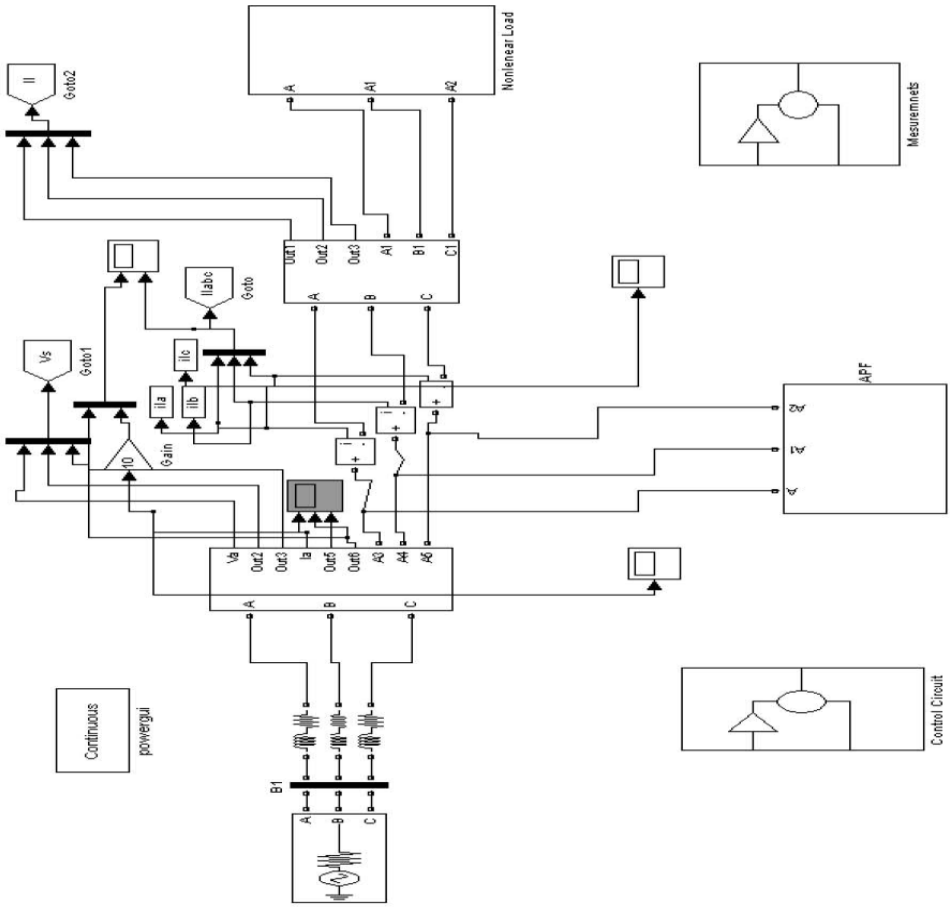

Figure 9: MATLAB/Simulink power circuit model of DSTATCOM

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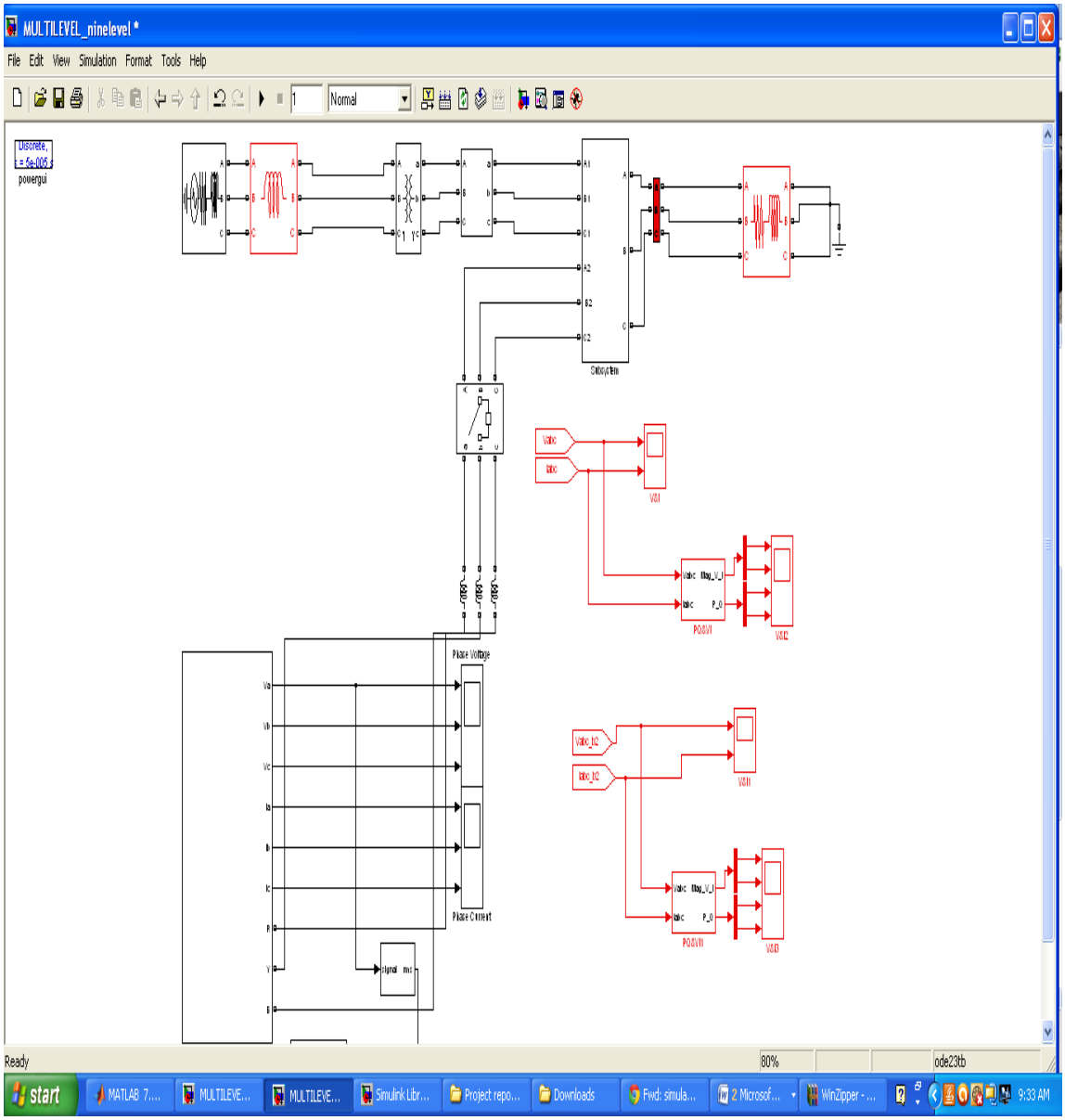

Figure 10: Overall Simulation Diagram

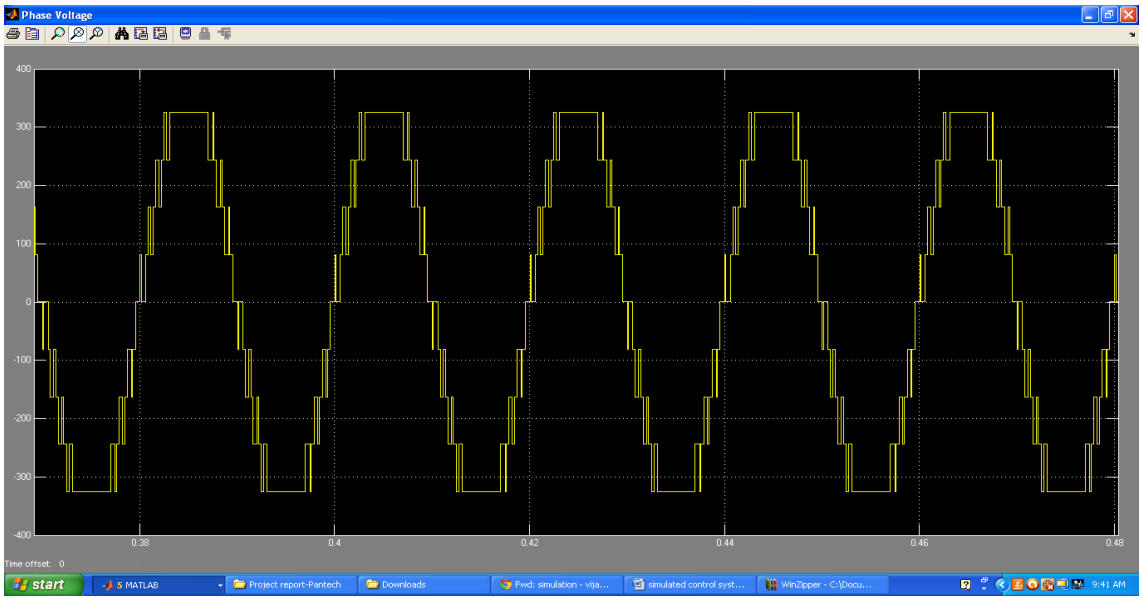

Figure 11: shows the phase- A voltage of NINE LEVEL output of phase shifted carrier PWM inverter.

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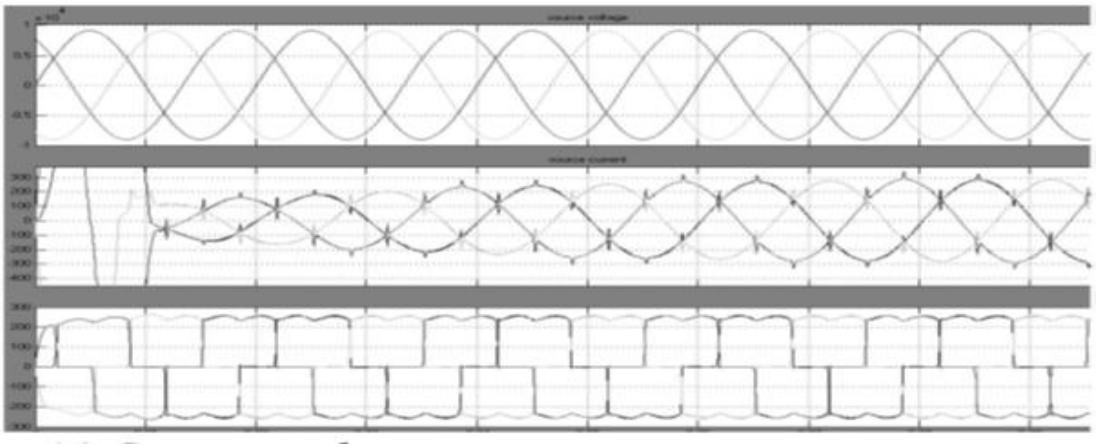

Figure 12: shows the three phase source voltages, three phase source currents and load currents respectively without DST ATCOM. It is clear that without DSTATCOM load current and source currents are same.

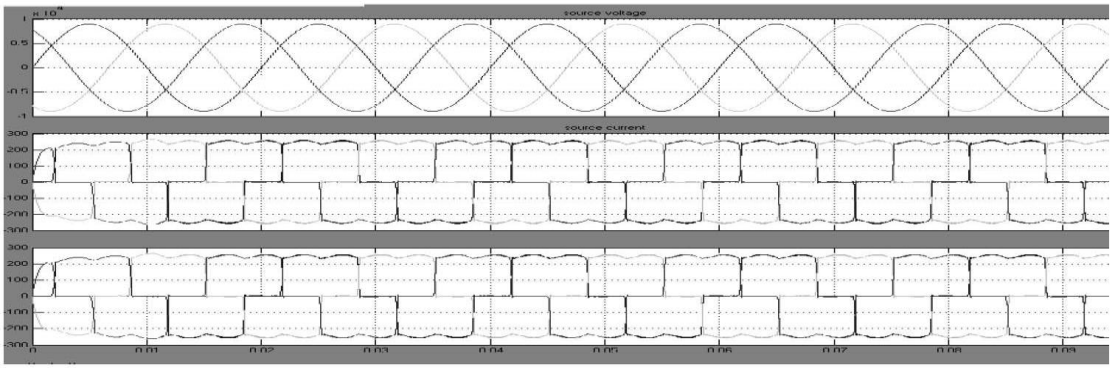

Figure 13: shows the three phase source voltages, three phase source currents and load currents respectively with DST ATCOM. It is clear that with DST ATCOM even though load current is non sinusoidal source currents are sinusoidal.

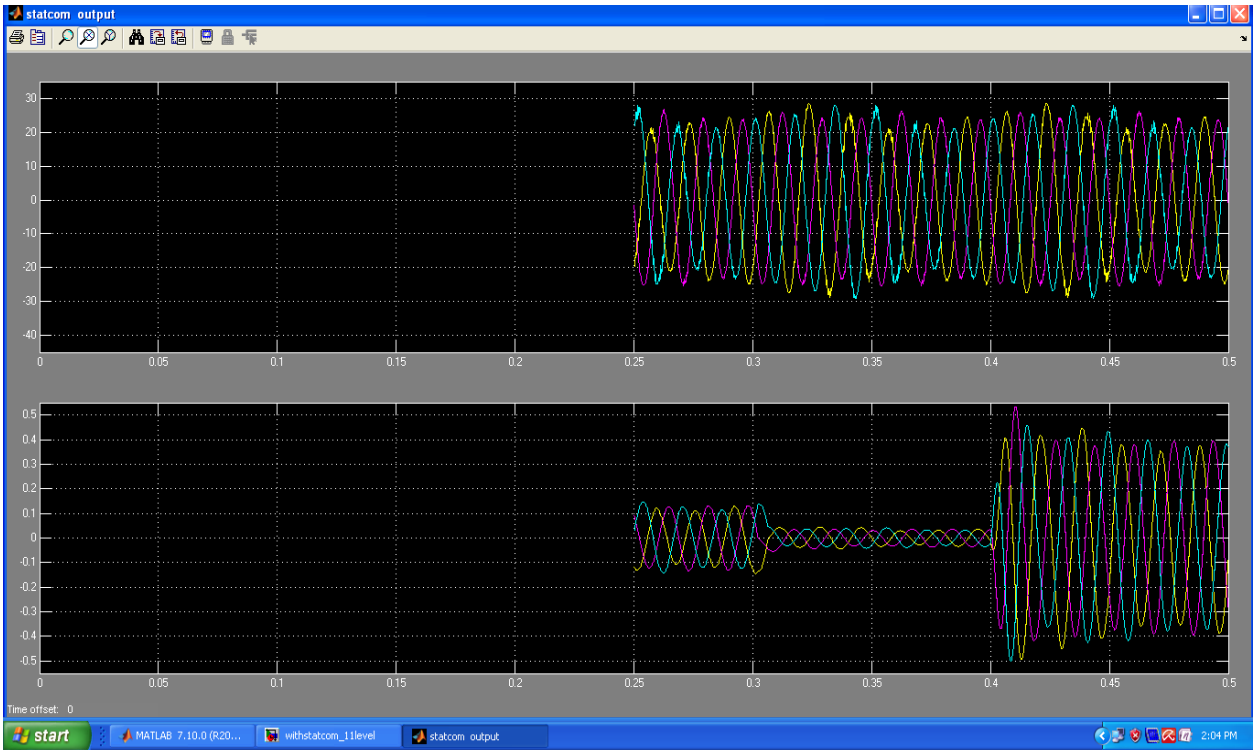

Figure 14: shows the matlab / Simulink model of proposed compensator using phase shifted modulation technique based DSTATCOM.

Figure-15 and 16 have confirmed that the Power Factor of load increased to 0.985 after the access of the DSTATCOM. So that, the load side current and the source side current are the same for all cases, which verifies satisfactory compensation effect of DSTATCOM.

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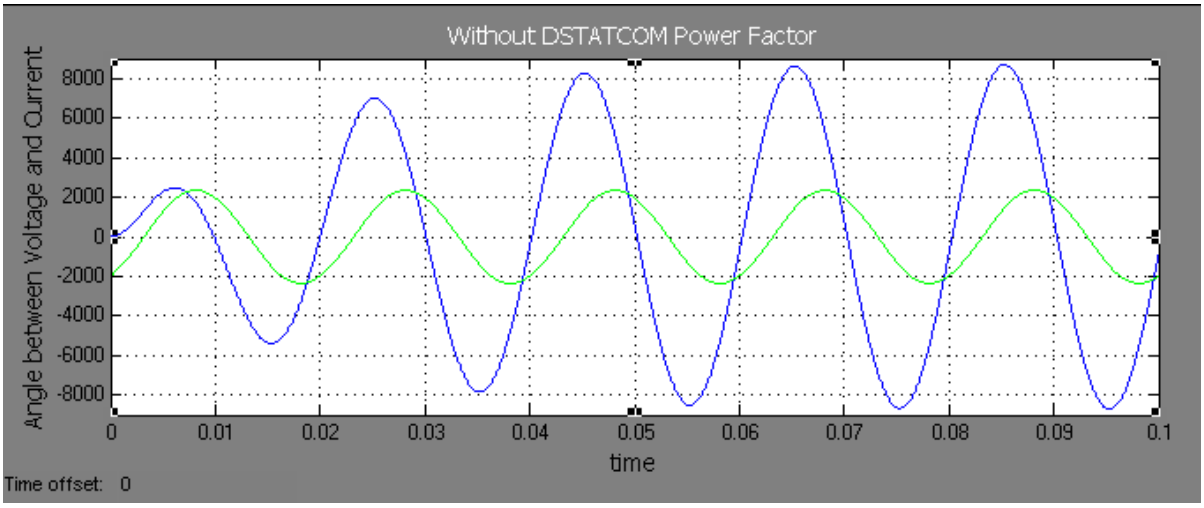

Figure 15: Before Compensation of Power Factor

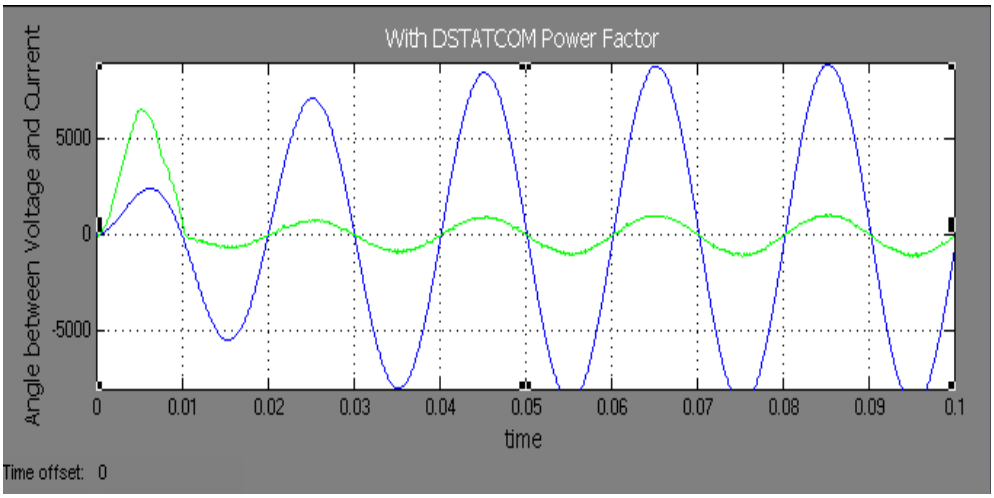

Figure 16: After Compensation of Power Factor

4. Conclusion

A D-STATCOM with nine level CHB inverter is investigated. Mathematical model for single H-Bridge inverter is developed which can be extended to multi H-Bridge. The source voltage, load voltage, source current, load current, power factor simulation results under non-linear loads are presented. Finally Mat lab/Simulink based model is developed and simulation results are presented.

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