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Design of Low Power CMOS Startup Charge Pump Based on Body Biasing Technique

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Abstract: ***CMOS is used to construct the integrated circuits with low level of static leakage. With this low level leakage we are designing all the transistor circuits in CMOS logic. To control this static leakage in the circuits the supply voltage is a major concern. Here the step-up converters with charge pump and the level for maintaining its threshold voltage (V_T) is to be analyzed and proposed. Here we are going to propose the novel approach as body bias effect and sub-threshold logic. This will be applied for the step-up converters for energy harvesting applications. The backward control is to be processed for control the internal voltage when the charge transfer switch could be in activation. When the supply voltage is to be raise from the fixed voltage level it will be turn OFF the transistor. The maximum level of the converters circuits contain the branch A and branch B which could be contains all p-MOS and n-MOS combinations. The oscillator circuit also to e designed and applied to the proposed six stage charge pump circuit to reduce the power consumption. To reduce the standby mode leakage we are designing the circuit by using power gating logic. These circuits are to be designed and verified by using the TANNER T-SPICE TOOLS.***

Keywords: Low power, Charge pump, Body bias, CMOS logic.

1. Introduction

A charge pump circuit provides a voltage or a voltage of reverse polarity to upgrade the [2] amplification process. In several applications like Power IC, continuous time filters, and EEPROM, voltages [3] on top of the facility provides square measure often times needed. Redoubled voltage levels square measure obtained during a [4] charge pump as a results of transferring charges to a electrical phenomenon load and do not involve amplifiers or transformers [12].

For that reason a charge pump may be a device of alternative in semiconductor technology [10] wherever traditional vary of operative voltages is proscribed. Charge pumps usually operate at high frequency level so as to [5] extend their output power among an inexpensive size of total capacitance used for charge transfer. This operative frequency is also adjusted by compensating [9] for changes within the power needs and saving the energy delivered to the charge pump.

Among several approaches to the charge pump style, the switched-capacitor circuits like Dickson [4] charge pump square measure very fashionable; as a result of they will be enforced on constant chip together with alternative [8] elements of AN integrated system. The voltage gain of Dickson charge pump is proportional to the amount of stages within the pump. it should price quite several [11] devices and silicon space, once a charge pump with the voltage gain larger than ten or twenty is required. Such high voltage gains square measure needed for low voltage EEPROMs, and generally quite 3 stages of Dickson charge pumps square measure used. Improved Dickson charge pumps for low voltage EEPROMs and flash recollections [9] square measure developed. Charge pump operates by shift ON and OFF an oversized range of MOS switches that charge and discharge an oversized range of capacitances, [13] transferring energy to the output load.

The required voltage level conversion and the amplification of the charge pump give the [5] better output and easily implemented in the all implementations. The devices that could be effort based on the all level of processing in the various that could be considered for [8] the leakage process. The mode of operation also to be varies and it could be provide various levels of operations based on the technology in the linear level of compensation. The most frequency adjustment could be from the 50Hz to the 500MHz. The architecture level conversion into the circuit design of process may or may not be vary from the IC'S [11].

So the designing process could be give the better result such as low power, better noise performance, and also to could not damage the devices [9].This condition could be satisfied as per the process of all level of variations from the related units of the charge pump circuits. The implementation could be analyzed as per the rules of the charge pump and the phase detector units. This could be implemented into the application [10] of PLL (Phase Locked Loop). This PLL give the frequency synthesizer for power grid applications for energy harvesting. This could be managed as per the elements of the switching activity from the main circuit.

2. Existing System

The charge pump circuit has to be design in the environment of short circuit current limit and the as well as the temperature protection. This could be used for the further processing of the voltage level of conversion from the circuit based on the all level of conversion of power and the current limit. This is mainly focused for the power grid applications. In existing system there are many charge pump has been designed and having many limitations.

In Dickson charge pump the respective switches could be given into the circuit that is the possible combination of the n-MOS and the p-MOS. It is shown in fig. This could be

switches as per the number of stages provided in the circuit combination of the charge pump. From the capacitance for charging and discharging units could be considered. In this charge pump circuit the extension could not be possible and cannot be added for the real time process. This could cause various errors during the testing of chips.

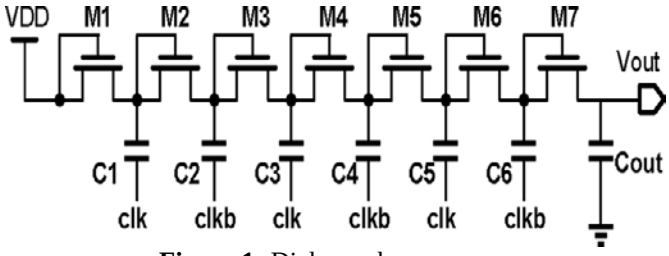

Figure 1: Dickson charge pump

In Wu Chang charge pump circuit the substantial uses of the circuit does not mismatch the p-MOS and the n-MOS conditions of the stages. And also this stage requires the more loop filters and also more current sources. Then this stage of the circuit occupies large silicon area of the chip causes more noises. Then charge pump circuit having the clock feed through and also this is not fully eliminating the charge sharing problems.

The Linear charge pump circuit having the limiting output voltage level form the desired area of the circuit conversion from the number of stages. This inverter level coupling stages could be providing amplitude degradation. And also providing switch mismatch condition for the all dead zone. By using this single ended coupling from the stages of all the coupling inverter gives the results for the more number of parasitic capacitance.

The main architecture of this system provides the non-ideal effects in the system. This could be causes more power consumption and could not be used for the implementation of the charge pump units. The required units cannot be adopted for the uses that carry the structural units from the circuit level of implementation process. The various units can be applied for the large stages and it also occupies the more area in the chip. The testing level of process cannot be accessed for the duration of the individual characteristics of the stages performing the operation of the all coupling. The main work could be considered for the process in the application of duration from the transmission gate charge pump structure.

3. Proposed System

The proposed charge pump has the six stages and then the coupling of the inverter stages and also for each branch. The body biasing and the backward control scheme has been applied to the each number of coupling stages and also could be provide the node level of separation from the each stages. The inverter coupling could be processed under the technology that could be beyond the network based applications.

The each node of operation having the reverse biasing voltages and also could be processed for the more stages form the applications. The proposed charge pump has been used for the real time implementation of the Phase Locked Loop. This is the feedback combining system for the linear process that could be connected to the phase detector and the voltage controlled oscillator for the process of all variations from the units. This could be fixed the low frequency signal for the extension of the phase variations from the two input signals.

The proposed charge pump circuit has been shown in Fig 2. The stages of inverter coupling have been adopted from the four level of inverter. This could be connected to the each branch of the circuits for the linear operation of the six stages of the proposed charge pump. The inverter coupling and also the capacitance (1pF) of the 1st stage of the two branches has been given to the input voltage supply.

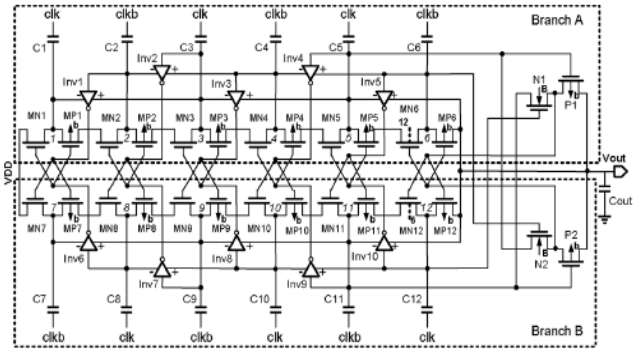

Figure 2: Proposed Charge pump with inverter stages

The capacitors from c1 to c6 in the two branches are used for the charging and discharging of the energy consumption based technique and also used for the amplification of the input voltage from the each stages. Then the body biasing can be applied from the node 1 of the c1 and the MN1 coupling with the MP1. This could be transferred to the branch B of the capacitance node 7 of c1. The coupling of the MN7 and the MP7 (Fig 3) of branch B gives the amplitude stage of first level voltage from the capacitor. The clock frequency has to be given into the circuit combination from the clk and clkb to the two branches.

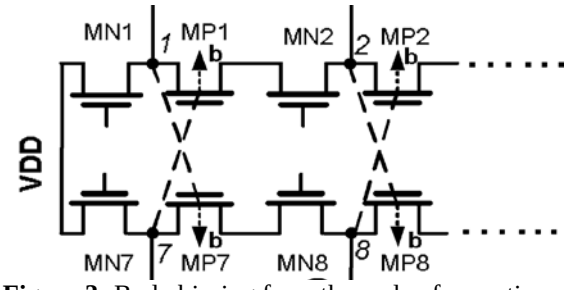

Figure 3: Body biasing from the node of operation

The clock supply and the input voltage (in milli volts) given to the first coupling of the inverter stage and then the body biasing node could be activated from the MN1 to MP7 and following to the all stages from the n-MOS to p-MOS. The second stage i.e the backward control and the reverse coupling of the MN2 from MN8 and also the MP2 from MP8. Then this node of operation can be better and improves when compared to the first node of operation. Then for the each level of stages can be amplified as per the backward control and the biasing node through the channel operation from the each number of stages.

This could be coupling and does not carry any dead zone of operation and this could be switching to the prominent to the all stages. The capacitance from the c1 of each branch carries the unit supply of the voltage from clk to clkb. Then the last stage from the n-MOS N1 and this could be coupling with the N2 and then the P1 coupling with the P2 having the amplitude switching. Then this storage from the each stages of the coupling from the node of operation can also to be calculated from the structural of the node 1 to 8. Then another node of bulk connection has been applied from the N1 to the P1 of linear stages. This could be effectively reduces the parasitic capacitance from the charge pump.

This proposed charge pump has advantages of the low power consumption based on body biasing bulk connection from the each node of operation. And also this charge pump circuit has been enabled for the lower input voltage (in milli volts) having the bulk output voltages from the clock pulses. The enabling signals that carry the circuit level of operation from the amplitude degradation of the unit supply to the needed positive up gradation from the input amplitude. This phase difference from the clock pulses into the bulk connection from the unit supply that can be varied as per the input signal.

The required connection between these signals has been proposed and implemented into the phase locked loop. This could be having the phase detector, Charge pump and the voltage controlled oscillator. The level of connection is to be a feedback signal from the VCO to the input voltage. The phase difference from the input and the feedback signals has been applied to the phase detector. Then the charge pump gives the amplification of the input voltage from the phase detector. The variations of the phase frequency has been identified and also applied for the frequency synthesizer.

The combination of the input voltage and the clock pulses that could be given into the application of the phase locked loop, modulators, servo mechanism and the digital communications. The variation cannot be finding from the amplitude and the frequency ranges of the input and the output from 50Hz to 1000MHz. These levels of frequency variation are used for the performance of the amplitude synthesizer.

A feedback charge pump circuit that uses cross-coupled NMOS switches area unit accustomed wins a high boost magnitude relation for a low-tension DRAM word-line driver. This circuit uses 2 capacitors that area unit switched in such the way that in each clock cycle, one electrical condenser is charged to the provision voltage and also the different electrical condenser is boosted to doubly the provision voltage by the clock. The two capacitors reverse roles each clock cycle, inflicting the voltage at the output to be a sq. wave that switches between VDD and 2VDD. 2 of those cross-coupled NMOS pairs area unit used on with Associate in nursing other form of charge pump and an electrical converter to form up the entire boosted voltage generator.

In, the cross-coupled NMOS charge pump introduced and that is employed to boost the speed of pipeline A/D convertor by boosting the clock drive so as to cut back the on-resistance of transmission gates within the pipeline. This work additionally utilizes a bias voltage generator to bias the n-well to double the availability voltage, preventing latch up from occurring throughout the initial startup transient. This architecture has been combined and gives the variations from the each circuit combination to the charge pump coupling into the inverter stages. That could be recognized as per the net list generation of the designing technique from the each coupling of the n-MOS and the p-MOS to the biasing node of operation units in the circuit implementation of the charge pump circuit.

4. Simulation Results

The existing Dickson charge pump circuit and the waveform (Fig 4 &5) are shown. The designing of this charge pump are designed in TANNER EDA.

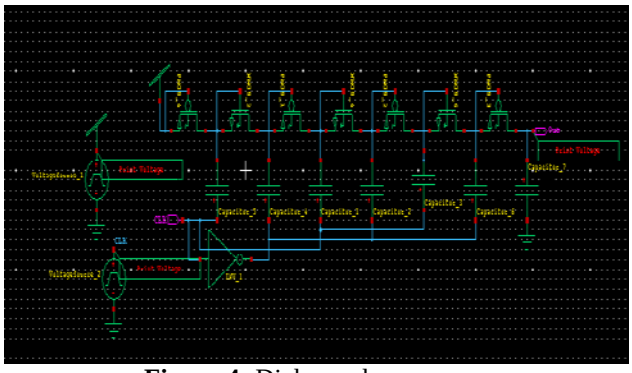

Figure 4: Dickson charge pump

The schematic diagram of proposed charge pump and the resultant output waveform is shown in the figure 6&7.

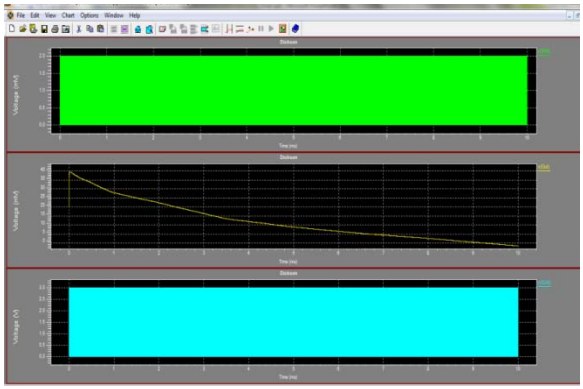

Figure 5: Waveform of Dickson charge pump

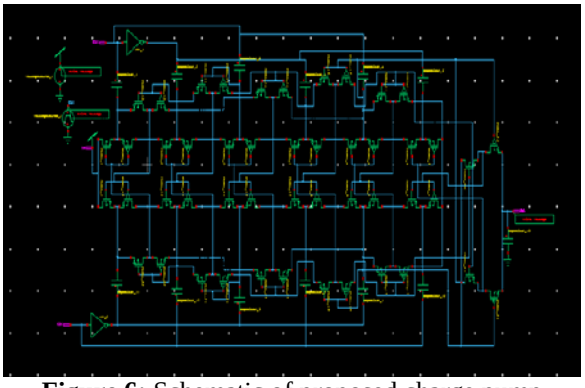

Figure 6: Schematic of proposed charge pump

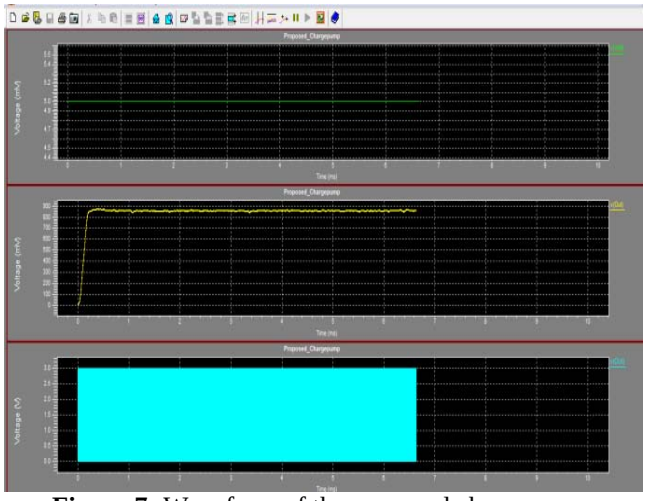

Figure 7: Waveform of the proposed charge pump

The output results of the parameter of power output voltage and the nanometer technology has been illustrated in the table-1. The consideration of this parameter has been verified and then processing of this bulk connection could be established as per the input voltage supply.

Table 1: Parameter results of the charge pump

Charge pump	*Power in watts*	*Output voltage*	*Pumping Efficiency*
Dickson charge pump	8.60 W	50 mV	56%
Wu Chang charge pump	8.04 W	20mV	42%
Linear charge pump	5.84 W	100mV	71%
Proposed charge pump	3.29 W	1000mV	83%

The results has been analyzed and verified by the parameter of the existing and the proposed charge pump. And also the capacitance of these charge pumps has been 1 pF. Then the technology of the nano meter could be used as TSMC CMOS. The operation input voltage is to be in 2mV. The variation of the output amplitude voltage could be obtained from this charge pump of the clock signal to be applied to the input source. The further variation process handled for the low area chip fabrication and for the low power consumption of this proposed charge pump circuit.

5. Conclusion

Charge pump based on body biasing and the backward control scheme has been proposed in this system. The power and the amplification could be efficient when compared to the other existing charge pump. The low output ripple and high system stability of the dual-phase charge pump circuit are demonstrated by the test chip and get better performance. Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the charge pump circuit so as to improve the power conversion efficiency. By using this efficiency calculation the pumping efficiency also calculated and gets the detailed configuration of the proposed charge pump parameter evaluation. The degradation of the amplification could be highly reduces and it could be generated as per the test identification stages proposed in the charge pump design circuit. This circuit could be further used for the implementation of the like PLL based analog devices.

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