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A Novel Current Sensor Design for Enhanced IDDQ Testing in CMOS Circuits

Yasser A. Ahmed

Department of Computer Engineering, College of Computer, Qassim University, Buraydah, Saudi Arabia
Email: *hsanien[at]qu.edu.sa*

Abstract*: This paper introduces a novel current sensor design aimed at improving IDDQ testing accuracy in modern low-power semiconductor technologies. Building on earlier measurement techniques, the proposed sensor distinguishes fault-induced currents from background leakage by analyzing their phase behavior under AC perturbation. The design enables enhanced fault discrimination while offering flexibility for integration either on-chip or off-chip. Analytical derivations and SPICE-based simulations, utilizing 0.8 µm BICMOS technology, confirm the sensor's capability to detect subtle current anomalies. These findings contribute to improved reliability in integrated circuit testing, particularly as device miniaturization amplifies leakage challenges.*

Keywords: IDDQ testing, current sensor, leakage current, fault detection, IC reliability

1. Introduction

IDDQ testing measures the quiescent supply current (IDDQ) of an integrated circuit (IC) when it is in a static, non-switching state. Compared with traditional digital functional tests, IDDQ testing offers several key advantages: it can detect physical defects, such as gate oxide shorts and bridging faults, that may not manifest in logic output errors; it requires small and simple test vectors, reducing test generation effort; and because the quiescent current of a defect-free CMOS circuit is very low, even slight increases can be detected with high confidence, offering enhanced fault coverage beyond logic testing alone. This research is significant for improving the precision of fault detection in low-power ICs, especially in the context of rising leakage currents in submicron technologies.

IDDQ tests are often faster and computationally simpler than exhaustive vector testing, as they focus only on supply current measurement without the need to observe internal nodes. The core challenge of IDDQ testing lies in accurately measuring extremely low currents amidst background leakage and process variations, especially in deep-submicron CMOS technologies where leakage currents have increased. [4], [5], [6], [7]

In this paper we introduce current monitor design based on the new approach discussed in [1][2] who introduced a measurement methodology to distinguish fault-induced current from normal leakage during IC testing, an increasingly critical issue as technology scales. This technique enhances current sensing reliability by analyzing fault vs. leakage characteristics, which is essential for accurate IDDQ testing in modern low-power processes.

2. Current Monitor

The current monitor in Figure 1 measures the phase relationship between the current signal and the introduced AC component at the power supply

The current monitor in (Fig. 1) provides a measurement of the phase of I_{GND} with respect to the introduced AC part at the power supply. This circuit detects the phase of I_{GND} by the multiplication of I_{GND} with another AC signal that has the same frequency and phase as that of the AC signal introduced at the power supply. The output of the circuit (Vol-Vo2) always has no dc component unless there is an error in the circuit. Which means the existence of a component of I_{GND} at frequency ω in-phase with the AC component of the power supply when there is faults in the circuit.

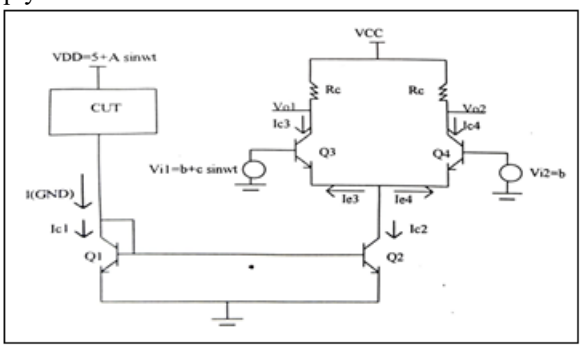

Figure 1: Current Monitor

Analysis of the Current Monitor

As shown in Fig.1, the circuit is mainly composed of two parts; current mirror and emitter coupled pair [3]

2.1 The current mirror

The emitter-coupled pair is analyzed based on the following Assumptions-

Identical transistors Q1, Q2

The collector currents of the transistors are independent of their collector-emitter voltages [3]

Since Q1 and Q2 have the same base Emitter voltage, their collector current are equal

$$Ic(Q1)=Ic(Q2) \quad (1)$$

$$I_{GND} - Ic1 - 2\frac{Ic1}{\beta f}=0 \quad (2)$$

$$\text{Thus, } Ic1=\frac{I(GND)}{1+\frac{2}{\beta f}} = Ic2 \quad (3)$$

If βf is large, Ic2 is nearly equal to I_{GND}

$$Ic2 \cong I_{GND} \quad (4)$$

Emitter Coupled Pair
The analysis of the emitter coupled pair is based on the following Assumptions-

i) Identical transistors Q3, Q4, therefor Is3=Is4 (5)
ii) Base, emitter and collector resistance's of each transistor is negligible

Output resistance of each transistor is infinite.
From Kirchhoff voltage law

$$Vi1 - Vbe3 + Vbe4 - Vi2 = 0 \quad (6)$$

From Ebers-Moll equations, assuming Vbe3, Vbe4 >> Vt

$$Vbe3=Vt \times Ln(\frac{Ic3}{Is3}) \quad (7)$$

$$Vbe4=Vt\times Ln\left(\frac{Ic4}{Is4}\right) \quad (8)$$

$$\frac{Ic3}{Ic4} = \exp\left(\frac{Vi1-Vi2}{Vt}\right) = \exp\left(\frac{Vid}{Vt}\right) \quad (9)$$

Where Vid = Vi1 –Vi2
The node eq. at the emitter of the transistors is given by

$$-(Ie3+Ie4) = I_{GND}= \frac{Ic3+Ic4}{\alpha f} \quad (10)$$

$$Ic3=\frac{\alpha f \times I(GND)}{1+exp\frac{-Vid}{Vt}} \quad (11)$$

$$Ic4=\frac{\alpha f \times I(GND)}{1+exp\frac{Vid}{Vt}} \quad (12)$$

$$Vo1 = VCC-Ic3\times Rc \quad (13)$$

$$Vo2 = VCC-Ic4\times Rc \quad (14)$$

$$Vod=Vo1-Vo2= \alpha f \times I_{GND} \times Rc \times \tan\left(\frac{-Vid}{2Vt}\right) \quad (15)$$

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for Vid<< 2Vt we get a linear relation:

$$Vod= \alpha f \times I_{GND} \times Rc \times \left(\frac{-Vid}{2Vt}\right) \quad (16)$$

As such Vod is proportional to the multiplication of Vid and I_{GND}

3. Simulation Results

We illustrate the Spice simulation results of the current sensor connected with the circuit under test (as shown in Figure 2) using. 0.8 µ BICMOS technology

We assume that VDD=5+sin ($2\pi\times100$ x 10^6 t) (17)
The inputs of the differential pair are given by
.Vil= 1.5 +0.01sin($2\pi\times100\times10^6$ t), Vi2=1.5
i.e. Vid= 0.01 V<<2Vt (18)
Vi2=b

The size of NMOS and PMOS transistors are 2λ × 2λ (minimum size).

The fault is modeled as a 100-ohm resistor between the drain and source of M2 between the drain and the source of M2.

The following symbols are used in the simulation results:-
V(vin) is the input of the inverter Vin.
V(1) is the output of the inverter V_{out}
(V_{o1} -V_{o2}) is the output of the emitter coupled pair

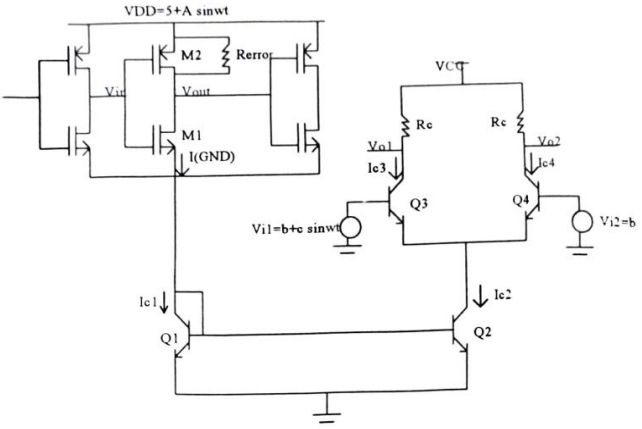

Figure 2: Current monitor is connected with three inverters

The following figure 3 illustrates the dc part in the Fourier transform of the output of different values of Rerror. The dc remains constant in the part where the transistor m1 in the saturation region. After that (when m1 is in linear region), the greater Rerror, the small the dc value will be.

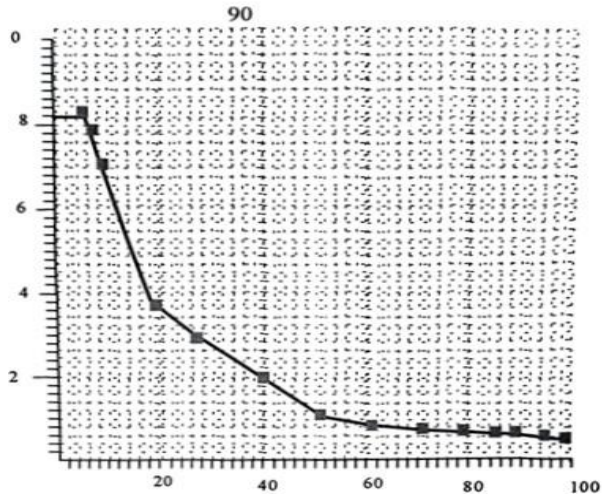

Figure 3: DC of Fourier transform of Vo for different values of Rerror

4. Conclusion

This study presents an innovative current sensor architecture based on methodologies from reference [2] and designed to improve the discrimination between fault-induced and

leakage currents during IC testing. The proposed sensor enhances measurement accuracy by analyzing the unique characteristics of these currents, which is vital for effective IDDQ testing in advanced low-power semiconductor technologies. Analytical evaluations and SPICE simulations validate the sensor's functionality, indicating its potential for implementation either on-chip or off-chip. The results demonstrate that this approach offers a significant advancement in fault detection capabilities within modern IC testing frameworks. Future research may explore sensor optimization for smaller process nodes or higher frequency ranges.

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Author Profile

Yasser Ahmed received the B.S. and M.S. degrees in Electrical Engineering from Cairo University 1993 and 1996, respectively. He received his Ph.D. from Renne1 University, France 2002.