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Planar Magnetics for Space Applications

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Abstract: ***The ever increasing demand of miniaturization of DC-DC converters expects for the converters to be designed for higher frequency of operation with better efficiency. The recent developments in high frequency power switches and evolved technologies in magnetic design such as planar magnetics helps to achieve small size and cost effective DC-DC converters and their subsequent usage in space applications. In spacecraft level; the parameters like size, weight and cost of all the hardware plays a vital role. In such applications these low profile, high power density and efficient planar transformers in DC-DC converters realization will have a significant improvement in overall performance. This work deals with tuning free multiple tap planer transformers which enables us to have a broader range of output voltages for the designed configuration. It is highly reproducible with a better regulation, efficiency and less ripple content compared to the existing conventional transformer based DC-DC converters. The salient features of this work are mentioned below.***

Salient Features: Low profile, Tuning free magnetic, Improved output regulation, High frequency of operation and improved efficiency, Lower ripple, Multiple outputs

1. Introduction – Planar Magnetic Technology

In case of a conventional wire wound magnetic components, the skin and proximity effects results in higher power losses and poor regulation particularly at frequencies above 100 kHz.The overall design goal for a dc-dc converter is to reduce the impact of heat and noise while achieving low output impedance, excellent dynamic response, a low cost and minimal size[1]. In such case, Planar Magnetics technology stands as the better alternative solution for the existing dc-dc converters for satellite applications. The two major parameters that made planar technology much more feasible are:

a) Power MOSFETs with increased switching frequency enabled to reduce the turns
b) Ferrite core which can be moulded and machined into almost any shape.

Planar magnetics are much advantageous compared to the conventional magnetic devices for which the demand of these devices increasing rapidly. Miniaturization with better efficiency is the key to opt this technology. Here are the major advantages of planar magnetic devices along with its limitation.

a) Advantages of Planar Technology:

When compared to a conventional wire wound, the planar magnetic component technology has several advantages.

- Low height
- Well suited for the development of high pulsed power converters
- Low leakage inductance
- High density power
- Repeatability values of parasitic parameters
- Excellent temperature characteristics

Planar Transformer has all the above advantages with a major limitation of having very high parasitic capacitance due to the large overlapping area and the small distance between consecutive layers. These parasitic capacitances can severely affect the performance of power converters and ***limit the application of PTs in high frequencies***. The method to reduce the effect of this limitation is also addressed in this work.

2. Planar Magnetics Design

The total power loss in magnetic devices usually consists of core loss in magnetic materials and copper loss in windings. The core loss has two portions, which are hysteresis loss and eddy current loss while the copper loss is often explained by DC or AC power loss dissipated in the windings in the form of heat[3].

a) Core Power loss Calculation:

The core and copper losses in a transformer under operating conditions will induce a temperature rise. This rise must stay below a maximum allowable value to avoid damage to the transformer or the rest of the circuitry. In thermal equilibrium the total losses in the transformer (P_{loss}), can be related to a temperature rise ΔT of the transformer by:

$$P_{loss} = \frac{\Delta T}{R_{th}} \quad \ldots\ldots (1)$$

R_{th} - Thermal resistance of the transformer (in ^{o}C/W)

The value of thermal resistance ($\mathbf{R_{th}}$) of a transformer directly to the value of the effective magnetic volume $\mathbf{V_e}$ of the ferrite core used. This empirical formula is valid for wire wound transformers with core shapes like RM and ETD. A similar relation has now been found for planar E transformers.With the assumption that half of the total transformer loss is core loss, the core loss can be expressed interms of volume of the core and temperature rise as:

$$P_{core\_loss} = \frac{12.\Delta T}{\sqrt{V_e}} [\text{mW/cm}^3] \quad \ldots.(2)$$

b) Calculation of Maximum Flux Density:

Power losses in ferrite cores have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (Tin° C). Core loss density can be approximated by the following formula:

$$P_{core\_loss} = C_m f^x B_{max}^y C_T \quad \ldots(3)$$

Where $C_T = Ct_o - Ct_1 T + Ct_2 T^2$

The parameters (fit parameters) in the above equation can be found by curve fitting equation of measured power loss data which is available in the manufacture's data sheet of core materials. These parameters vary depending on the type of the ferrite material that is being used.

After calculating maximum P_{core_loss} from eqn.4;the maximum allowed flux density B_{max} can now be calculated by rewriting equation [3]:

$$B_{max} = \left[\frac{P_{core\_loss}}{C_m C_T f^x}\right]^{\frac{1}{y}} \quad \ldots(4)$$

Due to the limited available winding space, it is recommended to use the maximum allowed flux densities in planar magnetics. The B_{max} value can be confirmed using the core loss curves of the selected core which is a plot of core loss versusB_{max} at different operating frequency ranges.

c) Planar Magnetics Design: Transformer

The calculation of B_{max} using the obtained power loss is clearly mentioned in the before section. To obtain the power loss the R_{th} parameter needs to be calculated [2]. Using that the number of primary turns can be determined as per the below steps:

(1) Determining the Coefficient of Thermal Resistivity:

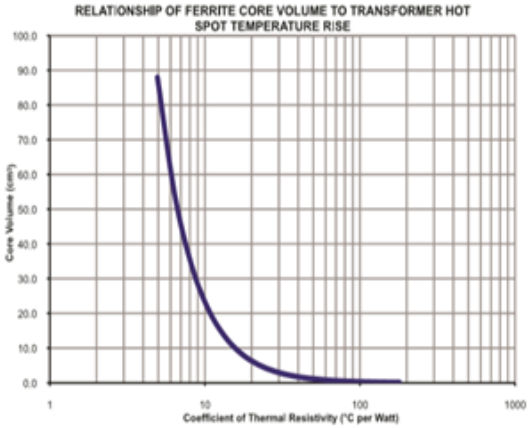

Figure 1: Coeff. Of thermal resistivity

The coefficient of thermal resistivity for an electronic device is the temperature rise per unit of loss, expressed in °C per W. A simpler way of expressing this relation requires only the core volume, and this parameter is widely available in all the core manufacturer's data sheets.

Ferroxcube conducted an empirical study comparing the hot spot temperature rise of many different cores and bobbin geometries to the total core and winding losses. The data of *volume* versus*coefficient of thermal resistivity* has been fit into a curve as shown in the fig.1.

The equation for the same curve can be written as:

$$R_{th} = 53 \times V_e^{-0.53} \text{ (°C/W)} \quad \ldots(5)$$

(2) Total transformer losses can be determined from R_{th} using eqn. [1].

(3) After the total loss calculation, by assuming that the core losses are half of that of total loss, core loss density can be calculated.

$$P_{core\_loss} = \frac{P_{loss}}{2V_e} (\text{mW/cm}^3) \quad \ldots(6)$$

(4) Once the core loss density is known, from the curves of "Specific power loss as a function of flux density with frequency as a parameter,B_{max} can be easily determined.

(5) Finally the no. of primary turns can be calculated using the below equation:

$$N_p = \frac{V_{in\,(min)} \times D_{max} \times 10^4}{B_m \times A_e (cm^2) \times f_{sw}\,(Hz)} \quad \ldots..(7)$$

The secondary side turns can be calculated using turns ratio, which includes line volt drop (V_{LD}) and diode drop (V_D) as:

$$T_{ratio,i} = \frac{(V_{out})_i + (V_{LD})_i + V_D \times D_{max}}{D_{max} \times V_{in\,(min)}} \quad \ldots. \text{Eqn. [10]}$$

i – 1 to k; where k is the number of secondary windings
From this, the secondary turns are calculated as:

$$(N_s)_i = T_{ratio,i} \times N_p$$

In the assembled planar transformer, every primary turn is at a precise location, governed by the PC board. The primary is always the same distance from the secondary. This provides a tight control over the primary to secondary leakage inductance resulting in the low leakage inductance of planar transformer.

d) Planar Magnetics Design: Coupled Inductor

The planar coupled inductor can be calculated similar to the conventional coupled inductor. The design calculation goes as follows:

(1) Assuming,

$$V_{in(max)} * D_{min} = V_{in(min)} * D_{max}$$

For the known values of input voltage range and the assumed value of D_{max} ; D_{min} can be calculated and from that $T_{OFF(max)}$ is obtained.

$$T_{OFF(max)} = (1 - D_{min}) * T$$

(2) The total magnetizing inductance can be calculated by assuming that the whole load current is flowing in the line with higher output current and taking ΔI = 20% of full load current.

$$L_m = E * \frac{\Delta t}{\Delta I}$$

Here Δt is$T_{OFF(max)}$.

(3) To select the planar inductor core, the energy LmI2 is calculated and the core of little higher energy is chosen than calculated from the standard data. This energy (mJ) versus A_L (mH/1000T) for different planar cores by *Magnetic Inc.* is helpful in determining the core of requirement. The

number of turns in the highly current carrying line is calculated using the below formula:

$$N = \sqrt{\frac{L_m}{L_{1000}}} \times 10^3$$

The ampere-turns will be constant till certain limit after which it starts reducing resulting in the reduction of the inductor value. This is called as maximum allowable DC bias (in AT) beyond which the inductance drops rapidly. For that the field strength (in oersted) is calculated as:

$$H = \frac{0.4 * \pi * N * I}{l_e}$$

The final number of turns can be calculated by considering the constant from H-μ Roll off curve.

$$N_{final} = \frac{N}{\%\ of\ \mu\ roll\ off}$$

The remaining outputs inductor's turns will follow the voltage proportionality.

e) Track parameters calculation for the available winding width

Windings should be divided over the available layers in such a way that the outer layers are symmetric with respect to the turns in the inner layers for symmetrical thermal expansion. Sandwiching of primary and secondary layers also helps to reduce the proximity effect. From the below figure, the track length in the available winding width can be calculated as shown:

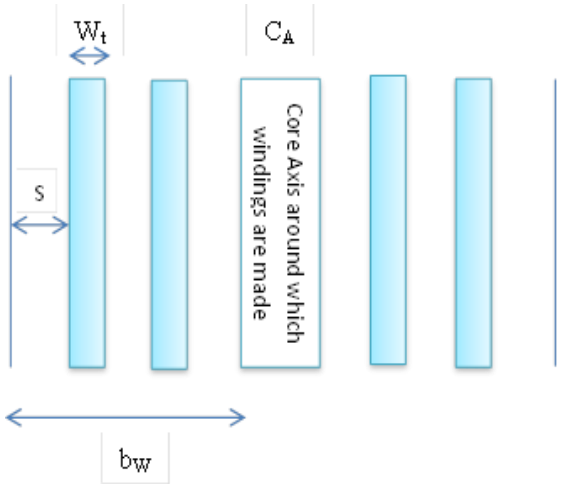

Figure 2: Track Width W_t calculation

Assume no. of turns per layer are – 'N'Spacing between turns-'s'. For an available winding width of b_W, the track width (W_t) can be calculated as:

$$W_t = \frac{b_W - (N+1)s}{N}$$

The track width of a winding depends on the value of current and the maximum current density allowed. The spacing between the turns is governed by the production capabilities and cost. Safety standards like IEC 950 require a distance of 400μm through PCB material (FR2 or FR4) for mains insulation between primary and secondary windings. If mains insulation is not required a distance of 200μm between the winding layers is sufficient.

f) Parasitic effect in Planar Transformer:

Planar transformers (PTs) have several advantages over the traditional wire-wound transformers that make them very desirable for the high-power density applications. In spite its key features, the proximity of layers on PCB causes planar transformers to have much higher parasitic capacitance. The parasitic capacitances have severe effects on the performance of power converters, especially in high frequency applications. The parasitic capacitances in the transformer can be classified into two groups.

(i) Intra-winding capacitance:

The large *intra-winding capacitance* gives rise to a high charging current at the transformer input, resulting in a loss of overall efficiency.In addition, this capacitor distorts the transformer voltage of power converters in light-loading condition resulting in poor regulation. The output voltage cannot be regulated by sweeping the frequency at light loading; therefore, this parasitic capacitance should be minimized in order to operate with a wide voltage.

(ii) Inter-winding capacitance:

On the other hand, the large *inter-winding capacitance* produces significant displacement currents that contribute to EMI problems.The total size and cost of the filter depends on the noise amplitudes in the circuit. Reducing the inter-winding capacitance significantly attenuates the common mode (CM) noise which simplifies the filter design and reduces the total filter size.

g) Methods to reduce effective parasitic values in planar transformer[4]

Considering an equivalent model of two-winding planar transformer (PT) as shown in Fig.3, where R_p and R_s are the resistances of the primary and secondary windings. C_{po}, C_{so} and C_{pso} are used to account for the self-capacitances of the primary and the secondary windings and the mutual capacitance between the two windings, respectively. It is desirable to keep C_{pso} as small as possible, and good EMI results could be achieved. The equivalent capacitors referred to the primary side can be determined approximately by the following relations.

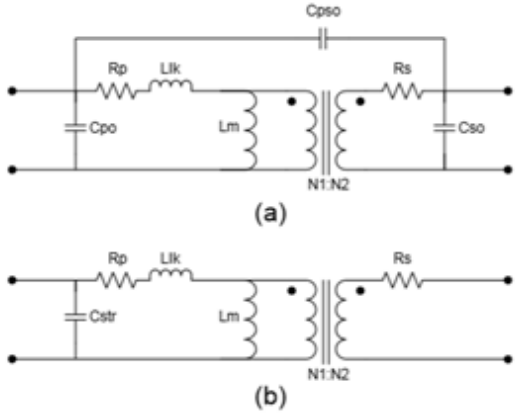

Figure 3: Transformer equivalent circuit (a) with self and mutual capacitances (b) with total stray capacitance referred to primary side

$$C_p = C_{po} + (1-k).C_{pso}$$
$$C_s = k^2.C_{so} - k(k-1).C_{pso}$$
$$C_{str} = C_p + C_s$$

where k is the turns ratio. The mutual capacitance C_{pso} due to the electrical coupling between the primary and the secondary windings can be approximately measured directly by shorting both primary and secondary sides. The single equivalent capacitance referred to the primary side, C_{str}.

In the case of PTs, static layer capacitances can be estimated easily since the windings consist of parallel and flat conductors.

$$C_o = \varepsilon_r.\varepsilon_o.\frac{S}{h_\Delta}$$

S represents the overlapping surface area of the two plates. The distance between the plates is h_Δ.

There are different ways to reduce the value of parasitic capacitance between overlapping traces of a PCB. The first approach is minimizing the overlapping between traces of top and bottom side. Though thismethod significantly reduces the value of parasitic capacitance, avoiding overlapping requires only 50% utilization of PCB and therefore, the DC resistance roughly increases two times.

(i) Reduction of intra-winding capacitance:Apart from reducing the over lapping area between the traces of top and bottom layers of PCB, the other method in minimizing the value of intra-winding capacitance is through reducing the voltage gradient between overlapping turns.Instead of having top and bottom turns in series, the top and bottom traces could be connected in parallel[5]. The rest of the turns are duplicated on both sides of another PCB and are connected to the first PCB through a middle connectionmaking the voltage gradient between overlapping traces zero.

(ii) Reduction of inter-winding capacitance:The value of inter-winding capacitance is proportional to the number of intersections between primary and secondary, the overlapping area, the distance between layers and the permeability of the material between primary and secondary layers. Increasing the distance between primary and secondary windings also is not a wise way of reducing the inter-winding capacitance as larger separation means less space for copper and consequently, higher DC resistance. Therefore, among all influential factors, only the number of intersections and the permeability of the material in the intersections of primary and secondary can be manipulated to reduce the value of inter-winding capacitance, without compromising the resistance.

3. Planar Magnetics Design Example - 50W DC-DC Converter

This section deals with the design calculations of planar transformer and planar inductor along with track width for a 50W DC-DC converter with the specifications as mentioned below. This adds much benefit in terms of space, cost and output regulation to the existing conventional magnetics based DC-DC converters. The specifications of this particular design example are considered based on the existing requirement of converters in the space applications.

Specifications:

Parameter	Range
Input Voltage	26-43V
Output-1 Output-2 Output-3	9V/4.5A 15V/0.5A 12.5V/0.05A
Topology	Forward Topology
Frequency of operation	200kHz
Duty Cycle (max)	0.4
Efficiency	80%
Ripple	50mV
Line regulation	±1%
Load regulation	±1%

Here 12.5V output line used as feedback to maintain the stability of DC-DC converter during load and line transients etc.

A. Planar Transformer Design data:Core chosen is*E22/6/16/R-3F3 (E/PLT combination)*

'E' represents the core shape whereas 3F3 indicates the core/grade material with permeability (μ) of 2000.This particular core is used in power transformers, power inductors and general purposetransformers and inductors in a frequency range of 0.2MHz to 0.5MHz.

Note: *The core selection of the planar transformer for the assumed specifications is selected based on the core data, frequency of operation, core loss density and the maximum flux density. One of the parameters is assumed to calculate the other parameters and the designed values are cross verified to ensure that all those values are fit into the requirements. In this way, the selected core is "Planar E Core – E22/6/16R-3F3".*

Now, as per the design steps mentioned above; for ΔT=40ºC & f=200 kHz; the maximum flux density was observed from the loss curves as:

$$\mathbf{B_{max} = 0.1T}$$

For a duty cycle of D_{max}=0.4, the primary turns are calculated as follows:

Output (Transformer)	No. of turns
Primary	7T
9V/4.5A	7T
15V/0.5A	11T
12.5V/0.05A	10T

Note: Maximum core power loss for the selected core is calculated using eqn.2 & eqn.3 where both the equations had given approximately same values.

B. Coupled Inductor Design data: As per the procedure mentioned above for the design of coupled inductor, the magnetizing inductance is calculated and the respective energy is 1.228mJ. This energy when mapped in the below graph (Fig.4), the corresponding planar E-core is observed as CP42216 (EI type) with an AL value of

400mH/1000turns. Here 'C' denotes the shape code of the core which means that 'planar core with clip recesses'.

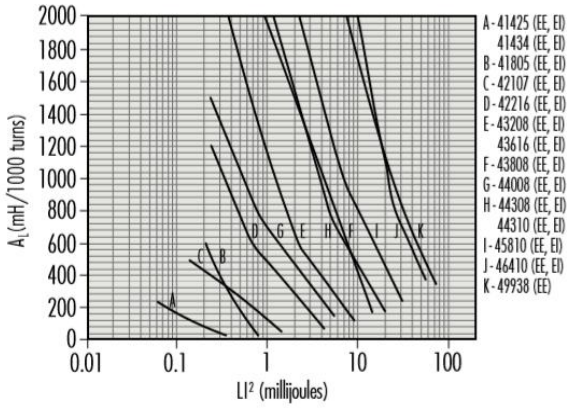

Figure 4: Inductor Core Selection graph

From thecore data, the no. of turns is calculated as follows:

Output (Inductor)	No. of turns
9V/4.5A	10T
15V/0.5A	17T
12.5V/0.05A	14T

4. Conclusion

A novel design methodology of planar magnetics is implemented in the design of DC-DC converter realization for space applications. Improper regulation, high surge currents in DC-DC converters of satellite application leads to reduced performance which affects the EMI compliance in a spacecraft. Hence it demands for more reliable system with less ripple and good regulation.The detailed study was done on the choice of the planar cores where the core losses are within the range for a particular operating frequency and maximum magnetic field density.The study of effects the higher parasitic capacitance in planar transformer has been completed along with its reduction techniques. The study of determining the track width, the number of PCB layers and insulation thickness with the designed data was completed. To establish the methodology of planar transformer/inductor design, a typical 50W DC-DC converter for satellite application had been considered.

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