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Implementation and Comparison of Tree Multiplier using Different Circuit Techniques

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Abstract: ***Multiplication is an important fundamental function in arithmetic operations and is used in various applications. The Tree multiplier is a high speed parallel multiplier used for large size operands.*** **In** ***this paper 4x4 Tree multiplier is implemented with CMOS logic, CPL logic and DPL logic technique and various performance parameters such as power, delay and transistor count of Tree Multiplier using different circuit techniques are discussed and compared. Different types of circuit techniques have a unique pattern of structure to improve their performance in various means like low power, minimal delay and decreased PDP. All the circuits are designed and simulated using 90nm technology, 2.5V supply Also layouts of all the basic circuits(AND2 and Full Adder) using CMOS logic, CPL logic and DPL logic are designed and the layout of the Tree multiplier using CMOS logic is designed and verified by its corresponding waveform.***

Keywords: Full adder, AND gate, Tree Multiplier, 3:2 compressor, CMOS, CPL, DPL

1. Introduction

Tree Multiplier was proposed by C.S. Wallace. Tree Multiplier can handle the multiplication process for large operands which is achieved by minimizing the no of partial product bits in a fast and efficient way by means of a CSA tree constructed from 1-bit full adders. Thus the main advantage of tree multipliers is its increased speed of operation.

2. Architecture of Tree Multiplier

In Tree multiplier [1][2][3], the partial products sum adders are arranged in a treelike fashion which reduces both the critical path and the number of adder cells required. In the Tree Multiplier number of adder cells and the depth of the tree is reduced. It uses 1-bit adder as 3:2 compressor, which takes three inputs and produces two outputs. A 1-bit full adder is a "ones counter" that counts the number of 1's on the A, B, C inputs and encodes them on the sum and carry outputs. In Tree Multiplier , the addition of partial products in a column of an array is equivalent to the number of 1's in that column with the carry being passed to the next column to the left. Tree multiplier as in figure 1 enumerates the adders required in a multiplier based on 3:2 compression method. The adders are arranged vertically into ranks according to the time at which the adder output becomes available. In the Tree multiplier architecture ,there is an "array" part and a CPA part at last stage (a ripple carry adder circuit).The total propagation time of Tree Mutiplier is the sum of final CPA time and the propagation time of the array. The delay through the array part is propotional to $\log_{3/2}n$, where n is the width of the tree. Its high speed of operation is due 1-bit adders used as 3:2 compressors which avoids carry propagation. There is substantial reduction in hardware for large tree multipliers.The main disadvantage of tree multiplier is that its architecture exhibits irregularities in the layout because of relatively complicated interconnection scheme.

Table 1: 1-bit full adder as 1's counter [3]

ABC	*CS*	*No of 1's*
000	00	0
001	10	1
010	10	1
011	01	2
100	01	1
101	10	2
110	10	2
111	11	3

Multiplication process for Tree Multiplier involves generating of the partial products then a set of counters reduces the partial product matrix without propagating the carries. This result in a matrix is composed of the sums and carries of the counters. Another set of counters then reduces this matrix and the whole process continues until a two row matrix is generated. Finally the two rows get summed up with a final adder, by a carry propagate adder at the last stage.

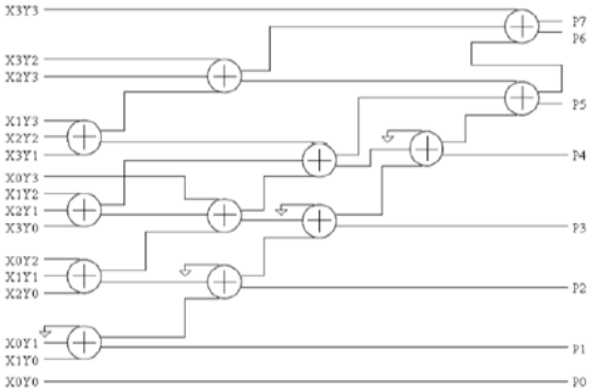

Figure 1: 4 x 4 tree multiplier [2]

3. Schematics & Layouts

Tree Multiplier uses AND gates and Full Adders as its subcomponents. To realize Tree multiplier using different logic styles[3][4][5][6] its subcomponents are designed using CMOS,CPL and DPL logic styles .These logic styles vary in structure and have their advantages and disadvantages and

thus provides different values of performance parameters. CMOS uses an NMOS pull-down and a dual PMOS pull-up logic network to realize any logic function. CMOS logic style is robust; its layout is straightforward and efficient. Disadvantages of complementary CMOS are the substantial number of large PMOS transistors, resulting in high input loads and relatively weak output driving capability due to series transistors in the output stage.

CPL is pass transistor logic. A CPL gate consists of two NMOS logic networks (one for each signal rail), two small pull-up PMOS transistors for swing restoration, and two output inverters for the complementary output signals. The advantages of the CPL style are the small input loads, the efficient XOR and multiplexer gate implementations, the good output driving capability due to the output inverters, and the fast differential stage due to the cross-coupled PMOS pull-up transistors. This differential stage, on the other hand, leads to considerably larger short-circuit currents. Other disadvantages of CPL are the substantial number of nodes and high wiring overhead due to the dual-rail signals and the inefficient realization of simple gates (i.e., high transistor count, two signal inversion levels).

DPL logic is used to avoid problems of reduced noise margins in CPL. In DPL twin PMOS transistor branches are added to N-tree. Its full swing operation improves circuit performance at reduced supply voltage with limited threshold voltage scaling. Balance in DPL circuits reduces data dependent delay.

3.1 AND GATE

In Tree multiplier AND gate is used to produce partial products. For implementing Tree multiplier using different circuit techniques AND gates using CMOS logic, CPL logic and DPL logic along with their layouts are as shown in figure 2,3 and 4.

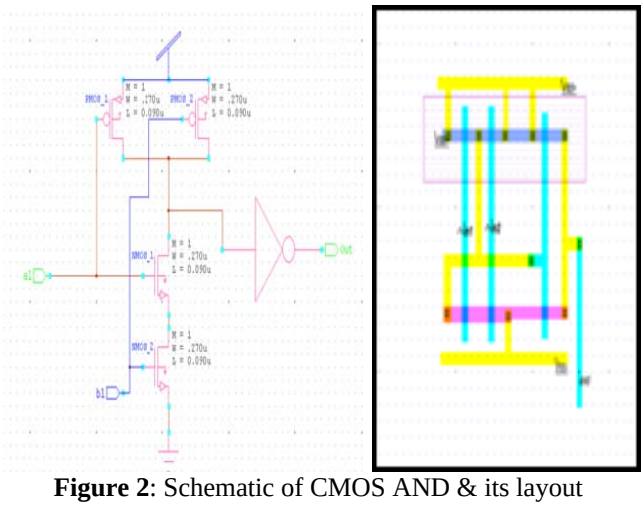

Figure 2: Schematic of CMOS AND & its layout

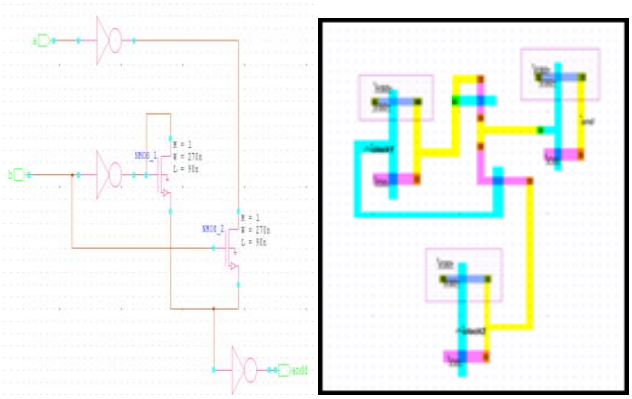

Figure 3: Schematic of CPL AND & its layout

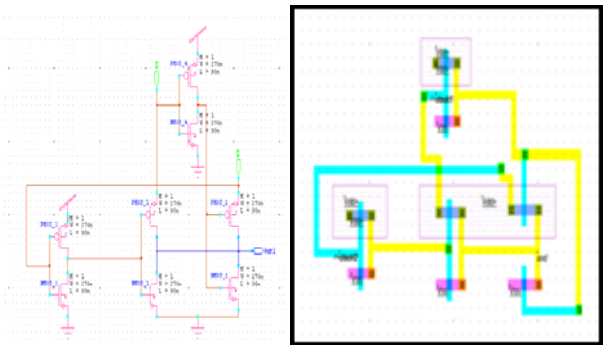

Figure 4: Schematic of DPL AND & its layout

3.2 FULL ADDER

In Tree multiplier 1-bit full adder is used as 3:2 counter. For implementing Tree multiplier using different circuit techniques 1-bit full adder using CMOS logic, CPL logic and DPL logic along with their layouts are as shown in figure 5,6 and 7

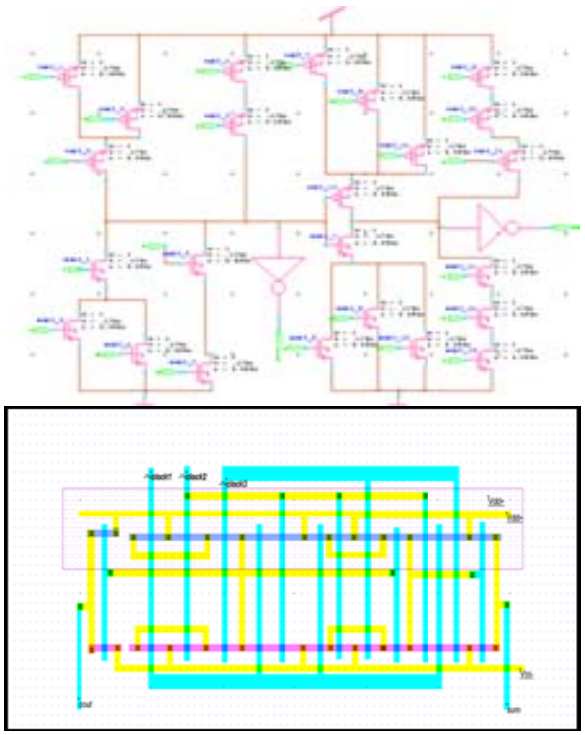

Figure 5: Schematic of CMOS 1-bit full adder and its layout

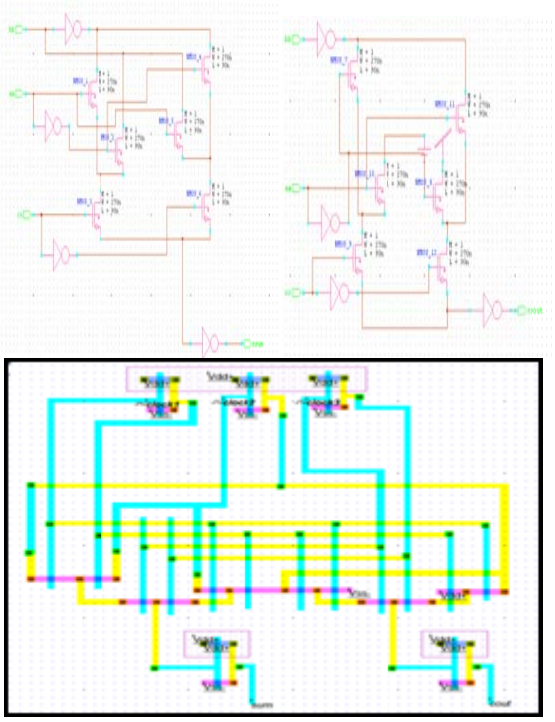

Figure 6: Schematic of CPL 1-bit full adder and its layout

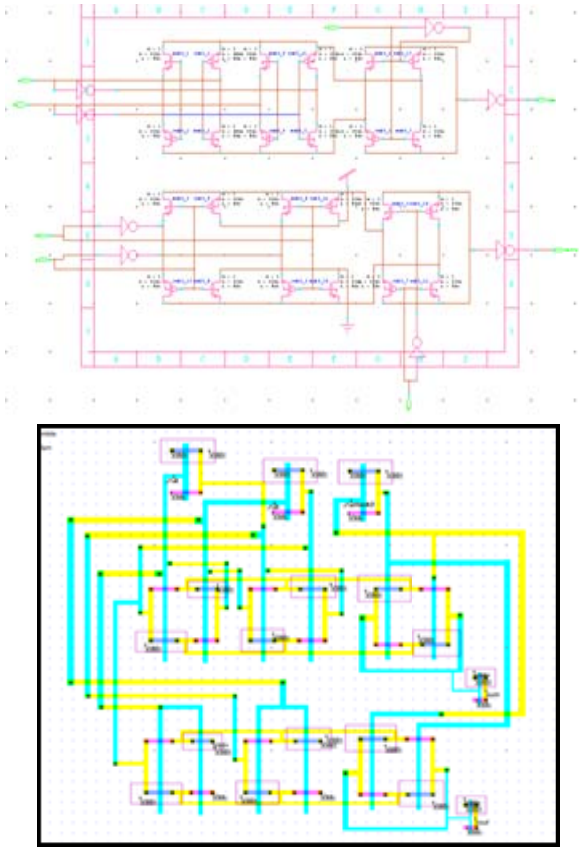

Figure 7: Schematic of DPL 1-bit full adder and its layout

3.3 Tree Multiplier

The gate level schematic of the Tree Multiplier is shown in Figure 8. The input waveform for the transient analysis of Tree Multiplier and transient response of the Tree Multiplier is shown in Figure 9. Layout of Tree multiplier using CMOS logic and its post layout simulation obtained is as shown in figure 10

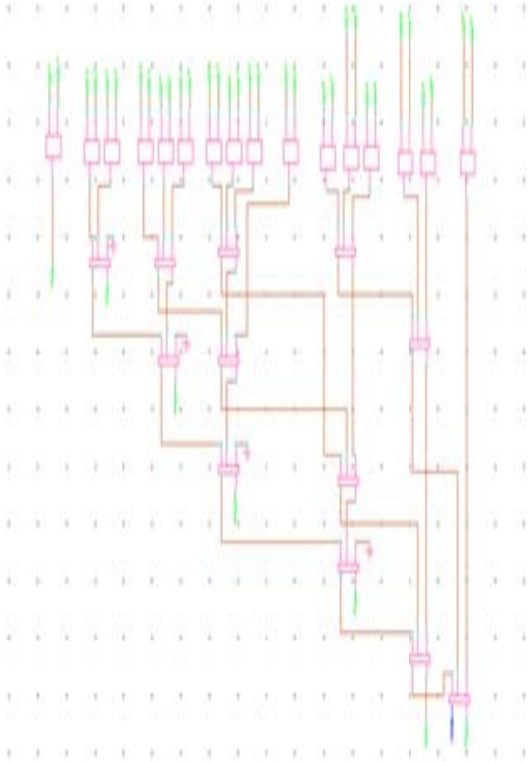

Figure 8: Schematic of Tree Multiplier

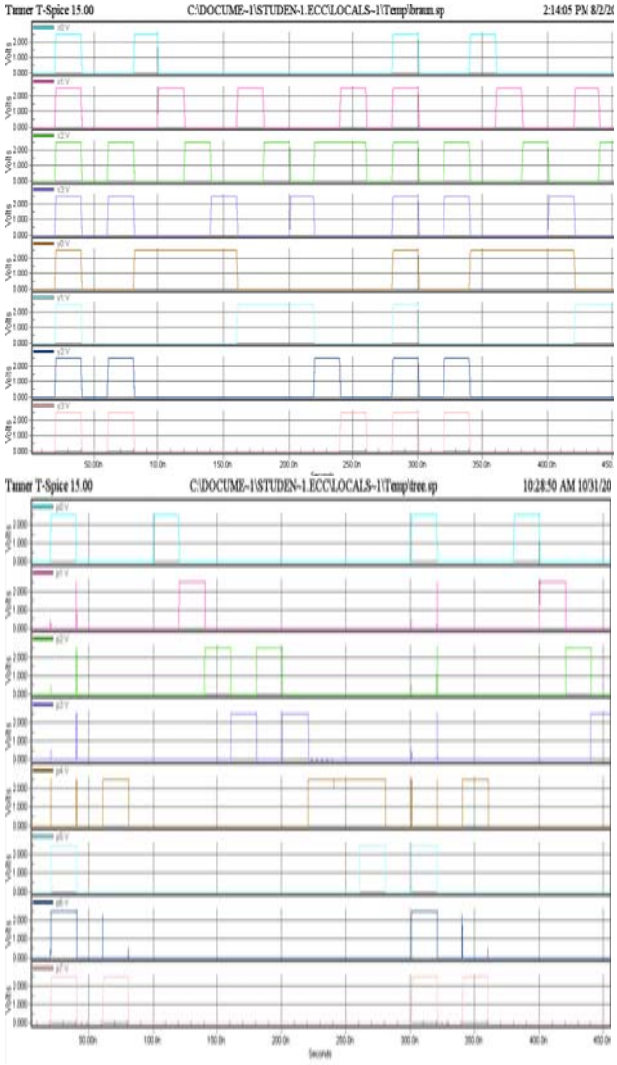

Figure 9: Input and output waveform of Tree Multiplier

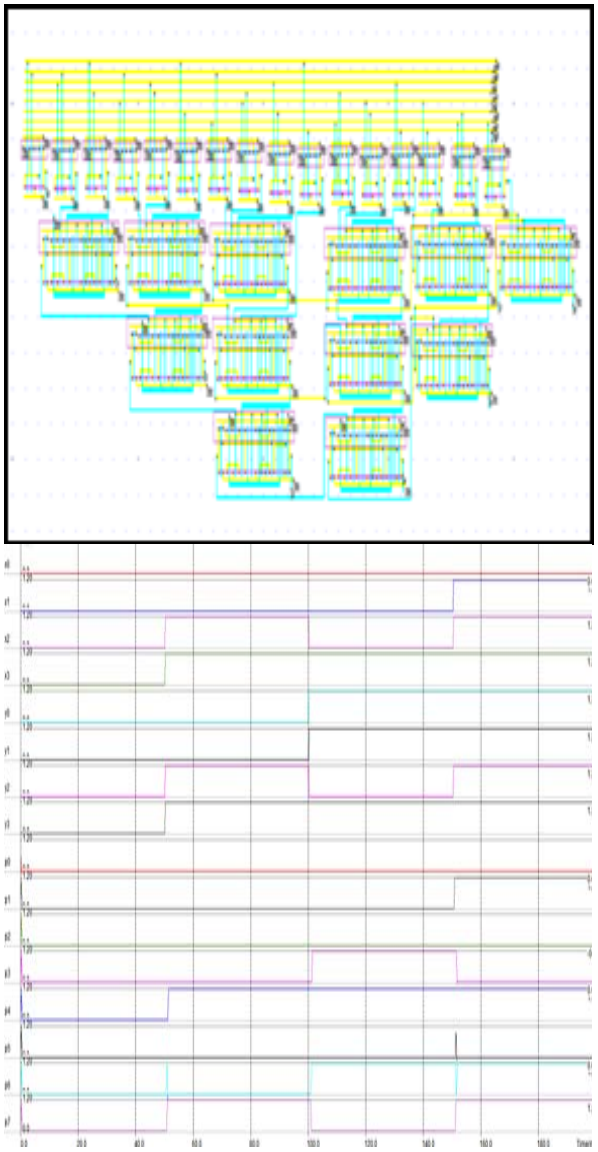

Figure 5.10: Layout of Tree Multiplier and its post layout waveform

4. Power & Delay Analysis

Table II shows the comparison results for Tree Multiplier using different logic styles at 90 nm technology and supply voltage of 2.5v. The table shows the average power consumed, the propagation delay and overall PDP of Tree Multiplier in different logic styles. The results are obtained with load capacitance of 100fF. The maximum power is consumed by CPL Tree Multiplier and minimum power is consumed by CMOS Tree Multiplier. Whereas minimum delay is obtained for DPL Tree Multiplier and maximum delay for CPL Tree Multiplier.

Table 2: 1-bit Comparison of Tree Multiplier using different circuit techniques

Logic Style	*Power Consumed(in µw)*	*Propagation Delay(in ps)*	*PDP ($x10^{-15}$watt sec)*	*Transistor Count*
CMOS	109.137	596.0548	65.051	432
CPL	202.813	623.7514	126.504	464
DPL	149.880	541.6173	81.177	608

5. Conclusion & Future Scope

The overall performance of the Tree Multiplier is compared on the basis of average power consumed , propagation delay, PDP and number of transistors using CMOS logic, CPL logic and DPL logic . Tree Multiplier uses AND gates and Full Adders as its subcomponents. For Tree Multiplier, the DPL logic uses maximum number of transistors and CMOS uses minimum number of transistors. The minimum power is consumed by CMOS logic and minimum propagation delay is found out for DPL logic. CMOS logic has the minimum PDP value. As it can be concluded from above discussion that minimum delay is exhibited by DPL logic but with maximum number of transistor count. The CMOS logic provides the best PDP for Tree Multiplier with minimum power consumption. As Tree multiplier is a fast multiplier used for large operands, high order tree multiplier can be implemented using other methods for different performance parameters and also layouts of Tree Multiplier architectures for CPL and DPL logic can be designed.

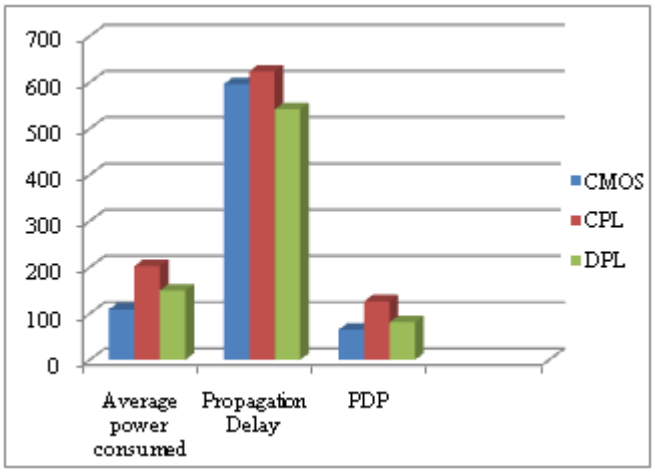

Figure 14: comparison of the Tree multiplier using different logic styles

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