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LDPC Minimum Sum Algorithm Decoder with Weight (3, 6) Regular Parity Check Matrix: A Review

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Abstract: ***Low-Density parity-check (LDPC) codes are unit one in every of the foremost powerful error correcting codes obtainable nowadays. Their Shannon capability approaching performance and lower cryptography quality have created them the simplest choice for several wired and wireless applications. This paper offers a review on the one of the best technique for error detection and correction. The paper includes all the previous work related to the LDPC codes.***

Keywords: LDPC, Decoder, Min-sum Algorithm, FPGA

1. Introduction

Low-density parity-check (LDPC) codes are a class of iteratively decoded error-control codes which have attracted much attention in recent years due to their excellent performance and parallelizable decoder architectures. These two peculiarities have significantly contributed to make LDPC codes among one of the most promising candidates for next generation data communication and storage systems, such as IEEE 802.16e, DVB-S.2 and 3GPP LTE, etc. In general, LDPC codes are decoded by the belief

propagation (BP) algorithm. Theoretically speaking, the BP algorithm will converge to a posteriori probability for variable nodes if the Tanner graph (TG) of each code is cycle-free. Unfortunately, the messages passed through the edges of the graph in the BP algorithm are statistically dependent, due to the existence of short cycles in the TG. So there is no guarantee that the BP algorithm is optimal for short and moderate block lengths. Additionally, the hardware implementation of the BP algorithm is limited by high computational complexity.

Shannon orchestrated the mathematical theories of communications in 1948, conflicted that the system capacity C of a channel flustered by additive white Gaussian noise (AWGN) may be a operate of the received signal power S, the noise power N, and withal the receiver bandwidth W. it's attainable to send data at the rate R, where RЈbC, through the channel with Associate in Nursing arbitrarily minuscule error likelihood by employing a sufficiently arduous committal to indicting theme. In 1962, Gallager orchestrated LDPC that may be a linear block codes, and endeavored that the info transmission rate of LDPC code will approach the technologist capability. The communications system devised during this work. Random range signal inputs are encoded mistreatment the approximate lower Triangular LDPC encoder, modulated by the binary section shift keying (BPSK) modulator, and sent to the receptor through the AWGN channel. Once the modulated signals are demodulated by the BPSK rectifier, the MSA rewriter is employed to decode the signals. Current LDPC secret inciting strategies are derived from the Sum-Product Algorithm (SPA). However, the SPA requires elongated multipliers throughout secret inciting, thereby elevating the issue of hardware implementation. Resultant students have utilized concepts within the exponent domain to transmute the multiplication equation of the SPA into a index equation, that is supple mentally called the logarithm-domain sum-product algorithmic program. Afterwards, the logarithm-domain algorithm (Log-SPA) is simplified to derive the MSA. Compared with the SPA, which requires extortionate multipliers throughout secret inciting, and the Log-SPA that requires advanced index computation during secret inciting, the MSA solely needs a comparator to consummate secret inciting, thereby considerably reducing the arduousness of hardware implementation. The MSA decoder developed during this study utilized 2 sorts of iteration (i.e., one iteration and ten iterations) to verify and compare the secret performance and committal to gains.

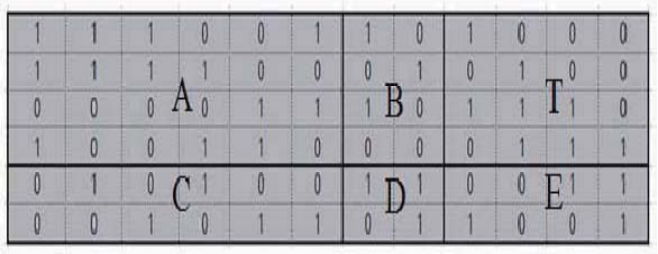


Figure 1: Parity Check Matrix (3, 6)

2. Min-Sum Decoding Algorithm

After obtaining a designed check matrix, the number of columns in the check matrix during decoding is equal to the number of check nodes *C (xi)*, and the number of rows is equal to the number of variable nodes *B (xi)*. In general, the Tanner Graph is used to connect the check nodes and variable nodes corresponding to each other. These connection paths are used to transmit the soft message regarding the log-likelihood ratio (LLR) of a signal. Fig. 1

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shows the regular parity check matrix with weight (3, 6), and Fig.2 shows the Tanner Graph of this matrix.

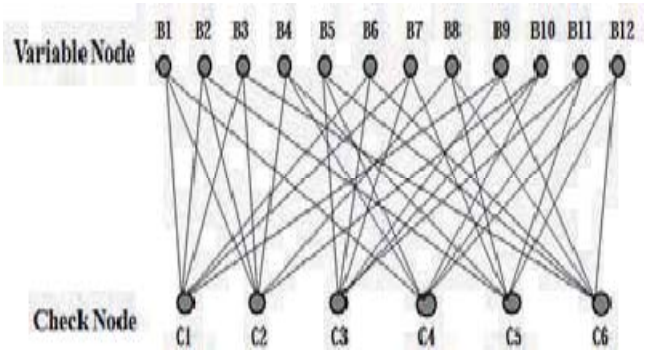


Figure 2: Tanner Graph of Parity Check Matrix (3, 6)

In the following, we assume BPSK modulation, which maps a code c = (Cl' *C2, ... ,* CN) into a transmitted sequence S *(Sl' S2, ... , SN),* according to Si 1, for 1, 2, . .. ,*N.* Then S is transmitted over an additive white Gaussian noise (AWGN) to Si after the demodulator is *Yi* = Si *ni,* where *ni* is a random variable with zero mean and variance *a 2.* We also assume is the related x parity check matrix. For ease of later use, let us define some notations as follows: the set of all variable nodes connected to check node with variable node excluded. *C* (i) the set of all check nodes connected to variable node with check node excluded the log-likelihood ratio (LLR) of bit which is derived from the received value *Yi.*

L(rji) : the LLR of bit which is sent from check node to variable node i. *L(qij)* : the LLR of bit which is sent from variable node to check node j.
L(i) : the posteriori LLR of bit computed at each iteration. The flow chart of BP algorithm is given below:

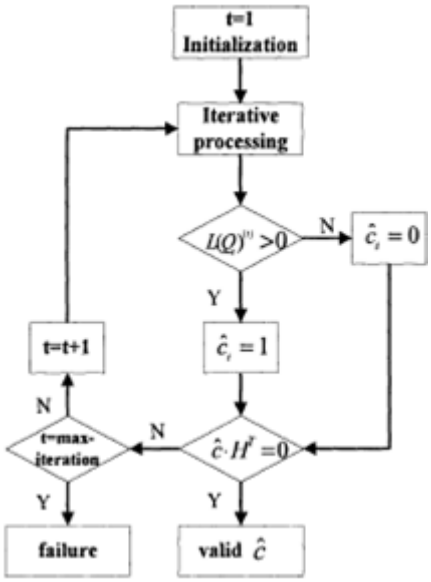


Figure 3: Flow Chart of BP algorithm

3. Research Approach

The proposed min-sum algorithm is implemented using Verilog HDL at QuestaSim 10.0b. The LDPC decoder is using the analog output from the channel after conversion to binary. The codeword from the channel will be then used with the H matrix to find the errors in the codeword. The errors will be then detected and removed. The FPGA implementation of the LDPC decoder then implemented using Xilinx ISE.

4. Conclusion

We have done a review of the LDPC Decoder using matrix (3,6). The Min.-sum algorithm is reviewed and based on this the FPGA implementation of the proposed architecture will be done in the project. The proposed architecture will be simulated on Questa-Sim.

References

[1] SHANNON C E. A mathematical theory of communication. CM SIGMOBILE Mobile Computing and Communications Review, 2001,5(1): 3-55.
[2] GALLAGER R G. Low-density parity-check codes[J]. IRE Trans. Inform. Theory, 1962: 21-28.
[3] KSCHISCHANG F R, FREY B J, LOELIGER H A. Factor graphs and the sum-product algorithm[J]. IEEE Trans. Inform. Theory, 2001: 498-519.
[4] FOSSORIER M P C, MIHALJEVIC M, IMAI H. Reduced complexity iterative decoding of low density parity check codes based on belief propagation[J]. IEEE Trans. Commun., 1999,47(5): 673-680.
[5] CHEN J H, MARC P C. Near optimum universal belief propagation based decoding of low-density parity check codes[J]. IEEE Trans. Commun., 2002,50(3):406-414.
[6] CHEN Y H, HSIAO J H, HE J S. FPGA Implementation and Verification of LDPC Encoder with Weight (3, 6) Approximate Lower Triangular Matrix[C]. 2nd ICCSNT, 2012:531-534.
[7] RICHARDSON T J, URBANKE R. Efficient encoding of low-density parity-Check Codes[J]. IEEE Trans. Inf. Theory, 2001,47(2):638-656. TANNER R.. A recursive approach to low complexity codes[J]. IEEE Transactions on Information Theory, 1981,27(5):533-547.
[8] SDR Forum website: at: http://www.sdrforum.orgH.
[9] JIANG M, ZHAO C, ZHANG L, et al. Adaptive Offset Min-Sum Algorithm for Low- Density Parity Check Codes[J]. IEEE Commun. Letters, 2006,10(6):483-485.
[10] LIAO Y C, LIN C C, LIU C W, et al. A dynamic normalization technique for decoding LDPC codes[C]. IEEE SIPS,2005:768-772

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