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Mechanism of Power Dissipation Capability of Power MOSFET Devices: Comparative Study between LDMOS and VDMOS Transistors

Aman Kumar Srivastav

IIT Delhi, India

Abstract: ***In this paper , the author has tried to understand the electrical-thermal coupling so as to understand the limits of power dissipation and he has compared the power dissipation in the two devices LDMOS and VDMOS. He has also tried to understand the mechanism of the power dissipation in both these devices.***

Keywords: Electrical-thermal coupling , Lateral/Vertical Diffused metal-oxide semiconductor field effect transistor(LDMOS/VDMOS), Zener Clamp , Snapback breakdown , RESURF (Reduced surface field)

1. Introduction

We are basically gone compare power dissipations in LDMOS and VDMOS and simulate both of them to try to understand the electrical-thermal coupling in these devices.The main agenda of all these experiment is to understand how does the power gets dissipated in these devices.These power dissipation helps us to decide the safe operating area of different devices.Electrical-thermal coupling effect is essential in understanding the limit of power dissipation. The detail of thermal and electrical interaction is not fully understood by us.Recently, Chung and Baird [6] reported a study on electrical-thermal coupling mechanism to explain the safe operating limit of LDMOS device. They proposed a 'Hot-Snapback' process that is sensitive to the lattice temperature and the operating voltage.

2. Experimental: Devices and Energy Capability

65V rated LDMOS and VDMOS transistors are integrated within a BiCMOS technology that is targeted primarily for high/analog power IC application.[7] Fig.1shows the device structures and components of the LDMOS and VDMOS power devices under investigation. The LDMOS and VDMOS differ in structure in only few aspects (as it cane seen in Fig.1(c) and 1(d)) like the position of the drain terminal in LDMOS is at the top and in VDMOS, the drain terminal was at the bottom of MOSFET , LDMOS uses RESURF layer(n-) near the surface to reduce the breakdown voltage , n-channel LDMOS have p-type substrate whereas n-channel VDMOS have n+ substrate.

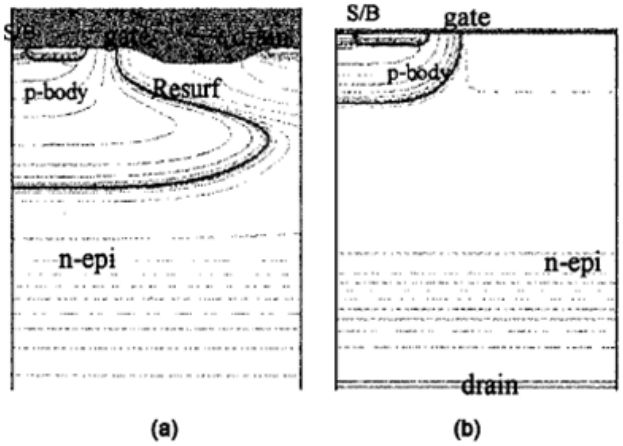

Figure 1: Structures of 65V feting power MOSFET devices integrated into a given BiCMOS technology, (e) the LDMOS device and (b) the VDMOS device. LDMOS employs the RESURF process to control the breakdown voltage

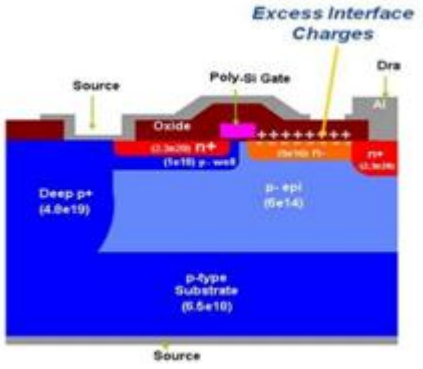

Figure 1 (c): LDMOS and

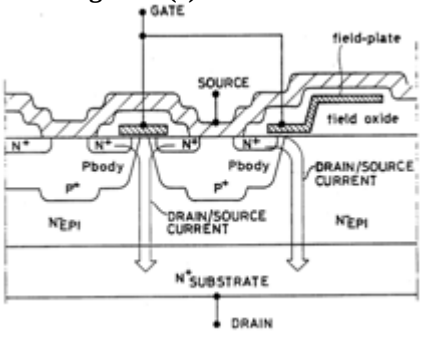

Figure 1 (d): VDMOS

The energy capability of LDMOS and VDMOS depends on the clamp voltages , ambient temperature and operating time. In energy capability test , we apply constant voltage between drain and source and maintain constant current for pulse time long enough to destroy the device.The power input is a single pulse with a rectangular waveform. An external Zener clamp between the drain and gate terminals sets the constant drain voltage. Fig. **2** shows a schematic of a clamp circuit (a) and typical voltage and current waveform (b). Ambient temperature is set by the chuck temperature ranging from **298K**to **453K.** Similar devices in size and shape were selected in order to eliminate concerns with the 3-D effects in diffusion.

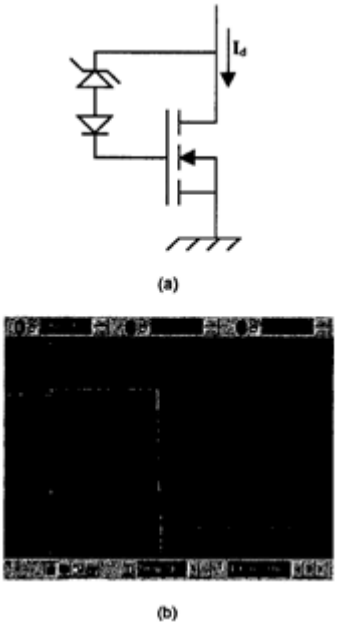

Figure 2: Transientpower capability characterisation (a) a schematics of test setup and (b) a typical input power wave bnn

The power dissipation capability is directly measured by difference in their time-to-failure. Fig. 3 shows the measured data on the input power density ***versus*** time-to-failure for both LDMOS and VDMOS devices included in the same wafer.

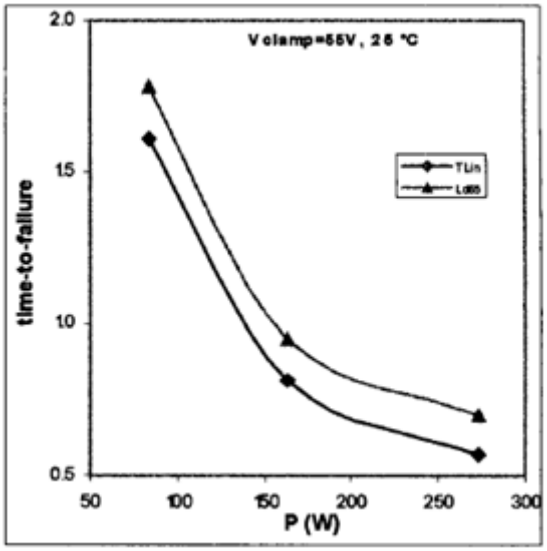

Figure 3: Comparison in time-to-failures measured between VDMOS and LDMOS with 65V rating.

The experimental results indicate that the LDMOS device reveals higher power dissipation capability by **10-20%** than the VDMOS device over the entire ranges.

Intuitively, VDMOS should have been superior to LDMOS in terms of energy capability . The power dissipation of the VDMOS device occurs vertically throughout the bulk epitaxial layer, while power dissipation of the LDMOS device takes place laterally, more likely in the surface region of the epitaxial layer due to the location of the drain terminal. Since most of the power dissipation occurs via conduction, the conduction is easy in bulk than the surface , so the power dissipation should have been more in LDMOS than VDMOS . However, the experimental results are opposite to this conventional thought. Difference in the power dissipation process between these LDMOS and VDMOS devices is theoretically analysed through simulation and discussed in the following section.

3. Simulation and Discussion

"The device simulation was performed using a non-isothermal method. The purely electrical operation significantly over-estimates, compared to natural electrothermal operation which properly includes the power dissipation process during the operation. The snapback breakdown characteristics are used to determine the ultimate operating limit, assuming that the snapback breakdown leads to thermal runaway formation. Here we focus on the difference in electrical and thermal coupling characteristics between the LDMOS and VDMOS devices."[7]. Fig. 4 shows the non-isothermal simulation results of I-V characteristics of the VDMOS and LDMOS transistors for two different ambient temperatures. The plots also include the changes in lattice temperature because of which there is fall in drain current after reaching the saturation level . The LDMOS simulation results show that as the lattice temperature reaches about **700K,** the snapback breakdown is triggered, independent of starting junction temperatures. This implies that activation of the snapback breakdown is controlled by power dissipation. As the starting junction temperature increases from **300K** to **400K,** the breakdown voltage of the devices significantly decreases. Since the starting junction temperature is increased from 300K to 400K , the temperature difference between starting and critical temperature is reduced and hence, the power required to reach the critical temperature decreases and the snapback voltage decreases.

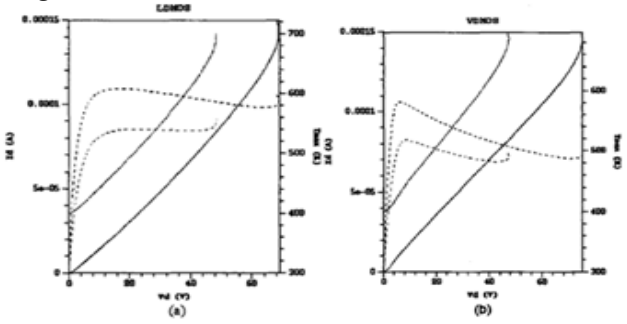

Figure 4: Non-isothermal simulation results of 1-V characteristics and the corresponding temperature changes for two different starting junction temperatures of (a) LDMOS and (b) VDMOS transistors.

Change in the snapback voltage with ambient temperature leads us to a conclusion that there is some electrical-thermal coupling.Due to some changes in thermal condition of the devices, there will be some changes in electrical properties of the device." As starting junction temperature increases from **300K** to **400K,** the snapback voltage of the LDMOS device decreases from 69V to 49V, about 29% while the snapback voltage of the VDMOS device decreases from **75** V to **44** V, about **41%.** Similar I-V behaviour with increasing the drain voltage and junction temperature is also observed for the higher starting junction temperature operation."[7]This difference in the extent of electrical-thermal coupling should have been the reason for the difference in energy capability of the devices which were experimentally observed.

Figure 5 shows a direct comparison in on- state I_d-V_d characteristics of the devices. The last data points of the current curves indicate the thermally coupled snapback breakdown limits. Notice the difference in the I-V characteristics between LDMOS and VDMOS. The drain current change with drain voltage of the VDMOS device appears to be more sensitive to power dissipation process than the LDMOS which implies less resistance faced by VDMOS than LDMOS which could be explained through the conduction process. Since most of the power dissipation occurs via conduction, the conduction is easy in bulk than the surface ,so the resistance faced at surface is more than that faced in bulk. "The LDMOS device shows that drain voltage increase leads to the drain current decrease, by about 10% just before the snapback activation. The drain current drop of the VDMOS device with the drain voltage is much more substantial, more than 30%."[7]There is a lattice temperature rise which decreases the electron mobility and hence the saturation drift current decreases in the graph."For similar starting saturation current levels, the power to activate the snapback breakdown is estimated to be 5.3 (W/mm) and 6.8 (W/mm) for the VDMOS and LDMOS devices, respectively. The corresponding snapback breakdown temperatures are **680K** and **700K."** [7]These simulation results indicate that LDMOS device can sustain higher power than the VDMOS, which agrees with the experimental data. And it also shows that there is less power dissipation in LDMOS than VDMOS.

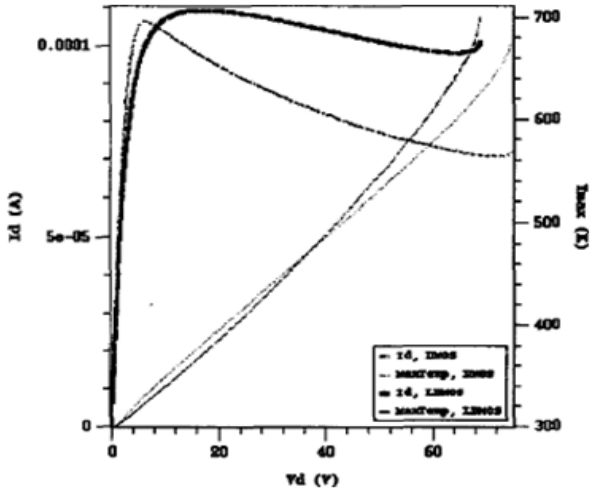

Figure 5: Simulated I_d-V_d characteristics and snapback limit of the VDMOS and LDMOS devices.

Among several different mechanism to dissipate the power, the electron current Joule heating is the dominant for NMOS devices. Fig. 6 and Fig. 7 show heat generation rates attributed to electron current Joule heating and the resultant lattice temperature change within the device structures at the onset of the snapback breakdown, respectively. The temperature profile within the structure is closely related to heat generation rate. The location of the highest temperature profiles is developed at the edge region of the channel end for the VDMOS case while the LDMOS device forms the hottest spot in the drift region toward the drain. LDMOS has the hottest point near the drain terminal because the electric field is highest in the RESURF layer near the drain terminal and same is the case with VDMOS, the field is more concentrated in drift region near the channel towards the drain that's why it is the hottest point in VDMOS.

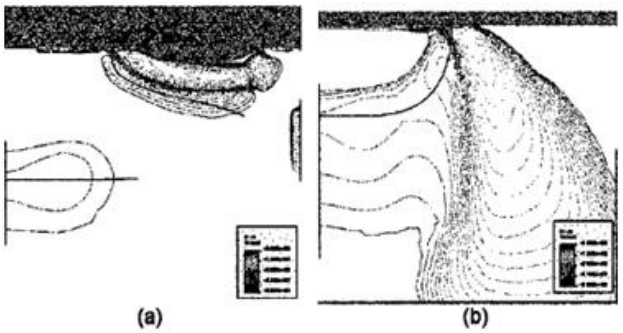

Figure 6: Heat generation rate within the devicesdueto electron currentJoule heating at the onset of the snapback breakdown,(a) LDMOS and (b) VDMOS.

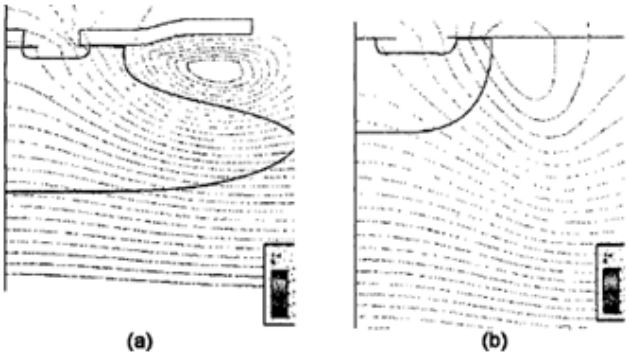

Figure 7: Temperature distribution within the devices due to power dissipation at the on-set point of the snapback breakdown, (a) LDMOS and (b) VDMOS.

4. Conclusion

Difference in energy capability between the LDMOS and VDMOS devices within a given technology was investigated from the power dissipation mechanics aspects. Experimental results showed that power capability of the LDMOS device was higher than the VDMOS device, by 10-20%. The power dissipation of LDMOS is lower than VDMOS. The electrothermal device simulations were performed to analyse difference in the power dissipation process between these devices. For transient power capability, temperature profile within the device plays a important role. Since there is a higher temperature profile closer to the channel and the base component, so VDMOS are subjected to snapback breakdown with less power that LDMOS.

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