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A CMOS 3–12-GHz Ultra wideband Low Noise Amplifier by Dual-Resonance Network

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Abstract: ***A low-power and high power-gain (S21) ultra wide-band low noise amplifier (UWB LNA) with flat noise figure (NF) based on global foundries 0.13-µm CMOS technology is reported. The load effect of common-gate (CG) topology is applied with dual-resonance load network for both wide band input matching and NF flatness. Combined with inductive-series peaking technique, the frequency response of CG-common-source cascade topology is further extended. The LNA circuit achieves the high and flat power gain of 13.5 ± 1.5 dB with input return loss better than 13dB and a flat NF of 4.3 dB ± 0.4 dB for frequencies 3-12 GHz. The fabricated LNA occupies a die area of 1.09 0.8 mm2 including pads and draw 8.5 mW from 1.2 V dc supply.***

Keywords: Common gate (CG), common source (CS), low noise amplifier (LNA), matching network, ultra-wideband (UWB)

1. Objective of Research

The main objective of the research presented in this thesis is to design a low noise amplifier to be used in radio technology for multimode operation. The goal of design is to understand the concepts of RF design such as gain, noise, matching networks and linearity that are essential for amplifiers. In the communication system, Low noise amplifier is the second element after antenna. LNA is used to boost up the signal of desire energy from the weak information signal of required energy with noise suppression. So, noise figure (NF) is the key issue of concern in this design. The receiver is the most power hungry block and the power consumption should be as low as possible. So, noise figure and power consumption are not less important issues than gain. With the small power consumption, the LNA should amplify the weak receiving signal to the level suitable for processing and provide gain to overcome the noise of subsequent stages while adding small amount of noise as possible. Matching of each block of the receiver is also an important issue in order to provide maximum power transfer at a particular frequency the matching is required. Furthermore, input and output matching to the source and load can maximize the gain. Input and output impedance matching is characterized by the input and output return loss. Since, it can affect the performance of the device. The gain should be large enough and the same time noise should be as less as possible. However, the gain of LNA should not be too high otherwise in the following stages, to ohm mixer is saturated. The LNA should present specific impedance at the input, e.g. 50 interface with the filter or antenna. Finding the delicate balance in all issues or parameters becomes the challenge more often than simply maximizing a single key parameter. The most recognizable trade-off is between LNA gain and noise figure (NF). Linearity is also an important design issue.

2. Introduction

CMOS technology has been widely applied in the RF and integrated circuit (RFIC) design because of its low cost, low power, and high integration related to other technology. The ultra-wideband (UWB) low noise amplifier (LNA) is the key component in the transceiver system, since it receives weak signal from the entire UWB band (3.1–10.6 GHz) and presents a enough signal-to-noise ratio for the following signal process; therefore, flat and enough power gain, and good input impedance matching with low and flat noise figure (NF) performance across the entire UWB band are required. Several techniques have been proposed for UWB LNA design. Filter synthesis technique is applied in the input matching network. However, the adoption of filter topology at input requires additional reactive elements, which results in higher NF and larger die size. The common-gate (CG) amplifier topology provides inherent wide band matching, low power, and high linearity; however, single CG stage cannot provide enough gain over the entire UWB band with enough gain flatness unless using extra stage with band width extension technique channel noise introduced by CG transistor degrades the noise performance. In this paper, the UWB LNA employing dual resonance load network is presented. The amplifier maintain slow power, wideband input matching, and reduced NF with flat and high power gain cross the UWB band.

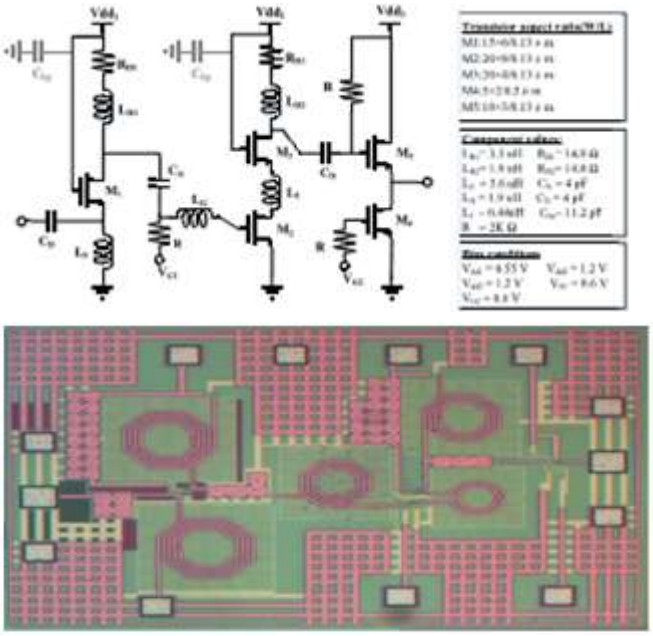


Figure 1: Schematic and chip micrograph of 3–12-GHz CMOS USB

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3. UWB LNA Circuit Design

Two stages employing cascade of CG (*M1)* and cascade (*M2* and *M4)* are applied for the proposed UWB LNA design. For wideband input matching, Fig. 2 shows the small- signal equivalent circuit of CG including the input of cascade stage. The input impedance can derived by

$$Zin(s) = (C_{gs1}||L_s)||\{1/ g_{m1}[1 + Z_L(s)/r_{ds}]\}$$

Where *gm*1 and *r*ds are the transconductance and output resistance of M1, respectively. *C*gs1 is the parasitic capacitance between gate and source of *M*1 and *LS* is the inductance

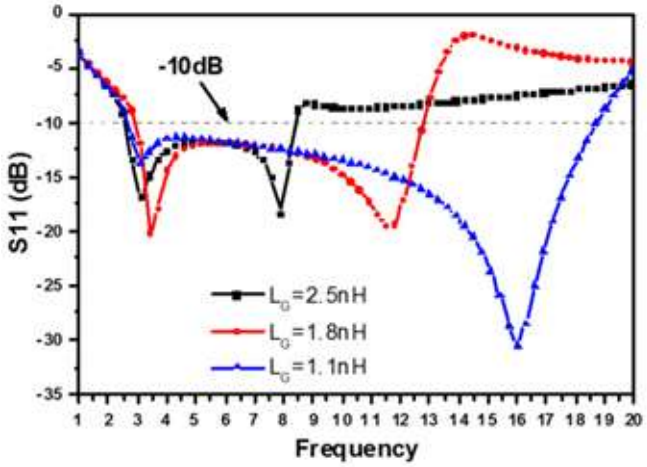


Figure 2: Illustration of wideband input matching dual-resonance network

To evaluate influence of the dual-resonance networking on input matching, the simulated *S*11 versus frequency is shown in Fig. The loading network is carefully designed. The two notch frequency points of *S*11 response are formed at low frequency (*ωo,* low*)* and high frequency (*ωo,* high*)*, respectively. These two notch responses extend the impedance matching condition. Meanwhile, bandwidth extension can be further illustrated by modifying the high frequency resonance (*ωo,* high*)*, as shown in by decreasing the inductance of *LG*, the higher notch frequency (*ωo*, high*)* in *S*11 response increased, resulting a wider impedance matching bandwidth. Meanwhile, the low notch frequency point (*ωo,* low*)* remains when the inductance of *LG* decreases. It is worthy to mention that, different from conventional CG-based UWB LNA input matching technique, which presents single notch frequency in the middle band of *S*11 versus frequency characteristics [2], the proposed dual-resonance network achieves wideband input matching by introducing two notch frequency at the low and high band of *S*11 versus frequency characterizes. The NF of the LNA is dominated by first CG stage and can be given by

$$NF = 1 + (\gamma/\alpha)(r_{ds}/r_{ds} + Z_{L\,(s)})$$

Where $\alpha = g_{ds}/g_d0$ is the ratio of the transistor transconductance to the channel conductance at zero VDS, *γ is* the channel thermal noise coefficient. For given rds, the NF is decreased with an increase of load network impedance $Z_{L\,(s)\,.\,TO}$ achieve flat and low NF over wideband, one needs to provide high impedance of load network over wide frequency range. In the proposed design, the load network is designed to provide high impedance over the wideband by introducing two resonances at low and high frequency, respectively

4. Circuit Design

The UWB LNA requires high gain, low noise figure and high linearity over the entire band with low power consumption. The LNA also needs to have a good input mating over the whole band to capture the transmitted RF energy efficiently. Figure 1 shows a schematic of the proposed three-stage amplifier. The first stage is the RC-feedback cascode topology that provides high gain, wider bandwidth, better stability and well reverse isolation. The middle stage is an inductor-capacitor parallel configuration (LB//CB) to pull up high frequency gain. The output stage is a simple current buffer that gives broadband out impedance of 50 ohm for measurement purposes. Schematic of the ADS-designed UWB CMOS shunt resistive-feedback LNA circuit which uses TSMC's 0.18□m RF CMOS technology. The dashed circle is LB//CB shunt topology

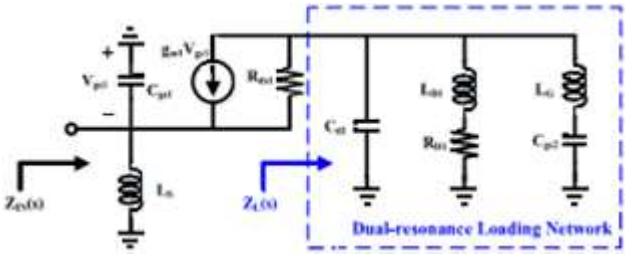


Figure-3 Small-signal equivalent circuit of CG stage including load network at the drain of M1

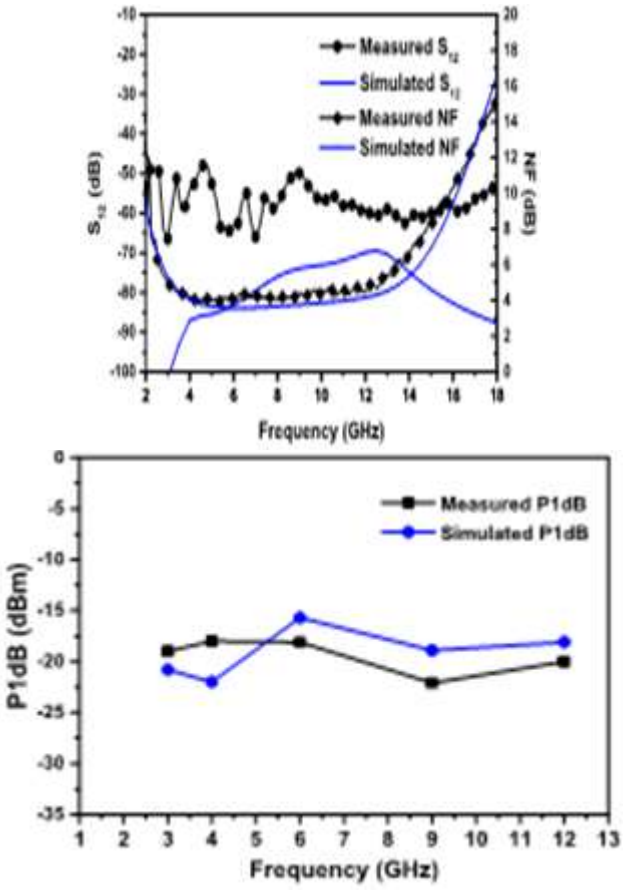


Figure 4: Measured input P1dB of the LNA

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5. Measurement Results

The standard 0.13-µm CMOS process provided by Global Foundry is adopted to design the UWB LNA. Fig. 1(b) shows the chip micrograph of the LNA. The chip area is 0.86 mm2. The LNA consumes 8.5 mW from a power supply of 1.2 V (excluding output buffer stage). Fig. 5 shows the measured and simulated S11 and S21 of the LNA. As can be seen, S11 of −11 to −17.6 dB for frequencies 3–12 GHz is achieved. The high and flat of 13.5 ± 1.5 dB for frequencies 3–12 GHz is achieved. The corresponding 3-dB bandwidth is 9 GHz. In addition, the simulated and measured NF of the LNA is shown in Fig. 6. The minimum NF of 3.8 dB at 4.7 GHz, and flat NF of 4.3 ± 0.4 dB for frequencies 3–12 GHz are achieved. Fig. 7 shows the measured input 1-dB comp. The performance of the proposed LNA and the recent publication is summarized in Table I. Compared with other work, the proposed LNA exhibits low and flat NF response, power gain (S21), low dc power, and high FOM, ression point (P1dB) at 3, 4, 6, 9, and 12 GHz of the LNA

6. Conclusion

A wideband LNA design approach is proposed based on dual-resonance network. Due to the unique feature of the proposed approach, wideband input impedance matching, and low and flat NF can be achieved simultaneously. The measured results show that the proposed LNA technique is suitable for UWB system.

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