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Design of Second Order Discrete Time Sigma Delta Modulator for High Resolution Applications

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Abstract: ***Aim of This work is to Design a second order discrete time sigma delta modulator for low frequency high resolution applications, which can be used in data converters (sigma delta ADC) where high resolution is required for more accuracy in signal processing's. A real world is analogue but easier to process digital data ex: speech, image processing's. Analog signal contains too much unnecessary data ADC samples the data and splits into finite information. Sigma delta ADC is very much suitable for less area low frequency and high resolution data conversions. Now the aim is to design a sigma delta modulator in which these parameters plays major role 1) resolution 2) order 3) OSR 3) power consumption 4)SNR 5)SNDR 6)dynamic Range. This design is carried out with the 180nM CMOS technology at an operating voltage of ±700mV, and the results are tested with the help of Cadence Virtuoso Spectre Circuit Simulator.***

Keywords: op-amp, 180nM, sigma-delta modulator, SDM

1. Introduction

All available natural signals are analog signals but it is easy to process digital signals, so there is always demand for analog to digital and digital to analog convertors. There are many ADC architectures are available but sigma delta ADC will have its unique advantage comparing with others .in general there are two types of ADC architectures are available they are one is nyquist rate ADCs and the second one is oversampling ADCs, these sigma delta ADCs will comes under the oversampling ADCs. The oversampling technique will avoids the use of sharp filters or aliasing filters, by using high gain and full swing amplifiers the signal degradation in intermediate stages can be avoided. The Sigma Delta ADC consists of manly two blocks they are modulator and decimation filter. High resolution is the main key factor which gives the unique position to the sigma delta modulator ADC among other ADCs. Sigma delta ADC consists of two blocks they are one is modulator and the other one is decimator.

The current work concentrates on the design of Discrete Time second order sigma delta modulator. To achieve the target performances of sigma delta modulator, a new approach was made as design of low voltage & low power modulators for that purpose, the design of low voltage and low power high performance operational amplifier is required. Low voltage means less than half of the nominal voltage, for 180nM nominal voltage is 1.8V but the current work designs the whole module with operating voltage of ±700mv.and the low power means the power consumption should be in the range of 1µ to some tens of µwatts. This prototype modulator achieve excellent performance constraints for a given bandwidth and resolution in spite of low supply voltages. In the design of low order modulators aiming at achieving high resolution with limited power budget particular attention should be given to power-resolution trade-offs involving the design of multi-bit quantizers. A smaller quantizer input range translates in a lower linearity requirement for the last integrator and at the same time in a smaller input offset for the quantizer comparators. These requirements are conflicting in terms of power demand especially in low voltage nanometer technologies [2]. This paper is organized in the following manner. Section II describes the operation and block diagram of sigma-delta modulator. Section III discusses the design of operational - amplifier and its power optimization. Section IV details the simulation results of proposed sigma delta modulator and comparison. Section V provides conclusion and future scope.

2. Block Diagram

The block diagram of discrete time sigma delta modulator consists of mainly

1) Sampling circuit: it consists of a switch when it is on signal will be transferred otherwise maintains the same level; it is used to sample the input signal.
2) 2nd order discrete time sigma delta modulator: It consists of two integrators with mixer circuit as shown in block diagram.
3) Comparator: It is used to compare the signal from output of integrator with the reference signal
4) DAC: Here 1-bit DAC is used; output pulse signal is given as the feedback to the input through DAC, and for better noise shaping feedback is given to the second integrator also through mixer.

The organization of above blocks can be shown as

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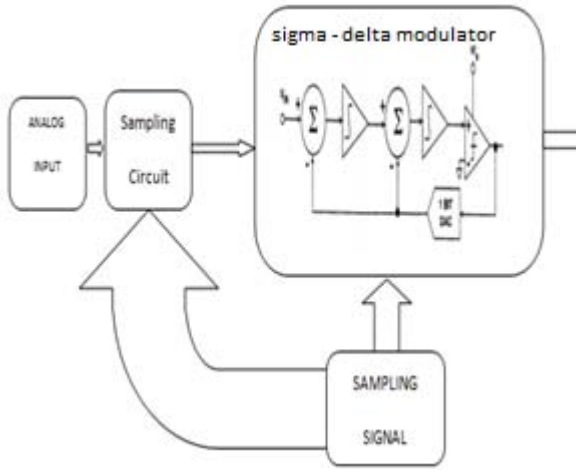


Figure 1: Block diagram of sigma delta modulator

This work mainly concentrates on design of low power second order sigma-delta modulator because of better noise shaping and also to improve the SNR & DR.

3. Design & Simulation

3.1 Design of Operational amplifier

The considered operational amplifier is two stage CMOS operational amplifier and the block diagram is given by

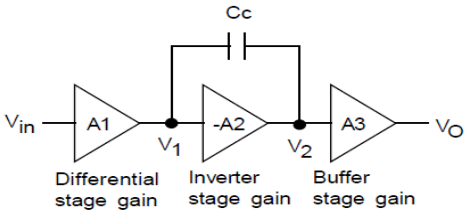
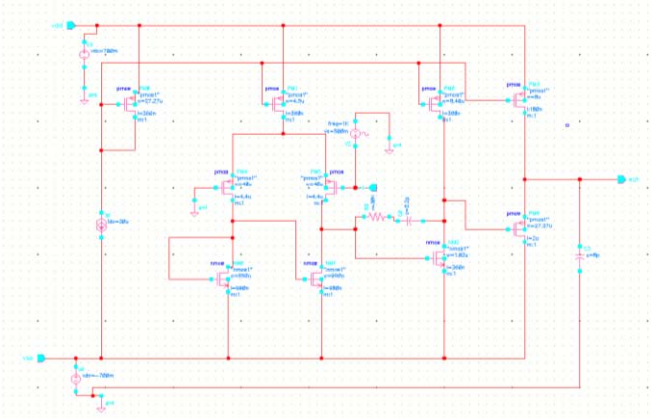


Figure 2: Op-amp General Block Diagram

The differential gain stage can be designed in two ways, they are
1) With the help of PMOS differential pair op-amp
2) With help of NMOS differential pair op-amp

Schematic diagram of two stage CMOS OP-amps are shown below



(a)

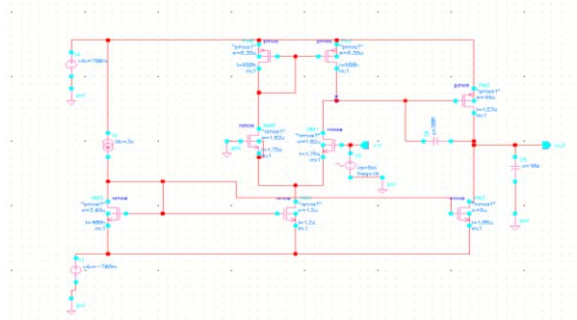
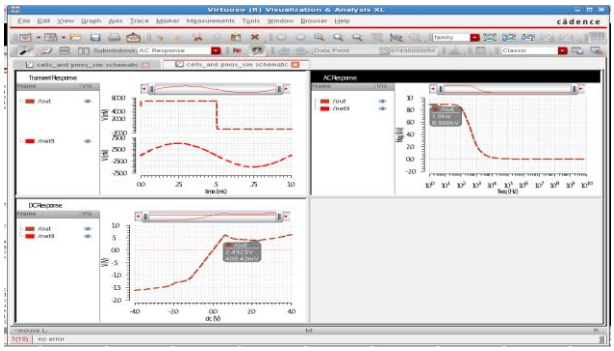
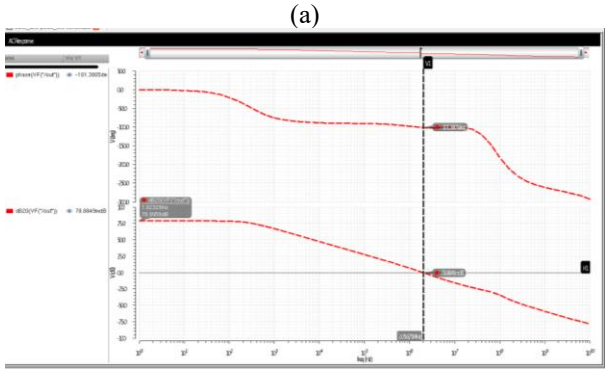


Figure 3: (a) PMOS differential pair (b) NMOS differential pair two stage CMOS op-amp circuit.

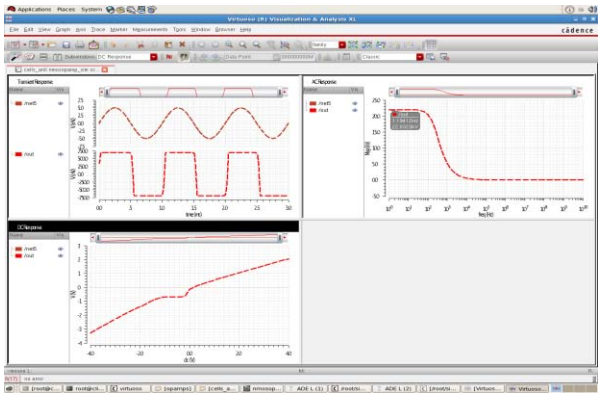
Simulation results of the above circuits in cadence virtuoso simulator are



(a)

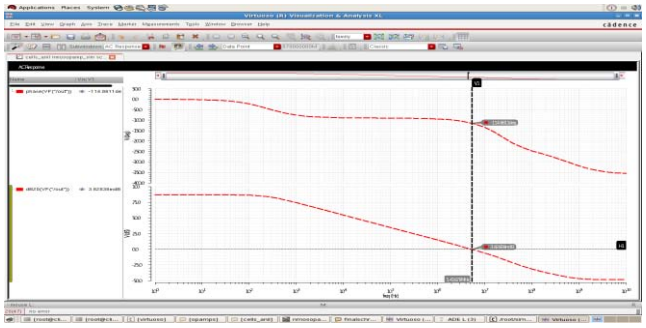


(b)



(c)

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(d)

Figure 4: (a) & (b) are the results of PMOS differential pair op-amp
(c) & (d) are the results of NMOS differential pair op-amp

Comparative analysis of simulations results of above two simulated op-amps is given by

Table 1: Comparative analysis of two stage op-amps

Specifications	Simulated results of PMOS differential pair Two stage CMOS op-amp	Simulated results of NMOS differential pair Two stage CMOS op-amp
Gain	78.99 dB	86.7Db
Phase margin	78.6degrees	65.2degrees
UGF	2.072MHz	5.419MHz
CMRR	76.7dB	86.58dB
Power Consumption	31.53µwatts	4.39 µwatts

By comparing above two circuits, it is clear that two stage CMOS op-amp with NMOS differential pair results are very good and achieves lower power than the PMOS differential pair and achieves good result. So, for further simulations am choosing two stage CMOS op-amp with NMOS differential pair as my op-amp so from now in the next stages of this paper op-amp implies two stage CMOS operational amplifier with NMOS differential pair.

3.2 Design of Sampling Circuit

The sampling circuit using the NMOS differential two stage CMOS op-amp is given as

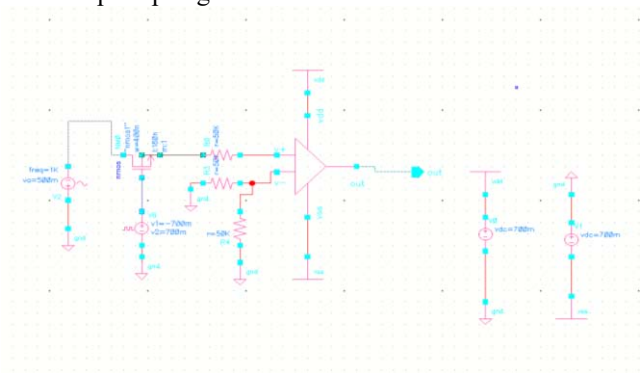


Figure 5: sampling circuit

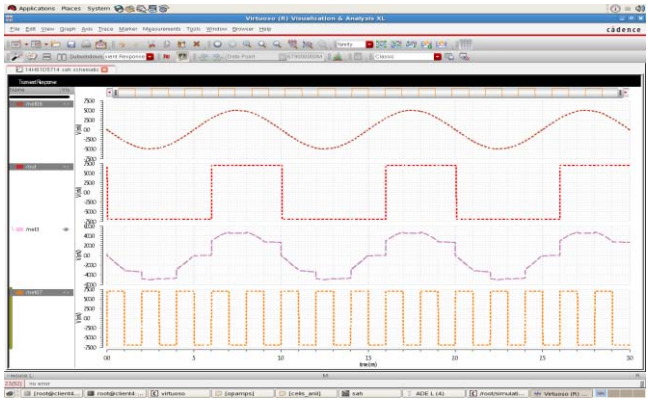


Figure 6: transient analysis of sampling circuit

3.3 Design of Sigma delta modulator

Second order discrete time Sigma-Delta Modulator cicuit is

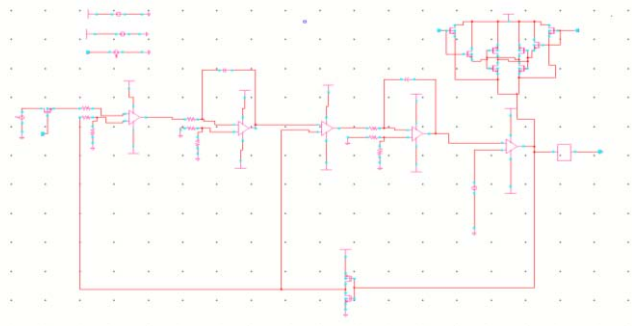


Figure 7: Second order DT Sigma-Delta Modulator circuit

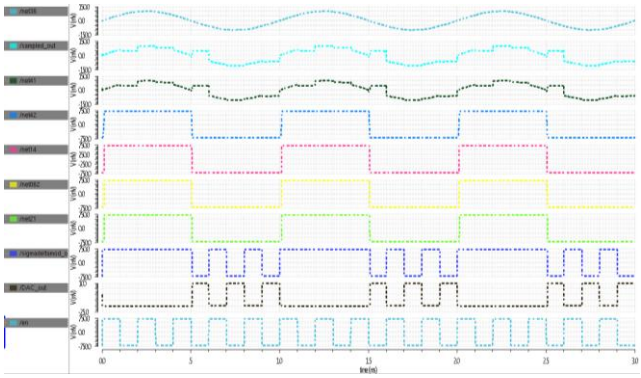


Figure 8: Transient response of Sigma-Delta Modulator

4. Results tabulation and comparison

The comparison with the reference [1] and this work is tabulated as,

Table 2: Comparison table

	Paper[1],2015	This work
Technology	180nM	180nM
Power supply	±900mV	±700mV
Input clock	250kHz	5MHz
Signal bandwidth	500Hz	2KHZ
OSR	250	1024
ENOB	10.5bits	23.4bits
Power	4.6µwatts	35.6µwatts
SNDR	64dB	70dB

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5. Conclusion and Future Scope

This paper presented the designing low power discrete time Sigma Delta modulators. The developed modulator design was done in CADENCE virtuoso spectre circuit simulator with the technology of 180nM CMOS, at an operating voltage of ±700mV, obtained better SNR& ENOB for specified input signal bandwidth. In future the order can be increased for better noise shaping and also there is a lot of scope to increase input signal band width for other applications with high resolution.

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Author Profile



R Anil Kumar pursuing the M.Tech in VLSI system design from ANURAG GROUP OF INSTITUTIONS and completed B.tech degree in Electronics and Communication Engineering from Bandari Srinivas College Of Engineering Technology in 2014.



E Srinivas received the B.Tech degree in Electronics and communication Engineering from Anurag Engineering College, in 2007 and M.Tech degree in VLSI System Design from Anurag Group of Institutions (Formerly CVSR College of Engineering), in 2010. He is Currently Pursuing his Ph.D degree in Electronics and Communication Engineering at JNTU Hyd. His Doctrol research is directed towards the design a low voltage, low power VLSI Analog circuits

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