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Fusion of March Algorithms in Counter based BIST for the Detection of Faults in RAM

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Abstract: ***Embedded memories covers the major portion and are the inevitable part of many of the SoC solutions. They are most sensitive to faults due to the dense design..A wide variety of faults can occur, causing various failures in the memory functions. Component density, Circuit layout, Manufacturing methods are some of the sources of the occurrence of the faults in the memories. Built-in self-test (BIST) mechanism has widely been used to test memories like RAMs, since it reduces the test cycle duration and the complexity. A counter-based BIST architecture is used here. Several algorithms of different complexities are developed to test RAMs. Among them, March algorithms were considered as the simple and widely used ones. It consist of sequences of read and write operations for the detection of faults. Fusion of March algorithms like MATS, March C and March X are used in this work for the detection of Stuck-at fault, Coupling fault and Transition fault respectively. Detection of different faults in a RAM memory using a single counter based BIST design is advantageous. Selection of the March algorithm is based upon a mode selection switch. Compression of the test data is carried out using a decoder module. The fusion of the test algorithms optimizes the performance of the BIST Controller. Detection of different faults in a RAM memory using a single counter based BIST design is advantageous. Compressed test data is obtained in the simulation result, using a decoder module. The design of the Counter-based BIST module reduces the area overhead and complexity compared to that of the FSM-based design The implementations are carried out by using Verilog hardware description language and Xilinx ISE 13.2.The proposed method reduces the fault detection time as well as the tester storage requirement.***

Keywords: Built-inself-test, Coupling fault ,March algorithms, March C, March X, ,MATS ,Stuck-at fault, Transition fault

1. Introduction

Memory modules cover a large part of the SoC‟s. The dense packing of the cores may create faults in the cells, leading to the improper functioning of the memory. As a result detection of the fault is essential. In future this diagnosis can provide a feedback to the IC manufacturing or can be used for the repairing using different techniques. As the technology evolves, complexity in the design process also get increased. Due to this, defects types are becoming more complex, diverse and are unable to detect during test procedures.

Built-in self-test techniques are gaining ground in the testing due to their cost-effective way to test high-density modules. It reduces the test cycle duration and the complexity. It needs only to power-up a chip, initiate the test signal and reads the chip status. As a result higher fault coverage without excessive cost can be applied. The motivation behind this BIST mechanism is that this logic can be incorporated in a chip, for both manufacture testing and in circuit testing. In memory BIST (MBIST) technology, a controller is used to implement a specific memory test algorithm when the module is under test. Over the years, several algorithms of different complexities have been developed to test RAMs. These algorithms were specifically designed to detect faults from various fault models. In this work, March Algorithms that have been applied for BIST implementation is selected. It is the widely used test algorithm and the reason for its popularity is its simplicity. Different varieties of March Algorithms like March C,March X, MATS, March DD, March RAW ,etc are there for the detection of different faults. March tests consist of finite sequence of March elements. Within the ,March element ,a number of memory read and write operations called access commands are there. On this work, a fusion of March C, March X and MATS algorithms for the detection of stuck-at fault, coupling fault and transition fault. Selection of the algorithm is based upon a mode selection switch. The fusion of the test algorithms can optimize the performance of the BIST Controller. Detection of different faults in a RAM memory using a single counter based BIST design is advantageous. The design of the Counter-based BIST module reduces the area overhead and complexity.

2. Preliminary Work and Motivation

In RAMs there is a technique of BIST scheme with diagnostic data compression. In that a March Algorithm named, MARCH RAW is used for the detection of functional faults [1]. SFs and DFs are the two classification of functional faults. The classification is based upon the number of different operations in a sensitizing operation sequence. In that method a March-element–based compression technique which compresses the diagnostic data is used. The diagnostic data include the session number, faulty address and hamming syndrome (HS),of a detected fault to external automatic test equipment. Syndrome is obtained by performing XOR operation on the test and the expected data, there by indicating the faulty bit in a word. If in a RAM having stuck-at 1 (SA1) fault is tested by March RAW, then the Pause And Export way for each read operation export the same diagnostic data three times when the second element of March RAW is tested .To overcome this MEB Compression scheme is proposed, which avoid the redundant diagnostic data. The motivation behind the preliminary work is [1].The design consists of mainly a Controller,TPG Block,MEB Compressor. Controller is the interface to the TPG.It feds commands to the TPG as March elements. Here March RAW Test is used.Stuck-at-0 fault is used in this design. Within the

Controller block, two types of PISO"s was used, which is used for inputing the commands. In March RAW six March elements were there.

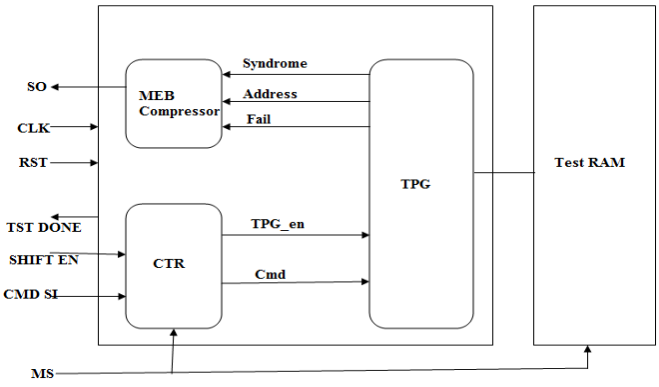

Figure 1: Block Diagram of BIST with MEB compressor

TPG is the Test Pattern Generator , which internally consists of RAM memory, Write memory and Comparator for detecting fault. The commands from the controller is decoded and executed by the TPG. During the write operation the value is written into the corresponding memory address. During the read operation, test memory value is compared with reference and fault detection takes place. A bit representing the fault and syndrome of the fault were the outputs of TPG.

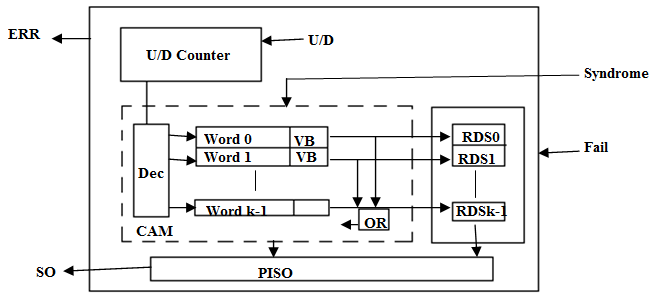

Figure 2: Block diagram of MEB compressor

The third important block of the design is the MEB Compressor. Syndrome Compression and Syndrome Exportation are the two phases in it. When a fault is detected by the first read operation its Hamming Syndrome(HS)is stored in a memory array as ,W0 and the corresponding valid bit(VB) is set to 1.If faults were detected by the subsequent read operations of March element,its HS is compared to the previous stored HS in W0. If a match is found,the corresponding Read Deteection Status(RDS) register records which read operation detects the fault else the U/D counter is counting up by 1 and the new HS is stored in memory,W1.This continues until all the test operation in March element gets completed. In Syndrome Exportation, the diagnostic data including Addr,RDS,HS and EB are exported serially through a PISO.

3. Memory Fault Models

Variety of physical failures can occur in memory array, leading to the failures in memory functions. May the component density, circuit layout or manufacturing method be the reasons. Different numbers of faults models have been developed to capture such effects. In this section, the important fault models relevant for the functional testing of RAMs using BIST,which is used in the proposed work is described.

- **Stuck-at fault models (SAF):** A memory cell is said to be SA1 or SA0 if its contents remain fixed at logic 1 or 0, irrespective of what is written into it.
- **Coupling Fault Model (CF)**: A pair of memory cells is said to be coupled if a transition in one of them changes the contents of the other cell from 0 to 1 or 1 to 0.Idempotent coupling fault and Inversion coupling fault are the two types of such faults. Transition in one cell forces the contents of another cell to a certain value(either 0 or 1)it is called as Idempotent coupling fault, whereas the later is one which the transition causes an inversion in the contents of the second cell. Coupling faults could also exist between three or more cells.
- **Transition Fault Model[2] (TF):** A cell fails to make a transition from zero to one and one to zero when it is written.

3.1 March Test Algorithms

March test algorithms are the widely used test algorithm because of its simplicity. A march test consist of different number of march elements delimited by parentheses. It consists of number of read-write operations called as access commands. Different types of march algorithms are there. Among them March RAW, March C,MATS and March X were selected for the proposed work. The rx in attest represents read operation and wx represents write operation. The complexity of a March test is linear with respect to the size of the memory under test. March algorithms are selected according to their fault coverage. If the fault coverage is more for an algorithm then that particular algorithm is most useful for testing. The different algorithms used in the work are as follows.

MATS

{ ⇕ (w0); ⇕ (r0,w1); ⇕ (r1)}

MARCH X

{ ⇕ (w0); ⇑ (r0,w1); ⇓ (r1,w0); ⇕ (r0)}

MARCH C

{ ⇕ (w0); ⇑ (r0,w1); ⇑ (r1,w0); ⇓(r0,w1); ⇓(r1,w0); ⇕ (r0)}

4. Proposed Work

Different March Tests are used for detecting different faults in RAM. A Fusion of March Algorithms in BIST for the detection of various faults in RAM is proposed here. Test Algorithms include March C, March X and MATS[2] for Stuck-at fault, Coupling fault and Transition fault. The selection of the algorithm is carried out using a mux with the

help of a mode selection switch. BIST technique is used here for test problems. A dedicated BIST controller is used to implement a specific memory test algorithm when the chip is under test .Counter and FSM based method are the two types existing. Area overhead is more in FSM based BIST. Of these counter based technique is used in the work, since its design and implementation is less complex. Optimization of the design is carried out by using the selected three algorithms in a single module, incorporated with a multiplexer for their selection.

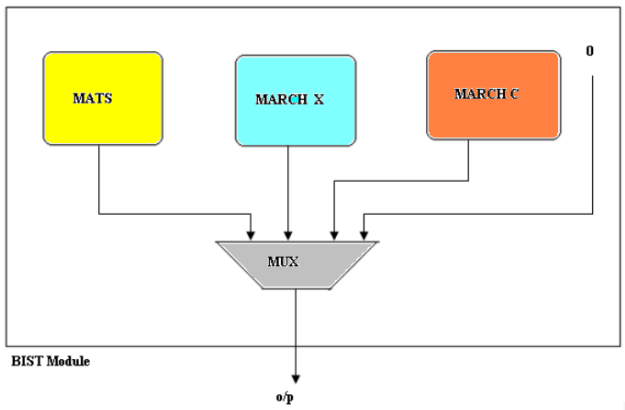

Figure 3: Block diagram of proposed work

Each March algorithm module mainly consists of counter, decoder ,memory section and comparator. Input data, address and switching between reading and writing the memory is carried by the counter. Counter itself produces the address and data. Separate counters are designed for each March Algorithm since the length of counter bit varies. The decoder module compresses the data written into it. Variable length memory module is implemented according to the selected algorithm for test. Comparator compares the data from the fault memory with the expected data.

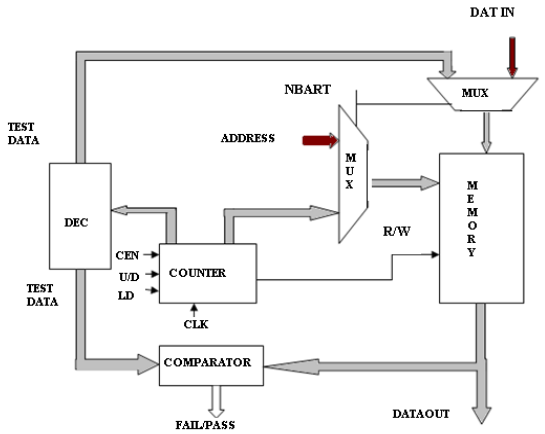

Figure 4: Block diagram of BIST A rchitecture

The reading operation is carried out when transition occurs between 1 and 0 for R/W control. Next, reading of zeros from all the memory locations, then writing ones to all the memory locations. The controller has two modes of operations, the Normal mode and the test mode. The flow between normal mode and test mode is controlled by two multiplexers. In the normal mode,the ordinary writing and reading operation of the memory. The memory read operations is initiated by means of the signal R/W. The operation gets completed when all the March elements are passed through the memory.

5. Experimental Results

MATS,MARCH C and MARCH X Algorithms are implemented on a single BIST Controller.Verilog HDL code of the modules was written and synthesized using XiLinx ISE 13.2.Memory selected for the work was RAM .Mainly the three faults were implemented in the memory. For the three test modules corresponding fail/pass signals were existing.MATS, MARCH X and MARCH C Algorithms were designed for the detection of Stuck-at fault, Coupling fault and Transition fault respectively. If an algorithm is executed for the detection of a particular fault, its corresponding fail/pass signal shows whether a fault is existed or not. Among the Counter and FSM based BIST design ,first one is chosen for the work. Compared with the FSM based design the area overhead of the counter based design is less .The proposed work optimizes the design by incoporating three modules in the single BIST module.

Figure 5: Simulation Result

A Stuck-at fault is introduced in the memory location. Execution of the MATS code detects the fault in the memory and the corresponding fail/pass signal shows a „1" ,which is the indication of fault. Along with that the address of the fault and tset data is also obtained.

6. Conclusion

A BIST scheme with the fusion of March Algorithms has been proposed for the fault detection in RAMs. BIST mechanism has widely been used to test memories like RAMs, since it reduces the test cycle duration and the complexity .The fusion of the test algorithms optimizes the performance of the BIST Controller. Detection of different faults in a RAM memory using a single counter based BIST design is advantageous. Compressed test data is obtained in the simulation result, using a decoder module. The design of the Counter-based BIST module reduces the area overhead and complexity compared to that of the FSM-based design.

References

[1] Chih-Sheng Hou,Jin-Fu Li,and Ting-Jun Fu, "A BIST Scheme With the Ability of Diagnostic Data Compression for RAMs," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL.33,NO.12 ,December 2014.

[2] Elsa Joseph and Rony Antony P, "VLSI design and comparative Analysis of Memory BIST Controllers",International conference on computatioanl systems and communications(ICCSC),December 2014.
[3] Jin-Fu Li, Ruey-Shing Tzeng And Cheng-Wen Wu, "Diagnostic Data Compression Techniques for Embedded Memories with Built-In Self-Test," in Journal Of Electronic Testing: Theory and Applications 18, 515–527, 2002.
[4] Sybille Hellebrand, Hans-Joachim Wunderlich, Alexander A. Ivaniuk, Yuri V. Klimets, and Vyacheslav N. Yarmolik, "Efficient Online and Offline Testing of Embedded DRAMs," IEEE Transactions On Computers, VOL. 51, NO. 7, July 2002.
[5] Manoj Franklin and Kewal K Saluja,"Built-in Self-Testing of Random-Access Memories",University of Wisconsin-Madison
[6] N. Mukherjee, A. Pogiel, J. Rajski, and J. Tyszer, "High volume diagnosis in memory BIST based on compressed failure data," IEEE Trans.Comput.-Aided Design Integr. Circuits Syst., vol. 29, no. 3, pp. 441–453,Mar. 2010.
[7] R.-F. Huang, C.-L. Su, C.-W. Wu, Y.-J. Chang, and W.-C. Wu, "A memory built-in self-diagnosis design with syndrome compression," *in Proc IEEE Int. Workshop Curr. Defect Base. Test. (DBT)*, Napa Valley, CA,USA, Apr. 2004, pp. 97–102.