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A New Cascade H-Bridge Inverter Based Multi-Level Statcom for High Power Applications

U. Rosaiah[1], M. Lokesh[2]

[1]PG Scholar, Dept of EEE, MITS College, Angallu, Chittoor, AP, India

[2]Assistant Professor,Dept of EEE, MITS College, Angallu, Chittoor, AP, India

Abstract: ***The industrial power sector and domestic power sector requires bulk power transfer from sources, in which reactive power andpower quality (PQ) are the major issues.This paper presentscascaded H-bridge inverter based multi-level static compensator (STATCOM) using space vector pulse width modulation technique (SVPWM). The main objective is reactive power compensation with improved power quality. The topology consisting of two standard H-bridge inverters connected through a three-phase transformer. In high power applications,VAR compensation is achieved using multi-level inverters. The SVPWM is the best reliable advanced modulation technique, enables better DC bus utilization. In addition SVPWM produces fewer harmonic in the output voltage and current thus gives quality of power.The performance of the scheme is analysed through MATLAB/SIMULINK.***

Keywords: Power Quality(PQ), Static Compensator (STATCOM), Space Vector Pulse Width Modulation (SVPWM), Volt-Ampere Reactive (VAR).

1. Introduction

Generation and transmission of power is complex process, it requires working of many components to produce maximum output. In which, the main component is reactive power in the system. To deliver the required active power through transmission lines, voltage is needed to be maintained. Reactive power is required for operation of loads such as motor loads and other inductive loads [1]. The performance of ac power system can be improved by maintaining this reactive power efficiently and which is generally called as reactive power compensation [2]-[3]. The reactive power compensation is associated with load compensation and voltage support [8]-[9].In recent years, static VAR compensators like the STATCOM have been developed [4]-[5]. These static VAR compensators come under Flexible AC Transmission Systems (FACTS)and it can absorb or generate the reactive power if it is required.

It is difficult to operate medium voltage grids with a single power semiconductor switch directly. Therefore multi-level inverters have been preferred for higher voltage levels. In industrial applications, multi-level inverters have more attention. These inverters can be used as static VAR compensators and also used in renewable energy systems, motor drives etc. [7]-[8]. Generally multilevel inverters have output voltage levels of more than two levels.This leads to generate reduced harmonic distortions in the output voltages and high quality output waveforms. Additionally, these inverters can have fraction of dc-link voltages when batteries, capacitors are used as sources. Multi-level inverters with these characteristics can be best suited for high-power and high-voltage applications. Inmulti-level family cascade Multilevel Inverter(CMI) is one of best topology due to its own advantages than other inverters [2]. The control of dc-link voltage of inverter is illustrated [10]-[11].

These inverters have been implemented with various PWM techniques [13] to control the output voltage and frequency also for better DC-AC power conversion. In the other hand, the usage of space vector pulse width modulation technique has been increased in last decade due to several advantages such as reduced total harmonic distortion [THD] and commutation losses. Thus quality power is achieved with these techniques.

The Overall paper is organized as follows: The section I presents introduction about the proposed system. Section II represents control scheme and proposed system description. Section III represents the concept of space vector pulse width modulation technique. Section IV represents Simulink model results respectively. Overall conclusion is shown in section V.

2. System Modelling and Description

The power system and STATCOM model is shown in Fig.1. This model represents the connection point of STATCOM in the power system

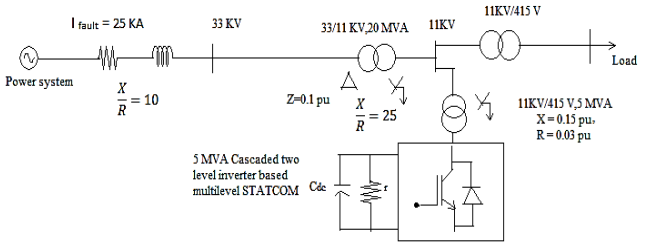


Figure 1: Power system and the STATCOM model

The schematic diagram of cascaded two-level inverter based multi-level STATCOM is shown in Fig.2. In which the low-voltage (LV) side and high voltage (HV) side of a transformer is connected to inverter and grid respectively.

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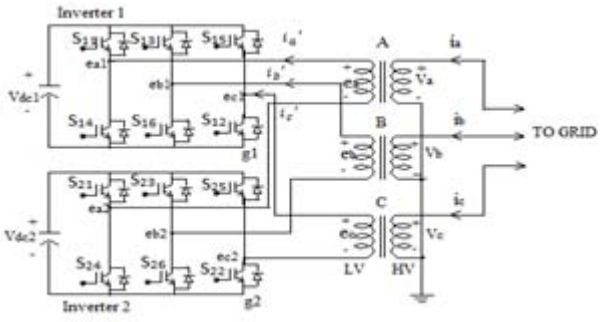


Figure 2: Cascaded two-level inverter based STATCOM

From the Fig.3, the three phase RMS source voltages V_a', V_b' and V_c' referred to the low-voltage side of the transformer. The leakage inductances of low-voltage side windings of the transformer are L_a, L_b and L_c respectively. The transformer losses are represented in terms of resistances, which are r_a, $r_b$and r_c respectively. The output voltages of inverter1 and inverter2 are e_{a1},e_{b1} , $e_{c1}$and e_{a2}, e_{b2}, e_{c2}. Finally leakage resistances of dc-link capacitors C_1 and C_2 are r_1 and r_2 respectively.

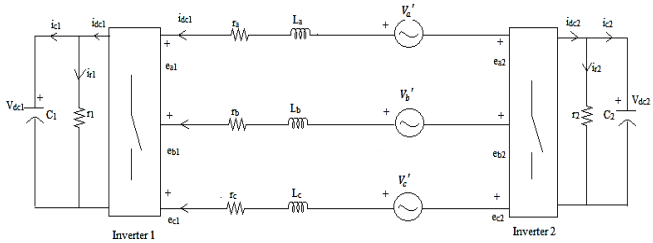


Figure 3: Equivalent circuit of two-level inverter based STATCOM

A. Phase Equivalent Circuit

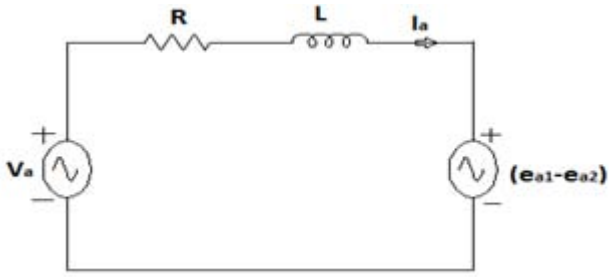


Figure 4: Equivalent circuit of phase a

Equivalent circuit of phase „a" is shown in Fig.4. In the figure, the RMS source voltage is represented as v_a' , total loss in the system is represented as R, the transformer winding leakage inductance is represented as L, the voltage across primary side of the transformer of inverter1 and inverter2 is (e_{a1}-e_{a2}).

Applying KVL to the loop

$$-v_a' + R_a I_a' + L_a \frac{di_a'}{dt} + (e_{a1}\text{-}e_{a2}) = 0 \quad (1)$$

Similarly for „b" and „c" phases

$$-v_b' + R_b I_b' + L_b \frac{di_b'}{dt} + (e_{b1}\text{-}e_{b2}) = 0 \quad (2)$$

$$-v_c' + R_c I_c' + L_c \frac{di_c'}{dt} + (e_{c1}\text{-}e_{c2}) = 0 \quad (3)$$

By assuming resistances $R_a = R_b = R_c = R$ and inductances $L_a = L_b = L_c = L$, the above can be written in mathematical model form as,

$$\begin{bmatrix} \frac{di'_a}{dt} \\ \frac{di'_b}{dt} \\ \frac{di'_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & 0 \\ 0 & \frac{-r}{L} & 0 \\ 0 & 0 & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i'_a \\ i'_b \\ i'_c \end{bmatrix} + \frac{1}{L} \begin{bmatrix} V'_a - (e_{a1} - e_{a2}) \\ V'_b - (e_{b1} - e_{b2}) \\ V'_c - (e_{c1} - e_{c2}) \end{bmatrix} \quad (4)$$

The equation (4) is known as mathematical model in the stationary reference form of cascaded two-level inverter based STATCOM. To control both the active and reactive currents independently, above stationary reference frame equations can be converted into rotating reference frame equations. The source voltage of q-component is set to be zero so that the source voltage of d-component can be align with the synchronously rotating reference frame.

The dynamic model in the synchronously rotating reference frame is give as

$$\begin{bmatrix} \frac{di_d'}{dt} \\ \frac{di_q'}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & \omega \\ -\omega & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i_d' \\ i_q' \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v_d' - (e_{d1} - e_{d2}) \\ -(e_{q1} - e_{q2}) \end{bmatrix} \quad (5)$$

Herev_d' represents the direct (d)-axis voltage component of ac source andi_d' , i_q' represents d-axis and q-axis current components of cascaded two-level inverter.

B. Control Strategy

The block diagram of control circuit is shown in Fig. 5. The d-axis and q-axis voltages can be controlled as follows

$$e_d^* = -x_1 + \omega L i_q' + v'_d \quad (6)$$

$$e_q^* = -x_2 - \omega L i_d' + v'_q \quad (7)$$

Where $e_d^*$and e_q^* representsd-axis and q- axis reference voltage components of the inverter. The parameters x_1 and x_2 are known as control parameters and these can controlled as

$$x_1 = \left(k_{p1} + \frac{k_{i1}}{s}\right)(i_d^* - i_d') \quad (8)$$

$$x_2 = \left(k_{p2} + \frac{k_{i2}}{s}\right)(i_q^* - i_q') \quad (9)$$

Where i_d^* is the direct (d)-axis reference current and is given by

$$i_d^* = (k_{p3} + \frac{k_{i3}}{s})[(V_{dc1}^* + V_{dc2}^*) - (V_{dc1} + V_{dc2})] \quad (10)$$

Where V_{dc1}^* and V_{dc2}^* represents the reference voltages of dc-link capacitors of inverter 1 and inverter2. The reference reactive current component i.e q-axis component i_q^* is obtained either from load, when used for load compensation or from voltage regulation loop when used in transmission lines.

Fig.5. Shows that the three phase voltages v_a, v_b, v_c are given to phase-locked loop (PLL) to generate the unit signals$\cos \omega t$and $\sin \omega t$. Phase lock loop or phase locked loop (PLL) is a type of control system, which is used to generate output signal to match the phase of input signal. These unit signals are used to transform the converter currentsi_a' , i_b' , i_c' intosynchronously rotating reference frame currents. So that it is easy to control reactive and active current components. These currents consist of large switching frequency ripples and which are eliminated by using low-pass filters (LPF). The reference voltages to the converter are e_d^*, e_q^* are generated from controller using $(V_{dc1}^* + V_{dc2}^*)$andi_q^*. The inverter supplies desired reactive

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component of current i_q^* and draws active component of current i_d' by considering these reference current components. Which can be further used to regulate total dc-link voltage $V_{dc1}^* + V_{dc2}^*$ of the inverter.

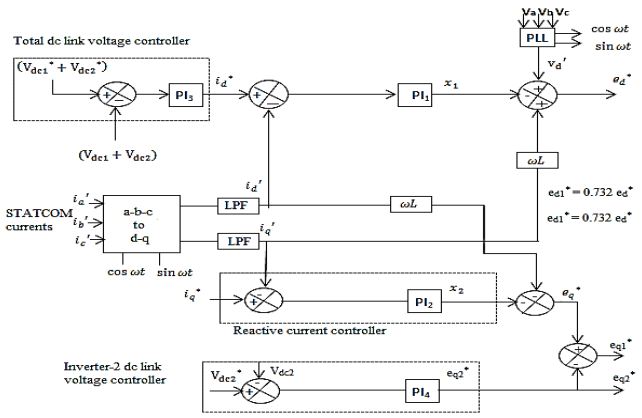


Figure 5: Control circuit diagram

C. DC-LINK Balance Controller

The total dc-link balance controller is used to provide magnitude and phase of resultant voltage supplied by the cascaded inverter. The active power sharing between the inverter and grid is depends on angle δ.From the figure, the reference voltage components of q-axis of the two inverters e_{q1}^* , e_{q2}^* is obtained as

$$e_{q1}^* = e_q^* - e_{q2}^* \quad (11)$$

$$e_{q2}^* = \left(k_{p4} + \frac{k_{i4}}{s}\right)(V_{dc2}^* - V_{dc2}) \quad (12)$$

Where e_{q1}^* controls the inverter1 dc-link voltage, e_{q2}^*controls the inverter2 dc-link voltage. The dc-link voltage of inverter 2 is controlled at 0.366 times dc-link voltage of inverter 1, so four level operation is obtained and output voltage harmonic spectrum is improved. The inverter1 dc-link voltage and inverter2 dc-link voltage is expressed in terms of total dc-link (V_{dc}) voltage.

$$V_{dc1} = 0.732\ V_{dc} \quad (13)$$

$$V_{dc2} = 0.268\ V_{dc} \quad (14)$$

The power transfer to inverter1 is indirectly controlled and for inverter2, power transfer is directly controlled. Therefore inverter2 attain its reference value quickly when compared to inverter1. The control circuit uses the sinusoidal pulse width modulation (SPWM) technique to generate gate signals from the obtained reference voltages.

3. Concept of Space Vector Pulse Width Modulation Technique

Space vector modulation (SVM) is generally developed as a vector approach to the pulse width modulation (PWM) used for three phase voltage source inverters (VSI). The SVPWM inverter generates higher voltage and lower harmonic distortions at the output compared to the sinusoidal PWM inverter (SPWM).Mostly PWM techniques have been applied to three phase voltage source inverters (VSI). The circuit diagram of three phase voltage source inverter is shown in fig.6

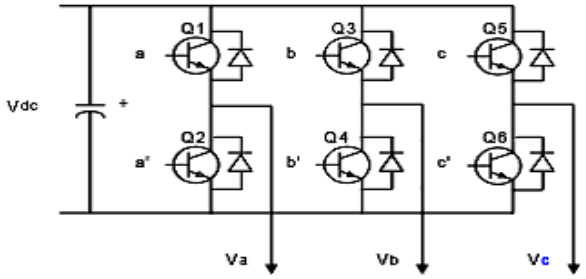


Figure 6: Three-phase voltage source inverter

The three phase voltages of a three phase inverter are Va, Vb and Vc respectively. The six power transistor switches $Q_1$to Q_6 are controlled by switching variables a, a¨ b, b¨ and c, c¨. The working principle is when upper switches are turned ON i.e a, b or c is 1, corresponding lower switches are turned OFF i.e a, b or c is 0. The ON and OFF of upper switches Q_1, Q_2 and Q_3 are used to determine the output voltage.

The relation between line-line output voltage in vector form $[V_aV_bV_c]^t$ and switching variables vector $[abc]^t$is given by the equation

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (15)$$

Similarly for phase voltage vector relation is given by

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (16)$$

Where V_{dc} is dc bus voltage or supply voltage. The maximum line to line and phase output voltage achieved by SVPWM is given by

$$V_{phmax} = \frac{V_{dc}}{\sqrt{3}} \text{ and } V_{llmax} = Vdc \quad (17)$$

The upper power transistor switches ON and OFF states gives eight possible combinations i.e six non zero vectors and two zero vectors. The six non zero vectors are (V_1-V_6) gives hexagonal shape and zero vectors are (V_0-V7). The eight combinations and phase or line voltages in terms of supply voltageVdc is given in table.

Table 1: Switching pattern and output voltages

Voltage vectors	Switching vectors			Phase voltage			Line to Line voltage		
	A	B	C	Van	Vbn	Vcn	Vab	Vbc	Vca
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

By assuming d-axis is fixed horizontal axis and q-axis fixed vertical axis, the phase voltage representation in the vector form with the eight switching patterns can be obtained by the d-q transformation to the phase voltages.

$$T_{abc\text{-}dq} = \frac{\sqrt{2}}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \quad (18)$$

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This d-q transformation is equivalent to orthogonal trajectory of [a, b, c]^t on to two dimensional perpendicular to vector [1,1,1]^t in the three-dimensional co-ordinate system. This results six non-zero and two zero vectors are possible. The six non-zero vectors (V_1-V_6) shapes the axis of hexagonal, supplies power to the load connected shown in figure.7. The zero vectors (V_0,V_7) are at the origin and supplies zero voltage to the load.

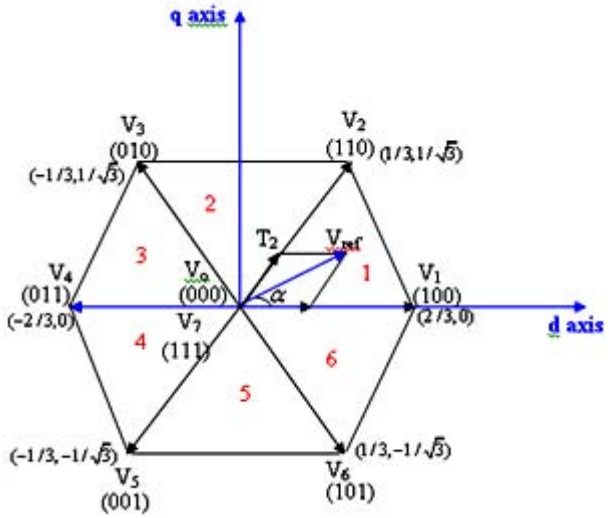


Figure 7: Basic switching vectors and sectors

The angle between any adjacent two non-zero vectors is 60 degrees. The eight vectors are called space vectors denoted as (V_1, V_2, V_3, V_4, V_5, V_6, V_7,V_8). To obtain reference voltage vector V_{ref}or V_{out} d-q plane, same transformation can be applied to output voltage. The magnitude of $V_{out}$is the RMSValue of the line to line voltage with defined d-q transformation.

The main objective of SVPWM technique is approximate the reference voltageV_{out} instantaneously by using eight switching combination corresponding to the basic space vectors. One of the simple way of approximation is generate the output voltage of inverter same as the reference voltage over a small time period T.

$$\int_{nT}^{(n+1)T} V_{out}(t) = \frac{1}{T}(T_1 V_x + T_2 V_{x\pm60}) \quad (19)$$

$$V_{out}(nT) = \frac{1}{T}(T_1 V_x + T_2 V_{x\pm60}) \quad (20)$$

In the equation T_1, T_2 are time duration to the switching states corresponding to V_x and V_{x+60} (or V_{x-60}) are applied. The V_x and V_{x+60} (or V_{x-60}) are basic space vectors formed the sector containing of V_{out}. If we assume change in reference voltage V_{out} with in small time of T, then equation (19)becomes (20), Where T_1+T_2< T. The time T be small with the change in speed of V_{out} , so it becomes critical. In practical, approximation is for every time period T_{pwm}.Therefore it is too difficult that to have small time period T with respect to change in V_{out}.

Equation (20) is for every PWM period, approximate the V_{out} with the inverter is in switching states V_x and V_{x+60} (or V_{x-60}) for time duration of T_1 and T_2 respectively. The sum of time durations T_1 and T_2 should be less than or equals to T_{pwm} and inverter should be at the origin in rest of the period. Therefore equation (20) becomes (22),where

$$T_1 + T_2 + T_3 = T_{pwm} = T \quad (21)$$

$$T_{pwm} V_{out} = T_1 V_x + T_2 V_{x\pm60} + T_0 (V_0 \text{ or } V_7) \quad (22)$$

We get the T_1, T_2 equation from the (22) equation

$$[T_1\ T_2]^t = T_{pwm}[V_x V_{x\pm60}]^{-1} V_{out} \quad (23)$$

Here $[V_x V_{x\pm60}]^{-1}$ is known as normalized decomposition matrix for the sectors. If we assume the angle between V_x and V_{out} is α then for time durations T_1 and T_2 is

$$T_1 = \sqrt{2} T_{pwm} ||V_{out}|| \cos(\alpha + 30^0)$$
$$T_1 = \sqrt{2} T_{pwm} ||V_{out}|| \sin(\alpha) \quad (24)$$

Advantages of SVPWM are

- SVPWM utilizes the dc bus voltage efficiently and generates the less total harmonic distortions (THD) compared to the SPWM.
- Low switching losses and wide modulation range is possible.
- Higher fundamental voltage magnitude i.e15.5% more over SPWM.
- Variable frequency control, voltage magnitude control and lower power losses.

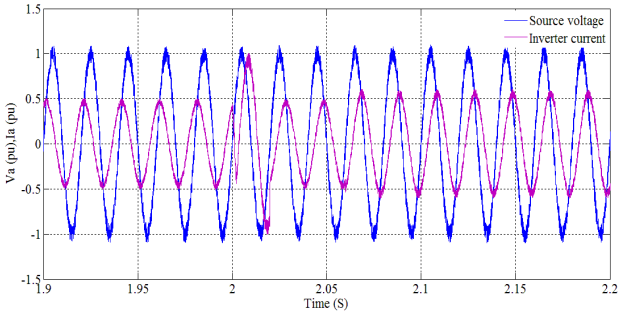
Table 2: Shows the different system parameters used in simulation

Rated power	5 MVA
Transformer voltage rating	11KV/400
AC supply frequency, f	50 HZ
Inverter-1 dc link voltage, Vdc1	659 V
Inverter-2 dc link voltage, Vdc2	241 V
Transformer leakage reactance, X_l	15%
Transformer resistance, R	3%
DC link capacitances, C_1, C_2	50 mF
Switching frequency	1200 Hz

4. Simulation Results

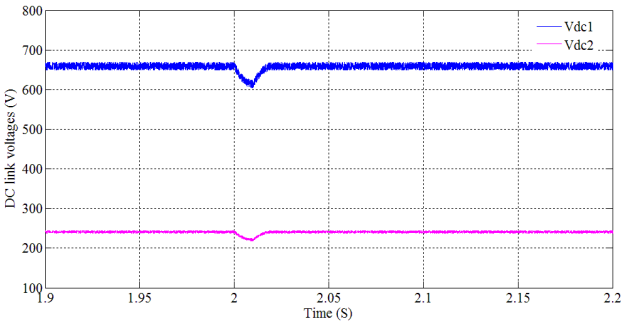
A. Reactive power control

Fig.8 shows the waveforms of source voltage and inverter current, DC-link voltage of two inverters in the reactive power control case.



(a)

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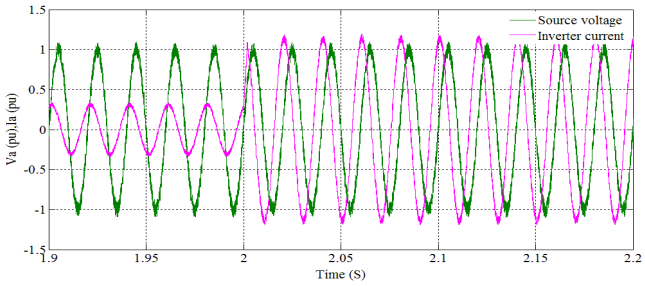
(b)

Figure 8: a) Source voltage and Inverter currentb) DC-link voltages of two inverters

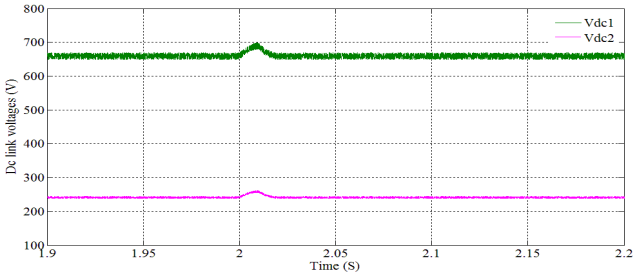
In this case reactive power is controlled by setting i_q^* i.e reference reactive current component at a particular reference value. Initially i_q^* is set at 0.5 p.u. At t=2.0 s, i_q^* is changed from 0.5 to -0.5. Dc-link voltage of two inverters are regulated during the STATCOM modes are changed.

B. Load compensation

In this case, reactive power of the load is compensated by the STATCOM. Initially STATCOM supplies the current of +0.5 p.u. When load current increases at t=2.0 s, STATCOM supplies more than +0.5 p.u. Therefore load compensation is effectively achieved by the STATCOM. The DC-link voltages of two inverters V_{dc1} and V_{dc2} are regulated at their respective values when STATCOM operating modes are changed.



(a)

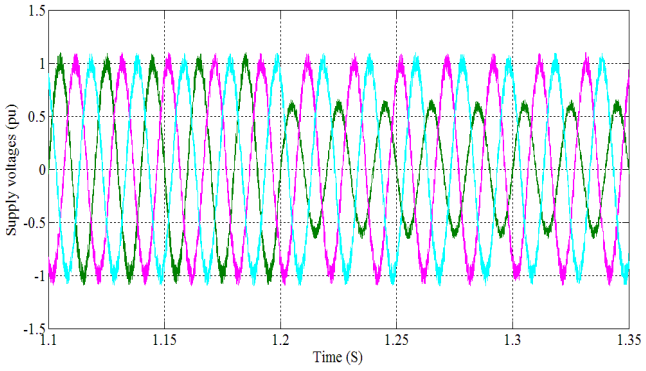


(b)

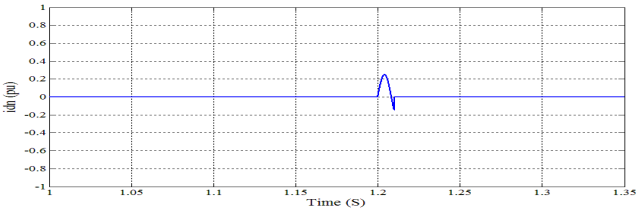
Figure 9: a) Source voltage and inverter current b) DC-link voltages of two inverters

C. Operating during the fault condition

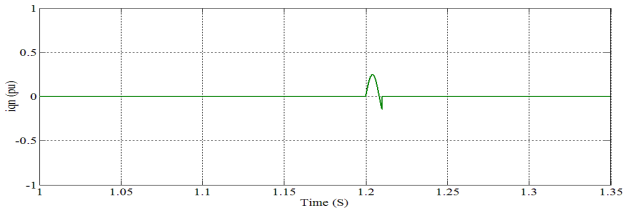
Fig.10 shows the waveforms of grid voltages on LV side of the transformer, during the fault condition. In which, a single line to ground fault is created at 1.2s and cleared after 200 ms on A phase of HV side of the 33/11 kv transformer. The corresponding d-q axis currents of the inverter are shown. The fault currents are regulated at their respective values i.e at zero.



(a)



(b)

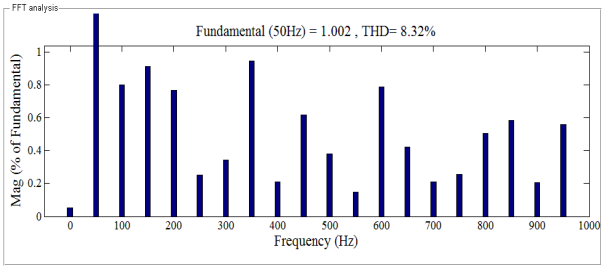


(c)

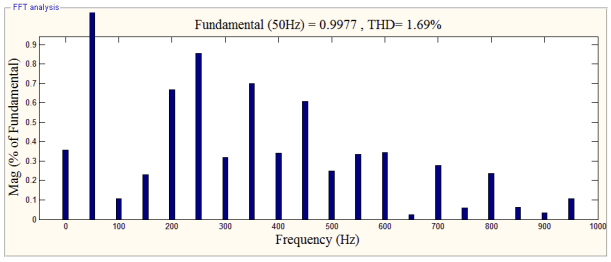
Figure 10: a) Grid voltages on the LV side of the transformer b) d-axis negative sequence current component c) q-axis negative sequence current component

5. FFT Analysis

The frequency spectrum of different signals is obtained by this FFT analysis.



(a)



(b)

Figure 11: FFT Analysis showing THD of load voltage by using SPWM&SVPWM

Powergui block can be used to obtain the frequency spectrum of any signal directly. The bar graph shows the order of

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harmonics and its magnitude. FFT analysis is carried out to study the harmonic spectrum of load voltage and load current before and after using SVPWM.By using SVPWM the THD load voltage reduced from 8.32% to 1.69%.The THD of load voltage with SPWM and SVPWM is shown in table.

Inverter modulation technique	*THD in Load voltage (%)*
Sinusoidal Pulse width modulation	8.32
Space Vector Pulse width modulation	1.69

6. Conclusion

This paper presents cascaded H-bridge inverter based multi-level static compensator (STATCOM) using space vector pulse width modulation technique (SVPWM).The main objective is to compensate the reactive power with the improved power quality. Sinusoidal pulse width modulation have better control on output voltage magnitude, they accounts for harmonics in the output voltage. By using space vector pulse width modulation the total harmonic distortion can be further reduced and it has various advantages than the SPWM. The scheme is analysed at various opearating conditions. SVPWM reduces the THD of load voltage from 8.32% to 1.69%. Thus power quality is improved with reactive power compensation.

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Author Profile

U. Rosaiahreceived B.Tech (EEE) Degree from JNTU, anantapuram in the year 2013. At present pursuing M.Tech in Electrical Power Systems from Madanapalle Institute of Technology & Science (MITS), Madanapalle, Andhra Pradesh, India.

M. Lokesh, M.Tech., Assistant Professor in the Department of Electrical & Electronics Engineering, Madanapalle Institute of Technology & Science (MITS),Madanapalle, Andhra Pradesh, India.

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