International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Impact Factor (2012): 3.358

Empirical Study of Incorporation of SET and Hybrid CMOS-SET in Decision Making Sub-Systems

Jayanta Gope[1], Aloke Raj Sarkar[2]

[1]Department of Electronics and Communication Engineering, Camellia School of Engineering and Technology, Camellia Group, Kolkata, West Bengal, India

[2]Dept. of Electrical Engineering, Camellia School of Engineering and Technology, Camellia Group, Kolkata, West Bengal, India

Abstract: ***Recent evolution in physics and fabrication technology has led to new horizon in electronics, one such promising candidate is the Single Electronics Technology that attracted huge attention in both academics and industry. It represents a new class of electronics that precisely detect and control the transport of individual electron and thereby create Single Electron Devices for next generation electronics in nano regime. SETs are considered as the next generation electronics for post CMOS VLSI ICs because of unique principle of operation, quantized nature of carrier transport, ultra small size and low power dissipation like intrinsic properties. Researchers now aim to emphasize this technology in every sphere of life. The authors here take this opportunity to employ SETs in designing decision making sub-system which is not only novel in nature but simultaneously very fascinating but challenging act. The designed model is tested using Monte Carlo based simulation tools so that to investigate all possibilities of the decision making. Further its fabrication strategies were analyzed which revealed two significant drawbacks of the SET model. The authors surveyed the possible solutions and hence hybrid CMOS-SET model was considered for designing the same decision making model. The second designed model is unique of its kind because applying hybrid CMOS-SET model for decision making has not been reported much previously. The second model was also empirically tested on T-Spice and subsequently both the results were compared to achieve the best viability.***

Keywords: SET, Hybrid CMOS-SET, T-SPICE, Decision making sub-system**.**

1. Introduction

Single Electronic Device (SED) ushered a revolution in contemporary device research and is anticipated to rule the market in very recent by introducing massive production technology. Thus it is for sure, that the next few decades would enjoy the privilege of nano-scale devices based on SEDs. Introducing this spectacular technology, Researchers now reveal the art of fabrication using e-beam lithography technique for electronic devices in small vicinity resulting in a massive reduction of power consumption and deducing the device size to nano-scale devices. They now aim to investigate every possible ways to articulate this technology in every sphere of life. This has led SED to challenge the human brains decision-making capability at present; thereby implementing such subsystem that can interface common non expert human brain with sophisticated technology to solve complex issues. One such complex course of action has been reported in this study related to the decision making of policy making aiming the utmost correct decisions to be taken, thereby, leading to automation of a person's career and life risk without involving any expert's physical presence or counseling.

Another most admiring concurrent research trend that has attracted lot of attention is Hybrid CMOS-SET. This aspiring but innovative research has augmented nano scale device study for next generation electronics. In the subsequent sections we have adopted this Hybrid CMOS-SET technology to design the above said decision making sub-system which advocates for novelty of our design. Besides such uniqueness of the model we have made empirical studies of it to explore its maximum flexibility in designing domain. The MIB compact model for SET device simulation was first incorporated to set the design and lastly the BSIM4.6.1 model for CMOS was integrated into the test-bench. The results showed better trade-off as anticipated in the abstraction mode of the designing.

2. Analytical Study of SET

SED, a pioneering-next generation electronics is envisaged as one of the most successful and booming Technology encompassing the modern physical effects of electron charge transport. It portrays infinite development in device study and depicts better figure of merit in nano-scale electronic device technology even though it integrated a number of open challenges for the future elegant solutions. Size reduction properties of SEDs have appeared to be blessings, rather than an obscurity as there was no compromise made in the consequences of the outcome in applying SEDs in modern technology [1-5].

SET posses various advantages over exiting bulk semiconductor devices and reveals great figure of merit but owing to its inherent physical limitations it has several open challenges waiting for elegant solutions. Single electronics inherently utilizes the opportunity and controls the movement and position of a single electron or a small number of electrons. As per orthodox theory, the single electron box is the simplest circuit, which exhibits what single electron charging effects is. The box is quite complex

Licensed Under Creative Commons Attribution CC BY

to understand but at the same time it is also relatively simple to manufacture and measure in the laboratory. A metal granule remains on one side which is connected by a tunnel junction. On this side electrons can tunnel in and out which resonates the electron transport phenomena. Millikan was the first to demonstrate the manipulation of single electrons in the metal granule in the seminal empirical studies at the very beginning of 1900, but it consisted of several impetus earlier research work in Messophysics [6-8]. As per several scientific investigation reports this delay in the implementation was due to the fact that manipulation requires the reproducible fabrication of very small conducting particles and their accurate positioning with respect to external electrodes. The necessary implementation in nano-fabrication techniques was introduced by e-beam lithography which was made available during 1985-2005 [9-11].

2.1 Technological Survey of SET logical Synthesis

The research on SET have stimulated in two distinctive paths; (i) Fabrication of SET using newer, sophisticated and cost effective technologies and (ii) Implementing SET technology in real life application i.e., application of SET. The fabrication technique of SET has been extensively explored as most of the Researchers employed their efforts in it and consequently several modern techniques have been reported so far [12]. But the later way of research i.e., implementation of SETs to create SEDs for real time circuit realization is still lagging far behind. Although application of SED is a rising field of low dimensional structures that has opened a new horizon for present and future device application and this is now an established fact. Some SET made devices have already matured into commercially useful products. Many SET built circuits now require extensive research to be commercially viable in near future. Thus it is a high time to initiate broader research related to application areas of SET such as Logic Gates, Memories and many more.

Owing to such considerations Researchers and Scientists all over the world emphasize in designing new SET based devices and as a result thousands of single-electron transistor (SET)-based logic schemes have been reported so far although the fact is that comparatively negligible amount of the proposed single-electron logic cells have been established experimentally. Kim et.al, demonstrated silicon-based single-electron logic circuits combining with FET to incorporate in post CMOS era [13]. The up rise of SEDs, so far proposed in the literature include single electron memories [14,15], dot-based cellular automata [16, 17], binary decision devices [18], inverters [19], pumps [20], majority gates [21], analog to digital converter [22], logic gates [23], single electron latches and buffers [24].

3. SET in Choosing Policy like Decision Making Sub-system – A Case Study

The SETs as discussed earlier are elements of nanometer scale electronic circuits because they can detect the motion of individual electrons and hence can be made very small. Herein the authors present a very complex and critical issue of choosing a policy as a decision making sub-system with a set of requirements under which an insurance policy can be taken. Let us consider that the applicant must be –

1. A married female 25 year old or over (x), or
2. A female under 25 years (z) or
3. A married male under 25 who has not been involved in a car accident or
4. A married male who has been involved in a car accident (w) or
5. A married male 25 years or over who has not been involved in a car accident (y)

Considering all the pre-conditions the authors here demonstrate the SET based above stated decision making sub-system using Monte Carlo based SIMON software. The critical issues involved during designing were positioning the basic elements at the nearest level without any interference of the other elements. For the sake of simplicity we have confined ourselves in only 5 conditions although more conditions could be added to it further.

3.1 Modeling the Decision Making Sub-system Using SET and Resultant Waveform for Optimization

The circuit realized in Fig.1 is capable to decide the policy taking steps and the same decision-making sub-system can be integrated into a nano-scaled IC which can be fitted to any present day available real life products. The resultant waveforms are enunciated in Fig.2.

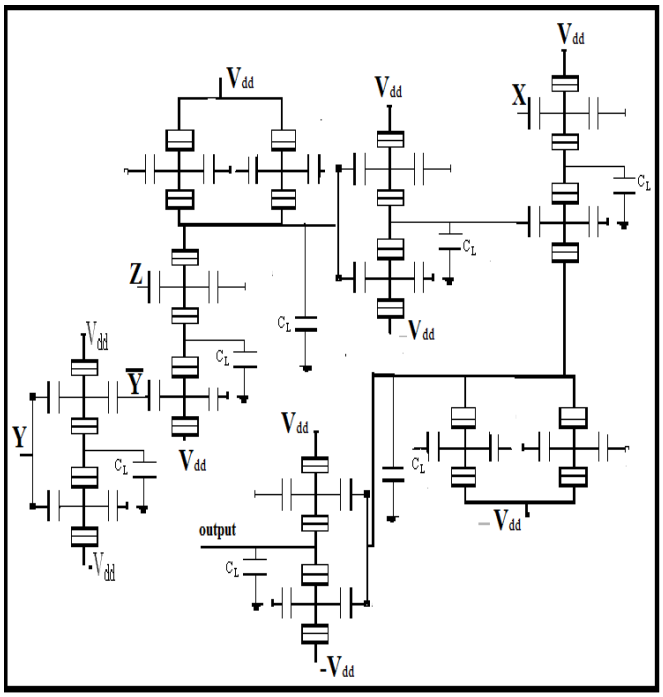

Figure 1: SET Modeling for Policy Choosing

The transportation of electrons from input to output is manipulated by the intrinsic properties of SED itself at different clock intervals with the incorporation of input signals and subsequently the propagation delay is controlled to minimize the power consumption and power dissipation of the proposed architecture. Simultaneously the integration density of this model is quite high. Moreover, its robustness

Licensed Under Creative Commons Attribution CC BY

and high speed performance deliberately increases its acceptability for nano IC configuration.

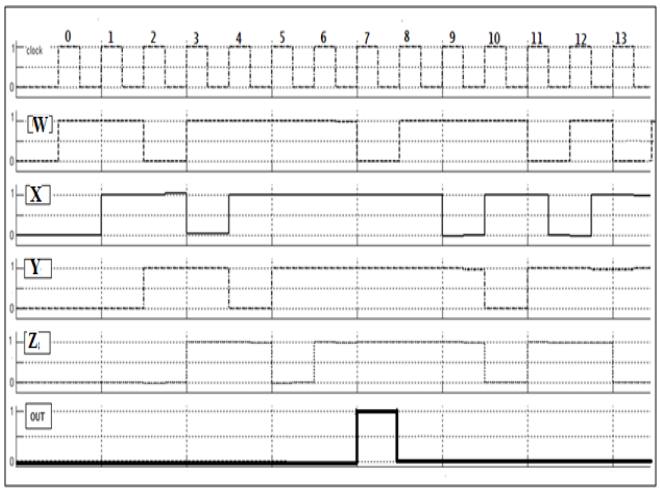

Figure 2: Partial Waveforms for Policy Making Decision Sub-system

From the waveform it is consequently revealed that the best condition to choose a policy will encapsulate at least three dissimilar successive conditions. Thereby, the modus operandi to choose the best policy will sufficiently be broad enough to adjust all possible pre conditions. And all these can be achieved without any expert's counseling. Thereafter, the common man's complex issue can be dealt quite easily and undoubtedly it would be much less time consuming.

3.2 The Physical Limitations of Implementing SET for Policy Making Decision Making Sub-system

As SETs are considerably made smaller, there is an increase in operating temperatures, in operating frequency as well as in device packing density. However, some of the circuit architectures that have been proposed for SEDs are basically copies of the semiconducting architectures which require SETs with voltage gain. Because of this limitation of SETs, it now seems that it has to go under extensive research before commercially designing a SET based dense integrated circuits using the existing technology. SETs have high output impedance and are sensitive to random background charges. This makes it unlikely that SETs would replace FETs in applications where large voltage gain or low output impedance is necessary [25-28] in very near future. The real problems preventing the use of SETs in most applications are the (i) low gain, (ii) the high output impedance and (iii) the background charges. Besides this, the CMOS devices are trustworthy as they can compensate for the drawbacks of SETs; thereby the Hybrid CMOS-SET architectures that combine both SET and CMOS devices are the best alternatives to the problems of SET mentioned above.

4. Hybridization of CMOS-SET and Modeling the Same Decision Making Sub-system

SEDs, with the present day known best lithography techniques, cannot fully overcome the physical limitation of poor current driving capabilities and lack of room temperature operation. Until a triumph over the fragilities of SETs, in near future is achieved, complete replacement of MOSFET by SET is not possible. Instead, CMOS is compensated with high voltage gain, high driving speed and also high input impedance. Other merits of existing and highly proficient as well as much matured CMOS technology are – a well developed e-beam lithography based fabrication technology and ample research studies with empirical results are available. Thus a profound prospect to adapt hybrid CMOS-SET to recompense the intrinsic drawbacks of SET can pay heed both in academics and industry. And so the unconventional revelation to assemble the circuit in hybrid structure by a combination of SET and conventional devices like CMOS for VLSI and ULSI circuits is gaining recognition. Hybridizing CMOS-SET can bring out new functionalities, which are not represented in pure CMOS or SET technology. Toshiba successfully empirically demonstrated the act of a hybridizing MOS-SET inverter on a SOI wafer [29, 30] with improved gain at transition levels however the current drive remained low. Such a co-integration methodology can move smoothly the sudden transformation of technology from CMOS to SET [31, 32]. Here again the authors bore the pain to incorporate this new technology in decision making sub-system of choosing a policy. Fig. 3 below that articulates the hybrid model of the same circuit of Fig. 2, have two basic differences with the above designed SET model, i.e., (i) the 'Pull Up' transistor is an SET and (ii) the V_{DD} is defined by the SET device parameters. Researchers at Delft University in Netherlands wee the first to recommended a SPICE simulation package for SET circuit [33] using the Orthodox theory of SET that can be incorporated for hybrid CMOS-SET optimization. The authors here adhere to the SET-MOS quaternary transmission gate [34]; the same is highly ascribed and mostly cited in reputed journals [35]. The co-integration model of policy choosing decision making sub-system were designed and further simulated on this above cited SPICE soft-computing layout which allows place sharing of SETs with the conventional MOS devices in one particular die area as elucidated in Fig. 3.

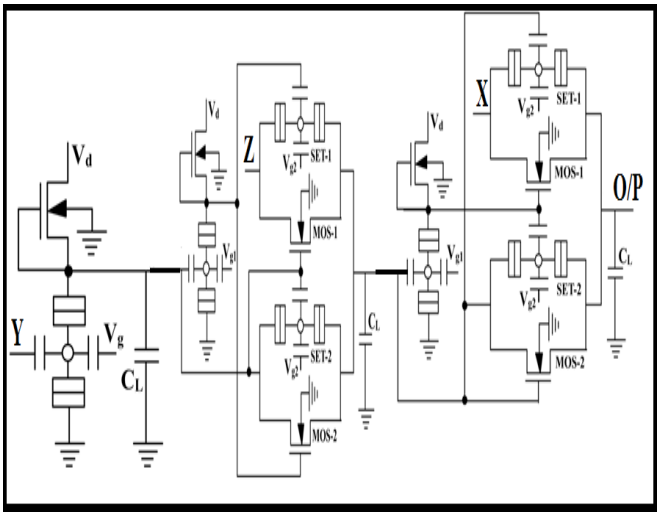

Figure 3: Hybrid CMOS-SET Modeling for Same Policy Choosing Decision Making Sub-system

For thoroughgoing exposure of the proposed sub-system and also for convenience, the logic operations of the proposed circuit were sequentially tested by simulation using T-Spice

Licensed Under Creative Commons Attribution CC BY

simulation software. Subsequently, MIB compact model for SET device and BSIM4.6.1 model for CMOS was amalgamated to obtain detailed experiential upshots. The resulted waveforms are attached in the following (Fig .4).

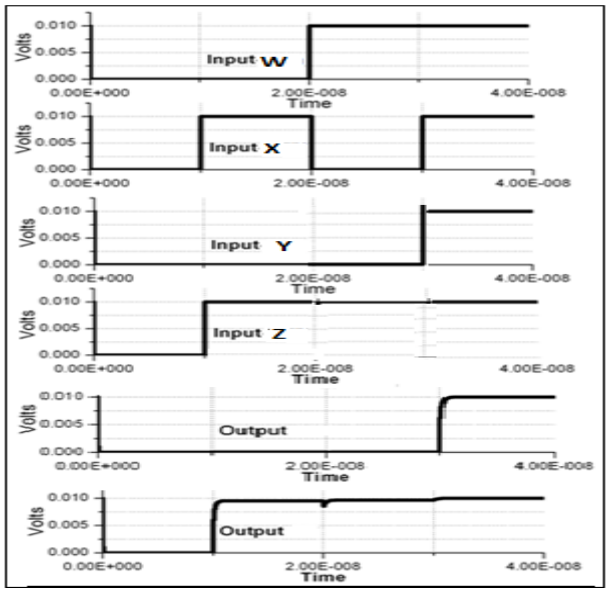

Figure 4: Resultant Waveform of the Hybrid Model

5. Comparative Analysis of Both Models

Both the proposed model showed no errors in performing the decision making operations, but the two distinctive drawbacks of SED designed model was counteracted. Likewise, the power consumption ratio & propagation delays when equated to CMOS technology were found quite fewer in hybrid CMOS-SET technology. Table-I below indicates only the approximated estimated values of power consumption of the decision making sub-systems employed in these two circuits. The output voltage gain is almost 4.8 as obtained from the drop of the transitional regions. The present projected conception of hybrid CMOS-SET decision making sub-system architecture shows gratification in trade-off between CMOS and SET.

Table 1: Partial Comparative Study of Both Models

Power Supply	No. of CMOS	No. of SET	Power Consumption
0.01V	3	3	1.02E-09 W
0.01V	3	3	1.02E-09 W

6. Future Scope

The design methodology creates ample scope for a new horizon in the field of nanotechnology incorporation for modeling decision making sub-systems. Furthermore, the speed and robustness is of greater value when compared to conventional pure CMOS systems. Apparently, such models are expected to hit the market in very near future.

7. Conclusions

The design and simulation of two distinctive but co-related nano scale technologies i.e., SET and hybrid CMOS-SET decision making sub system is modeled categorically and the results are acquired emphatically to render the underlying potential of both the models. The results of SET based model showed absolute gain over conventional CMOS technologies. Apparently such systems should be considered as the successor of age old CMOS conventions. But the inherent physical limitations as well as fabrication limitations have hardened its accomplishment. Therein the approach of hybridizing CMOS-SET smoothens the pave way for SET in near future. Beside others, one incredible feature of hybrid decision making model is that the SET and CMOS were positioned in series and in this manner if the hybridization is achieved, it is anticipated that the result shows improved gain of the models and simultaneously the propagation delay decreases to some extent. Both the models was designed and implemented using sophisticated simulation software by means of empirical study to explore maximum flexibility which revealed that the switching speed, mobility and power dissipation shows enhanced performance, thereby increases the possibility to incorporate the same in next generation electronics.

8. Acknowledgement

The authors hereby acknowledge the technological and financial aid provided by the Camellia School of Engineering and Technology (CSET) of Camellia Group.

References

[1] K. K. Likharev : IBM J. Res. Devel., vol 32 , 144 , 1988
[2] Kawarabayashi, J.; Kadoi, T. ; Watanabe, K.-I. ; Uritani, A. ; Iguchi, T., “Single electron transistor for cryogenic detector read-out”, IEEE Nuclear Science Symposium Conference Record, 2001
[3] Morris, J.E. ; Wu, F. ; Radehaus, C. ; Hietschold, M. ; Henning, A. ; Hofmann, K. ; Kiesow, A., “Single electron transistors: modeling and fabrication”, 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.
[4] Teruhisa Matsui, Jun Kawarabayashi, Kenichi Watanabe and Tetsuo Iguchi, “Evaluation of Single-Electron Transistor as Nanoscale Thermometer for a Cryogenic Radiation Detector”, Journal of NUCLEAR SCIENCE and TECHNOLOGY, Supplement 6, pp. 73–77 September 2008.
[5] P. Hadley, G. Lientschnig, and M. Lai, “Single-Electron Transistors,” pp. 1–8.
[6] N. Asahi et al.: “Single-election logic systems based on BDD”, IEICE Trans. ED E-81-C, Jan 1998.
[7] T. Henning, "Coulomb Blockade Effects in Anodized Niobium Nanostructures", LANL e-Print Archive, cond-mat/9710037, October 1997.
[8] K. P. Hirvi, J. P. Kauppinen, A. N. Korotkov, M. A. Paalanen, and J. P. Pekola,: "Arrays of normal tunnel junctions in weak Coulomb blockade regime", Appl. Phys. Lett., vol. 67, pp.2096-2098.
[9] Daw Don Cheam ; Karre, P.S.K. ; Palard, M. ; Bergstrom, P.L., “Mass Production of Room Temperature Single Electron Transistors using Step & Flash Imprint Lithography and Lift-Off Technique”, 8th IEEE Conference on Nanotechnology, 2008. NANO '08.

Licensed Under Creative Commons Attribution CC BY

[10] Yaqing Chi ; Bingcai Sui ; Liang Fang ; Zhou Hailiang ; Haiqing Zhong ; He Sun, "A compact analytical model for multi-island single electron transistors", IEEE 8th International Conference on ASIC, 2009. ASICON '09.
[11] Haiqin Zhong ; Yaqing Chi ; He Sun ; Chao Zhang ; Liang Fang, "Macromodeling of realistic single electron transistors for large scale circuit simulation", 3rd International Nanoelectronics Conference (INEC), 2010
[12] Dae Hwan Kim ; Suk-Kang Sung ; Kyung Rok Kim ; Jong Duk Lee ; Park, Byung-Gook, "Single-electron transistors based on gate-induced Si island for single-electron logic application", IEEE Transactions on Nanotechnology,2002.
[13] S.J. KIM et al., "SINGLE-ELECTRON LOGIC CELLS AND SET/FET HYBRID INTEGRATED CIRCUITS", JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.6, NO.1, MARCH, 2006
[14] K. Yano, T. Ishii, and T. Sano, "Single-electron memory for giga to tera bit storage', Proc. IEEE 87, pp. 633-651, 1999.
[15] B. H. Lee and Y. H. Jeong, "A Novel SET/MOSFET Hybrid Static Memory Cell Design", IEEE Trans. On Nanotechnol, vol. 3, no. 3, pp. 377-382, 2004.
[16] C.S. Lent and P.D. Tougaw, "Dynamic behavior of quantum cellular automata", J. Appl. Phys., vol. 80, pp. 4722-4736, October 1996.
[17] Nan-Jian Wu, Noboru Asahi and Yoshihito Amemiya, "Cellular-Automaton Circuits Using Single-Electron-Tunneling Junctions", Jpn. J. Appl. Phys. 36, pp. 2621-2627, 1997.
[18] N. Asahi, M. Akawwa, and Y. Amemiya, 'Single-electron logic devices based on the binary decision diagram device', IEEE Trans. Electron Devices, 44, pp. 1109-1 116, 1997.
[19] C. P. Heij, P. Hadley and J. E. Mooji, "Single-electron inverter", Appl. Phys. Lett., vol. 78, no. 8, pp. 1140-1142, 2001.
[20] T. Altebaeumer and H. Ahmed, "Silicon nanowires and their application in bi-directional electron pumps", Microelectronic Engineering, vol. 57-58, pp. 1029-1033, 2001.
[21] T. Oya, T. Asai, T. Fukui, and Y. Amemiya, "A majority-logic nanodevice using a balanced pair of single-electron boxes", Journal of Nanoscience and Nanotechnology, vol. 2, no. 3/4, pp. 333-342, 2002.
[22] S. J. Ahn and D. M. Kim, "Asynchronous analogue-to digital converter for single-electron circuits", Electron Lett., vol. 34, no. 2, pp. 172-173, 1998.
[23] I. Tsimpetidis, I. Karafyllidis, and A. Thansilakis, "A single-electron three input AND gate", Microelectron. J., 33. pp. 191-195, 2002.
[24] T. Oya, T. Asai, and Y. Amemiya, "Single electron logic device with simple structure," Electronics Letters, vol. 39, no. 13, pp. 965-967, 2003.
[25] Eugene S Soldatov, Vladimir V Khanin, Artem S Trifonov, Sergei P Gubin, V V Kolesov, D E Presnov, S A Iakovenko, G B Khomutov and A N Korotkov, "Room temperature molecular single-electron transistor", Eugene S Soldatov et al 1998 Phys.-Usp. 41 202.
[26] Y. Takahashi, et. al, "Silicon single-electron devices," Journal of physics: Condensed matter, pp.R995-R1033, 2002.
[27] K. Yano, et al, "Room-temperature single-electron memory," IEEE Trans. On Electron. Dev,. Vol. 41, pp. 1628-1638, Sept. 1994.
[28] S. Tiwari, et al, " A silicon nancrystals based memory," Appl. Phys. Lett., vol. 68, pp. 1232-1234, Aug. 1996.
[29] Uchida, K., et al., "Programmable Single-Electron Transistor Logic for Low-Power Intelligent Si LSI," Proc. of. ISSCC2002, Vol. 2, pp. 162–453
[30] Uchida, K., et al., "Programmable Single-Electron Transistor Logic for Future Low-Power Intelligent LSI: Proposal and Room-Temperature Operation," IEEE Trans. Elec. Dev., Vol. 50, No. 7, pp. 1623–1630, 2003.
[31] Ziegler, M. M., and M. R. Stan, "A Case for CMOS/Nano Co-Design, "Proc. of. ICCAD 2002, pp. 348–352.
[32] Hutchby, J. A., et al., "Extending the Road Beyond CMOS," IEEE Circuits and Devices Magazine, Vol. 18, No. 2, 2002, pp. 28–41.
[33] G.Lientsching, I.Weymann and P.Hadley "Simulating Hybrid Circuits of Single Electron Transistors and Field Effect Transistors" – Japanese Journal of Applied Physics, vol. 42, pp 6467 – 6472, 2003.
[34] Santanu Mahapatra and Adrian Mihai Ionescu "Realization of multiple valued logic and memory by hybrid SETMOS architecture" IEEE transactions on Nanotechnology, Vol. 4, No. 6, November 2005.
[35] Jayanta Gope et. al., "Analytical Modeling of Hybrid CMOS-SET Based Moore and Mealy Logical Circuit", IPASJ International Journal of Computer Science (IIJCS), May 2014.

Author Profile

Prof. Jayanta Gope, B.E., PhD (Engg.) has completed his PhD in Nanotechnology from Jadavpur University and is presently associated with Camellia School of Engineering and Technology. His field of interest includes Nano device modeling, Single Electronic devices, Spintronic Devices, Hybrid CMOS-SET. He has already published several international research articles in this category.

Prof. Aloke Raj Sarkar, B. Tech, M.E. (Electrical) from Jadavpur University is presently Faculty Member of Camellia School of Engineering and Technology. His research area is Sensor and Transducers, and nanotechnology, nano-sensors, and decision making sub-systems using nanotechnology.

Licensed Under Creative Commons Attribution CC BY