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Performance Analysis of Voltage Scaled Low Power Clock Distribution Network with Different Frequencies

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Abstract: ***Clock distribution networks forms an inherent part of any digital circuit. It use a large part of the total circuit power, which is not worthy. Different techniques are employed up till now to reduce the clock power. In this paper we have to demonstrate how clock power can be reduced significantly by distributing it at reduced supply voltage and analyse the power consumption of clock distribution network with different frequencies like 100 MHz, 200 MHz, 250 MHz, 400 MHz, and 1 GHz etc. The clock distribution network is designed and simulated in 180 nm technology. Achieving power reduction of about52%, 48%, 44%, 38%, 27%and26%respectively***.

Keywords: Low-power design, voltage scaling, clock networks, VLSI (Very Large Scale Integration)

1. Introduction

In synchronous digital circuits, clock distribution network is crucial part.The clocking networks consume large amount ofpower in some complex circuits around 20-50% of the whole circuit power, which is not worthy. If the clock power is reduce, it can reduce the total circuit power.The whole power dissipation in a clock network in any CMOS digital circuit, consists of three components: (a) leakage current (b) short circuit power and (c) dynamic power .The leakage current depends on its technology relatively negligible in clock circuit. Short circuit power occurs due to short circuit current through PMOS and NMOS transistors during logic changes, if we keep proper rise time and fall time throughout the clock network minimize the short circuit power component .The clock network has very high switching activity ,therefore dynamic power is the dominant factor of power consumption ,so leakage current and short circuit power are negligible. The dynamic clock power dissipation can be mathematically expressed by the relation

$$P=f\,C_L V_{DD} V_{SW} \quad (1)$$

where f is the clock signal frequency, C_L is the load capacitance ,V_{DD} is the supply voltage and V_{SW} is the output swing. If output buffer swing from GND to V_{DD}, then the equation of dynamic clock power becomes

$$P=fC_L V_{DD}^2 \quad (2)$$

Frequency scaling, voltage scaling, both voltage and frequency scaling or load capacitance scaling are used at different design abstractions to reduce dynamic power.

Supply voltage scaling has been the most adopted approach to power optimization, since it normally yields considerable amount of power savings due to the quadratic dependence of switching on supply voltage V_{DD}.Nowadays frequency is a fundamental parameter for the circuit, it cannot be change but its effects can be reduced by techniques like clock gating and obtain linear reduction in power consumption.If we reducing the load capacitance, which is consistent to achieve the minimal wire length and the minimal buffer powerdissipation.Reducing output swing of buffer without reducing supply voltage, which corresponds to a linear reduction in the power dissipation. According to this fact there are various techniques has been suggested for reducing clock distribution power

In[1] explain about VLSI scaling methods and low power CMOS circuits and these scaling methods are used to identify the effects of those scaling methods on the power dissipation and propagation delay of the CMOS circuit .In [2] suggest a new problem formulation for low power clock network design that takes rise time constraints imposed by the design into account and then obtain on significantly better result than previous approaches in terms of power dissipation and area. In [3],[4]discussing about reduced swing clock network and multiple supply voltage schemes for low power applications. In [5], [6] proposed voltage scaling and frequency as well as voltage scaling schemes for reducing power consumption and temperature fluctuations. In [7] describe a buffered H-tree topology technique to distribute the clock signal and to de-skew a clock network .In[8] proposed a half swing clock distribution scheme that allows them to reduce power consumption of clocking circuitry as 76%, because all the clock signal swings are reduced to half of the supply voltage

In Section 2 contains the proposed system and in Section 3 the test setup used for clock distribution network in section 4 describes clock distribution circuits used for analysis and simulation**.** The experimental results are shown in Section 5. Finally, concluding remarks are made in Section 6

2. Proposed System

In this work we have used the idea of supply voltage scaling technique for reduce power consumption in clock distribution network. To analyse and compare the performance of clock network with scaled supply voltage and without scaled supply voltage on power dissipation,

used two methodologies ie,Case1 and Case2.In Case1 Clock signals are distributed with full scale supply voltage and in Case2 Clock signals are distributed with reduced supply voltage and converted to full scale supply by using some level converters.

3. Test Setup for Clock Circuit

The main objective of this work is to analyse and compare the power consumption in two clock networks, (a) clock signals are distributed with full scale supply voltage to load and (b) clock signals are distributed with scaled supply voltage.Fig.1 and Fig.2 are shown the setup used for clocknetworks. Case1 is shown in Fig.1 i.e. clock signal is distributed with full scale supply voltage. Most of the clock distribution networks are using H-tree topology for distributing clock signal thought circuit as it reduce the effect of clock skew. Here we took a portion of such H-tree type clock distribution network, which has two loads in the form of D latches, namely DL1(D latch1) and DL2(D latch2).Assume the first load DL1 is nearer toclock source so there is only negligible amount clock skew. But the second load DL2 is far from clock source, since long interconnect length clock skew will be present. During the simulation of such clocking circuit clock skew is made as the form of Resistance Capacitance (RC) network between DL2 and clock source.

The clock distribution network in Case2 is shown in Fig2, here the clock load which is far from clock source i.e. clocking signal to DL2 is distributed with reduced supply voltage for interconnect power reduction .Supply voltage of clock signal is reduced by using H.L.L.C (High to Low Level Converter) at clock source and converted back to original form by using L.H.L.C (L.H.L.C) at clock load. The clock load which is near to clock source, i.e. clock signal to DL1 is distributed with full scale supply voltage, means the supply voltage of clocking signal to DL1 is not reduced. Here the clock distribution circuits are designed simulated in 180nm technology with 1.8V supply. The clocking signal is given to DL2, i.e.the clock load which is far from clock source is reduced to 1.2V for interconnect power reduction. This reduced value of supply voltage as 1.2V is due to design and operation of delay and power. In order to convert1.8V to 1.2V by using H.L.LC(High to Low Level Converter) shown in Fig.3.The reduced voltage ,ie.1.2V converted back to original form by using L.H.L.C(Low to High Level Converter) Shown in Fig.4

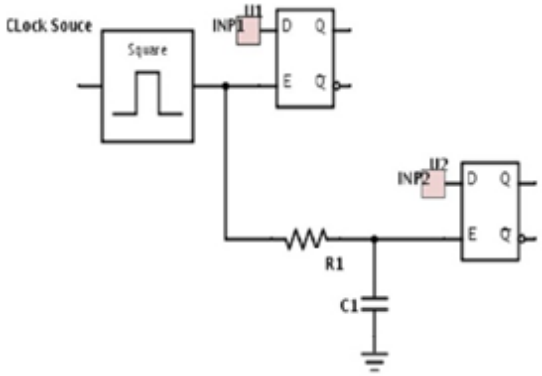

Figure 1: Test setup of clock distribution network with full scale supply voltage

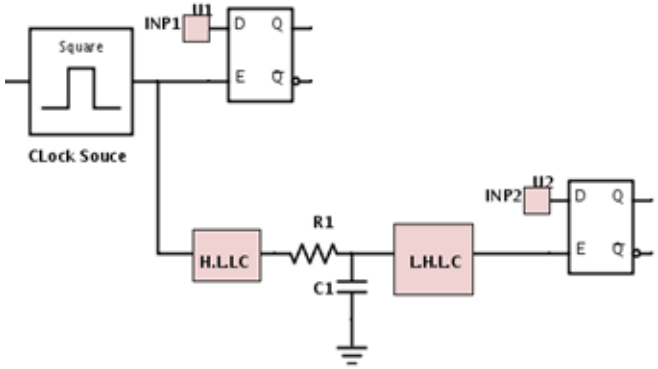

Figure 2: Test setup of clock distribution network with scaled supply voltage

4. Design of Clock Circuits (Case1 & Case2)

4.1. Case 1: Clock Distribution Network with Full Scale Supply Voltage

In Fig.1 shows the test setup of clock distribution network with full scale supply, here the clock source is used for generating clock signal with 1.8V ,since the loads such as DL1(D latch1) and DL2(D latch2) are operated on supply voltage with 1.8V.These two latches DL1 and DL2 are positive triggered D latches build by using transmission gates and inverters .The circuit of D latch is shown in Fig.3.Here these D latches are require clock signal as well as clock bar signal because D latches are constructed by using transmission gates. In order to develop clock signals we have to use two clock sources. One for clock signal generation and author for clock bar signal generation .The clocking signal which is distributed far from clock source, i.e. between clock source and DL2 have a skew of 40ps.Here this RC network is designed to give delay of 40ps with R=20Ω C=2pF

4.2. Case 2: Clock Distribution Network with Scaled Supply Voltage

In Fig.2 shows the test setup of clock distribution network with scaled supply voltage .The operation of this distribution network is also same like clock network with full scale supply voltage. Clockloads, i.e. D latches DL1 and DL2 are positive level triggered requires clock and clock bar signals for their operation. Two clock signals are generated by using two clock sources. Pair of clock and clock bar signals is directly given to DL1, i.e.the load which is near to clock source. Second pairs of clock and clock bar signals are reduced to appropriate voltage and given to DL2, ie, the load which is far from clock source. Here we have to use two H.L.L.C (High to Low Level Converter) and two L.H.L.C (Low to High Level Converter),one for clock signal and author for clock bar signal .Fig.4 shows high to low level converter for scale down the clock signal from clock source ,this is an inverter circuit with supply voltage of 1.2V.The low to high level converter circuit is shown in Fig.5,which is used for convert and restore back cock signal with full scale supply voltage at load DL2.Both the clock circuits are simulated at different frequencies for power comparison. While simulating at differentfrequencies, the high to low level converters are designed at every frequency in order to

maintain the nature of the clocksignals and also keeping in view low power dissipation

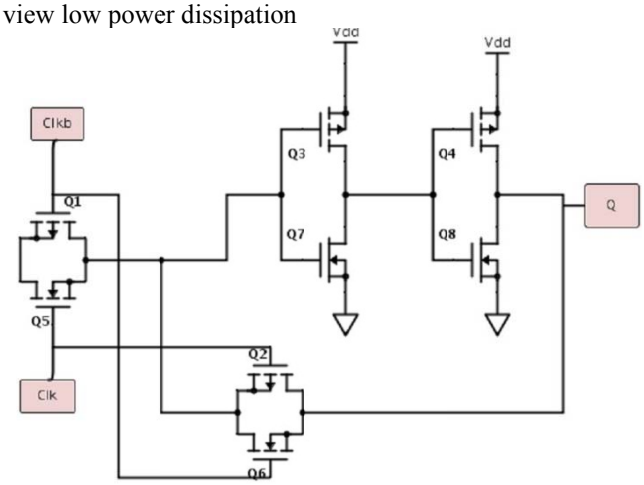

Figure 3: D latch

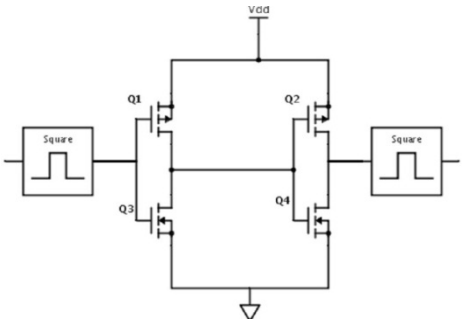

Figure 4: High to Low Level Converter

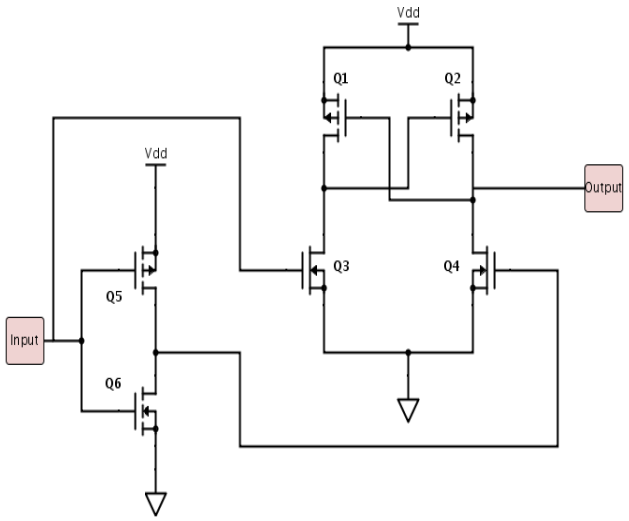

Figure 5: Low to high level converter

5. Results and Discussions

5.1. Case 1: Clock Distribution Network with Full Scale Supply Voltage

The clock network ,i.e. clock signal which is distributed with full scale supply is simulated with different frequencies such as 100Mhz, 200Mhz, 250Mhz, 400Mhz, 500Mhz and 1Ghz.Calculated the power dissipation of clocking network at each frequency.Fig.6 and Fig.7 demonstrated the simulation circuit and transient response of clock distribution network with full scale supply voltage. In Table1 shows power dissipation of clock network with different frequencies

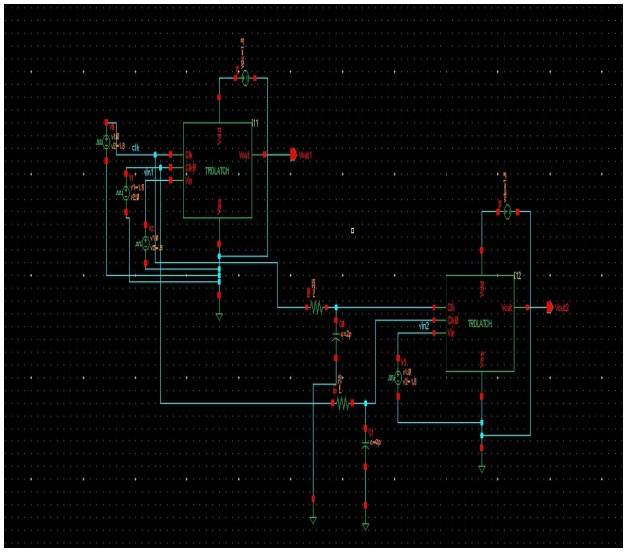

Figure 6: Simulation circuit of clock network with full scale supply voltage

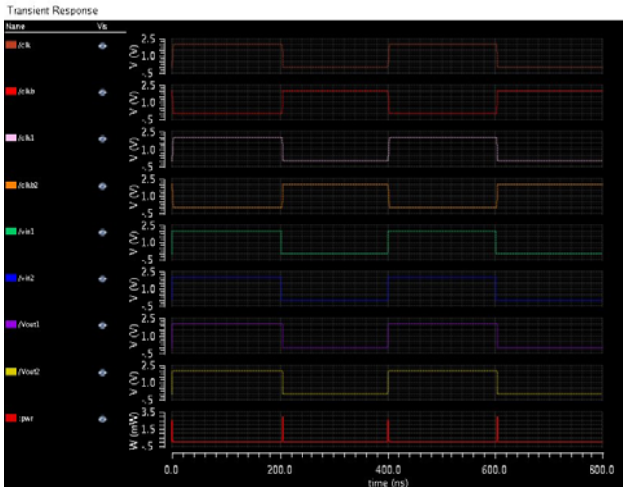

Figure 7: Transiant response of clock network with full scale supply voltage

Table 1: In Case1 power dissipation of clock network with different frequencies

Frequency	*Power dissipation in clock network with full scale supply*
100MHz	1.12mW
200MHz	2.684mW
250MHz	3.489mW
400MHz	5.895mW
500MHz	7.508mW
1GHz	14.75mW

5.2. Case 2: Clock Distribution Network with Scaled Supply Voltage

Here the clock network i.e. clock signal distribution with scaled supply voltage is simulated with same frequencies, which we used for simulation in clock network with full scale supply voltage. Such as 100MHz, 200MHz, 250MHz, 400MHz and 1GHz .Calculate the power dissipation of clock network with scaled supply voltage. Fig.8 and Fig.9 Shows the simulation circuit and transient response,Fig.10-

12 shows the circuit layouts of level converters and D latch.Fig.9 shows the transient response of clock signal with reduced supply voltage .Here the input signals to H.L.LC(high to low level converter) are clock signal of 1.8V which are reduced to 1.2V represented as sclk(scaled clock) and sclkb(scaled clock bar).This scaled signals are then passed through RC networks which are introduce clock skew of 40ps.After this scaled clock signals are reconverted to its full scale supply voltage of 1.8V using L.H.L.C(Low to High Level Converter)at load. In Fig .9,ie.transiant response shows the input signals(Vin1,Vin2) of D latches and its output(Vout1,Vout2) waveforms finally difference between clock signals from clock source(clk,clkb) and reduced clock signals (sclk,sclkb), delayed clock signals (dclk,dclkb) ,restored signals respectively.Table-2 shows the power dissipation of clock network at different frequencies

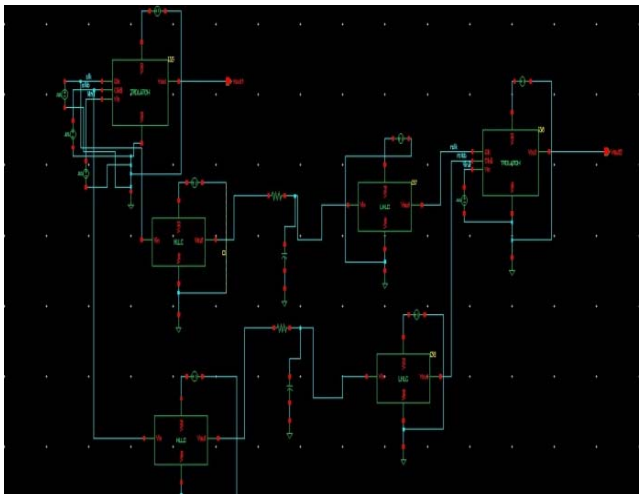

Figure 8: Simulation circuit of clock network with scaled supply voltag

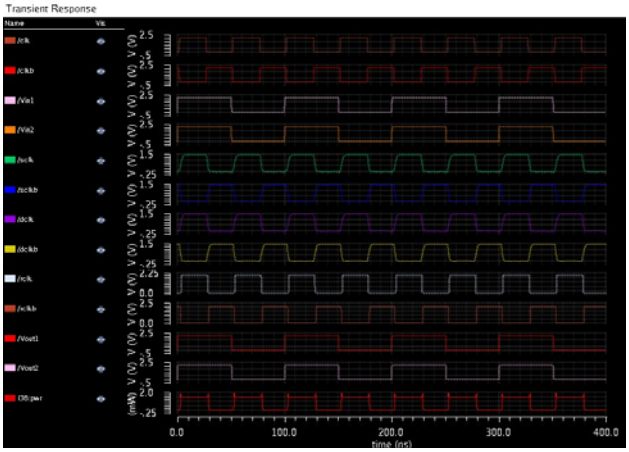

Figure 9: Transiant response of clock network with scaled supply voltage

Table 2: In Case2 power dissipation of clock network with different frequencies

Frequency	*Clock source power*	*H.L.L.C Power*	*L.H.L.C Power*	*Total clock power Dissipation*
100MHz	75.29 µW	25.48 µW	436.1 µW	0.53mW
200MHz	148.9 µW	40.41 µW	1.20mW	1.38mW
250MHz	276.5 µW	102.2 µW	1.55 mW	1.93mW
400MHz	900.9 µw	382.6 µW	2.34 mW	3.62mW
500MHz	1.79 mW	697.2 µW	2.97 mW	5.45mW
1GHz	3.90 mW	1.27 mW	5.68 mW	10.8mW

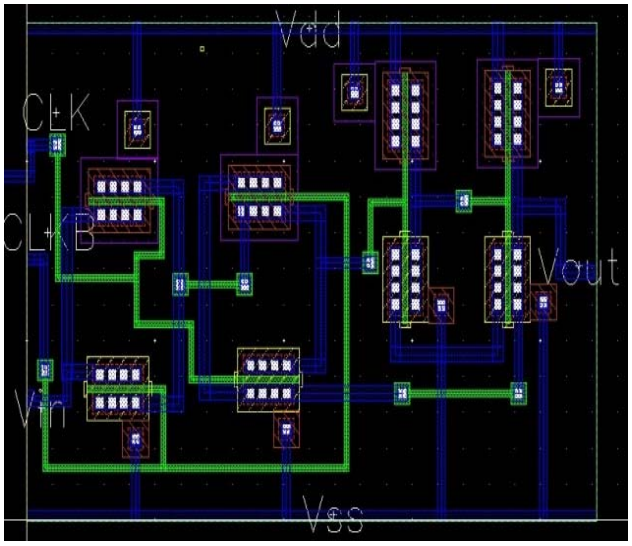

Figure 10: Layout of D latch

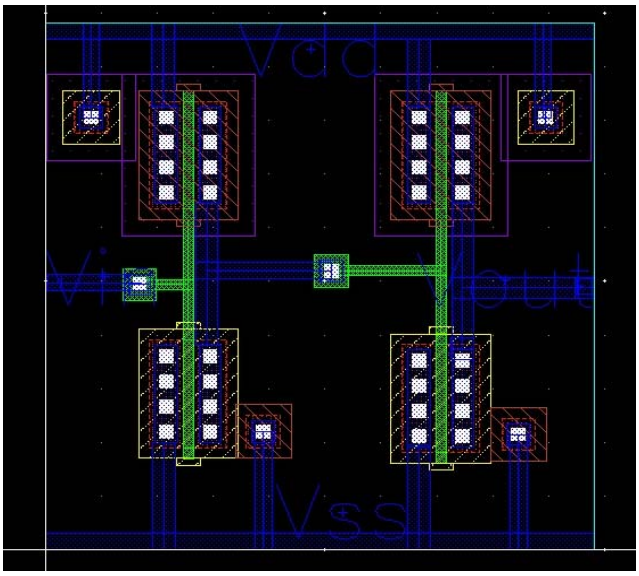

Figure 11: Layout of H.L.L.C

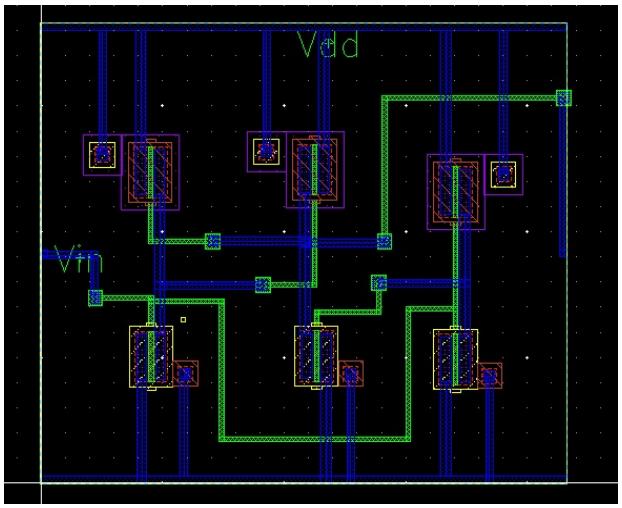

Figure 12: Layout of L.H.L.C

Compare the clock power dissipation in Case2, i.e. Clock distribution network with full scale supply voltage and Case1, i.e. clock distribution network with scaled supply voltage, we observed that a certain amount of power reduction in Case2 at each frequency is achieved.Table-3

shows the clock power dissipation and power reductiondue to supply voltage scaling in two clock networks such as Case1 and Case2 at different frequencies

From table-3 we can see that, if power dissipation inboth clock distribution network is compared there is a noticeable amount of power reduction in clock network with scaled supply voltage(Case2) as compared to clock network with full scale supply voltage(Case1).The main objective of designing such a clock distribution network was power reduction. The power dissipation of clock networks are reduced but a little amount of clock skew introduced due to level converters.

Table 3: Comparison of clock distribution power

Frequency	*Power*	*Power*	*Power*
100MHz	1.12mW	0.53mW	52.15%
200MHz	2.684mW	1.38mW	48.59%
250MHz	3.489mW	1.93mW	44.66%
400MHz	5.895mW	3.62mW	38.6%
500MHz	7.508mW	5.45mW	27.32%
1GHz	14.75mW	10.8mW	26.42%

6. Conclusion

In this brief, we compared the power dissipation in two clock distribution networks,i.e.clock distribution network with full scale supply voltage (Case1)and clock distribution network with scaled supply voltage (Case2) at different frequencies. In Case2 we achieved a significant amount of power reduction than Case1 at each frequency due to scaled supply voltage. Clock signals are reduced from 1.8V to 1.2V during clock distribution and converted back to full scale supply of 1.8V using level converters, such as H.L.L.C(High to Low Level Converter) and L.H.L.C(Low to High Level Converter).We can conclude from these results there is a significant amount of power reduction with supply voltage scaling.

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