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Design of Low Power Voltage Controlled Ring Oscillator Using MTCMOS Technique

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Abstract: ***In this paper, a parallel analysis of input and phase noise of ring oscillators subjected to MTCMOS technique by using different delay cells is presented. Based on this analysis oscillators that are tolerant to supply/ground noise can be identified and used for low noise oscillator design. MTCMOS techniques have been simulated and presented here which shows very drastic reduction in leakage power and noise. By using MTCMOS tech phase noise is 70 % reduced by using the Forward body bias tech and 78% reduced by diode based technique and 85-88% reduced by using SS-ULP diode based MTCMOS technique as compared to the base case when phase noise is measured for different delay cells at 45nm scale. A significant amount of leakage power has been reduced by using power gating scheme. Leakage power is reduced 72% by using the Forward body bias technology and 78% reduced by diode based trimode technique and approx 85% reduced by using SS-ULP diode based MTCMOS technique as compared to the base case measured for different delay cells at 45nm scale.***

Keywords: Phase noise, Ring Oscillator, MTCMOS, Delay cell etc.

1. Introduction

The Voltage controlled oscillators have a wider application in PLL (Phase Lock Loop) circuit that gives rise to the investigation of Ring VCO. Two most generally used VCOs are CMOS ring oscillator and LC tank based oscillators. Although the phase noise performance of LC oscillator is better but it consumes large layout of the circuit summed by combination of inductor and capacitor as compared to CMOS based oscillator circuits. The ring VCO has the greater performance over LC oscillator because of its low power and less area requirements but it more prone to noise viz. substrate noise and white noise as compared to LC oscillators yet its benefits cannot be avoided. So it is required to design the optimum performance ring VCO that has a good agreement between low power requirement and low noise circuit design. Ring oscillators are easy to tune and have wider tuning range that enables it to have a frequency in GHz range which makes its application domain wider that is WIFI and RF communication systems for the frequency translation and selection of channels. Due to their ease to integrate makes CMOS based ring oscillator as an essential building block in almost every large scale integration systems with large applications in battery operated mobile devices. A ring oscillator can be made of delay element along with the feedback path from output to input phase. At present many types of voltage controlled ring oscillators have been proposed using different types of delay cells including single ended delay cells, multiple-feedback loops and dual-delay paths. A single ended 5-stage ring VCO is shown in figure1:

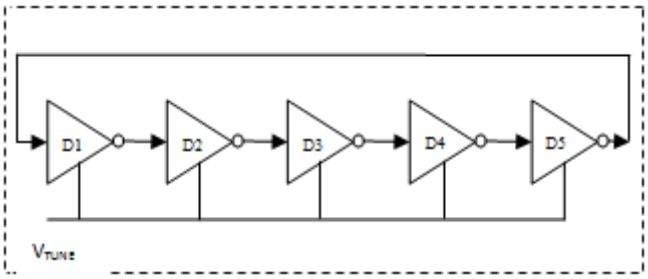


Figure 1: Five-stage cascaded Voltage controlled Ring oscillator

In present paper we have implemented the differential input delay cell based ring VCO. A comparative analysis has been done to study the noise and leakage performance of the ring oscillator design by using some of the most popular delay cells. The necessary condition for ring oscillator to oscillate is unity voltage gain provided that phase shift of 2π, which can be achieve by providing π/N phase shift followed by dc inversion. Assuming t_d is the delay of each stage the signal must go through each stage twice to achieve total period of $2Nt_d$. Single ended oscillator requires odd number of stages for dc inversion. Hence oscillation frequency of ring oscillator can be given as:

$$f = \frac{1}{2Nt_d} \quad (1)$$

Where N is the number of stages and t_d is delay of each stage.

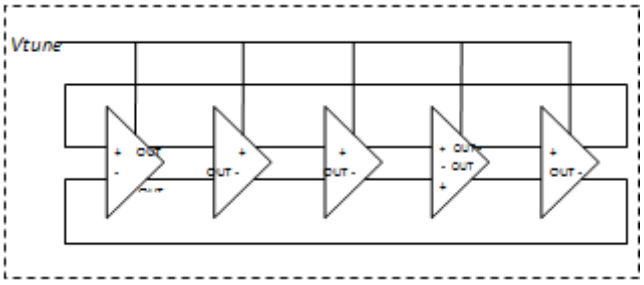


Figure 2: Five-stage differential voltage controlled ring oscillator

According to Barkhausen criteria the necessary but not sufficient condition for the oscillation is given by the following equations (3) and (4). Here we can see that overall magnitude of the feedback loop function must be equal to or greater than one and total phase difference must be equal to twice the multiple of π.

$$|A_1(j\omega).A_2(j\omega).A_3(j\omega) \dots \dots A_N \geq 1 \quad (2)$$

$$\angle A(j\omega) = \alpha = \arctan = \frac{2K\pi}{N} \quad (3)$$

Some major design matrix parameters of ring based oscillators include phase noise, large power consumption with the restriction of achieving highest operating and tuning frequency so a better agreement has to be between them to design optimum performance Ring oscillator. There are various sources of noise from various viz. white noises, supply and substrate noise etc. In VLSI circuit total Power consumption chiefly depends upon static power, dynamic power and leakage power consumption, Dynamic power consumption results from switching of load capacitance between two different voltage levels and also depends on the frequency of operation, whereas static power consumption depends on direct path short circuits currents between supply (VDD) and ground (VSS) and dependent on leakage currents. In a digital CMOS circuits main sources of power dissipation (P) can by the equation:

$$P_{avg} = P_{dynamic} + P_{static} = (P_{short} + P_{switch}) + P_{static} = I_{sc}V_{dd} + \alpha C_L V_{dd}^2 f + I_{leak}V_{dd} \quad (4)$$

The first term Pshort represents the power consumed during transient time gate voltage. In CMOS technology this is only related to the direct path short circuit current (Isc) which flows when both the NMOS and PMOS transistors are concurrently in active mode, conducting current directly from supply Vdd to ground or Vss. The second term, P switch represents the dynamic part of switching power due to charging and discharging total loading capacitance which is represented here by C_L, *f* refers to clock frequency and α is the average switching activity factor (typical value for α is 20% for logic blocks in 65 nm technology).The leakage power of the circuit is measured in the standby mode. It explained that how much power is wasted by the whole circuit. Leakage power is the product of the leakage current and supply voltage. The basic equation of leakage power is realized by Eq. (5).

$$P_{leakage} = I_{leakage} \times V_{dd} \quad (5)$$

Where, $I_{leakage}$ = leakage current, V_{dd} = supply voltage.

2. Circuit Description

Some of the most popular delay cells are described here. These are subjected to analyze on the basis of MTCMOS technology to achieve greater noise immune performance and reduced leakage power consumption in the design of Ring oscillator. Figure 3 represent the mane at is delay cell and Figure (4)-(5) represents the some other popular low noise delay cell. Symmetric load and self biasing feature of these delay cells makes them very useful in circuit design because they are very efficient in substrate and supply noise rejection.

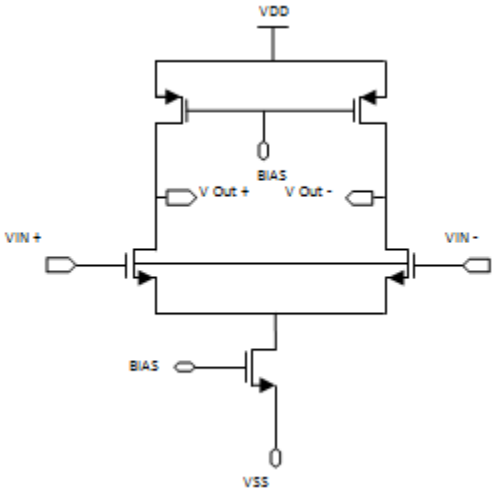


Figure 3: Delay Cell (A)

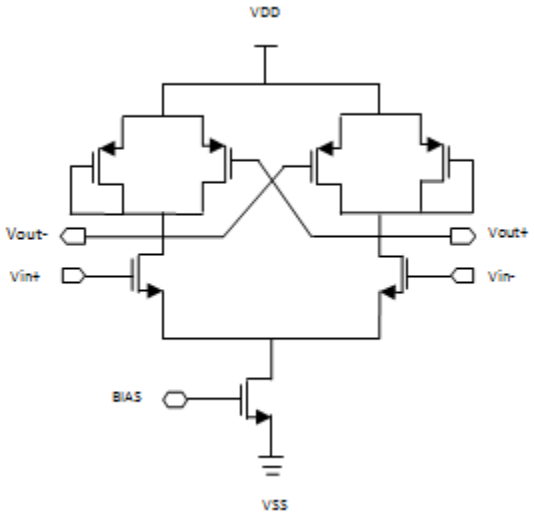


Figure 4: Delay Cell (B)

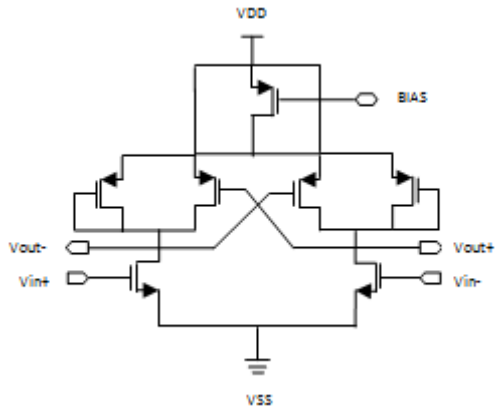


Figure 5: Delay Cell (C)

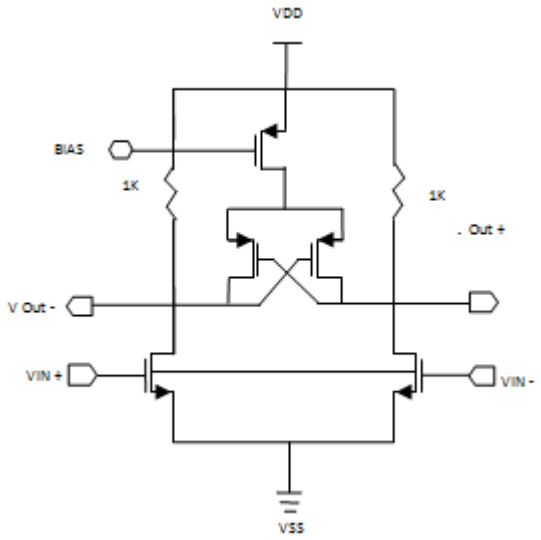


Figure 6: Delay Cell (D)

3. Design Implementation with MTCMOS Techniques

Different MTCMOS techniques are described in this section for reducing leakage current and to improve noise performance of the ring oscillator circuit. In this section, the description and analysis of some major MTCMOS technique has been done. These techniques are Forward Body Biased (FBB) MTCMOS, Diode Based Tri-mode MTCMOS, Ultra Low-Power Diode Based MTCMOS etc.

3.1 Forward body biased MTCMOS:

In this section, we design our circuit with Forward Body Biased MTCMOS technique for leakage current. In this technique high threshold transistors N_1, N_2 and P_1 are used to reduce a leakage current in standby mode effectively. Stacking of transistors N_1 and N_2 are used to reduce standby leakage current. An additional delay signal is introduced between sleep and active mode. So that discharging of ground voltage during a sleep-to-active mode is divided into two parts: sleep-to-wait and wait-to-active mode. Forward Body Biasing voltage (V_{BIAS}) is applied to voltage can reduce and more ground voltage is discharging during sleep-to-wait mode transition.

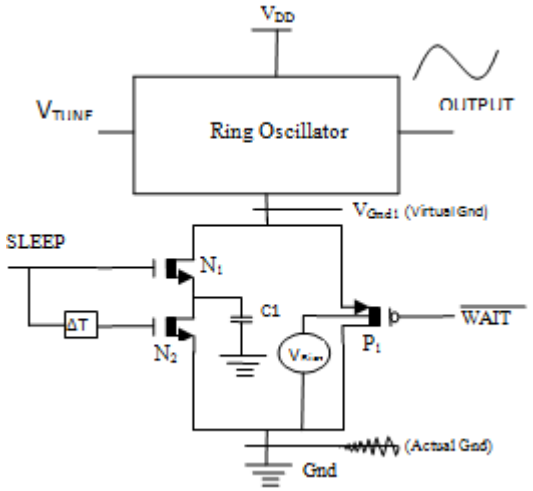


Figure 7: Forward Body Biased MTCMOS Technique

In standby mode sleep transistor N_1, N_2 and P_1 are turned OFF. The sub-threshold leakage current is shown below

$$I = Ae^{\frac{q}{n\,k\,T}(V_{GS} - V_{TH} + \gamma V_{BS} + \eta V_{DS})}\left(1 - e^{\frac{-q\,V_{DS}}{k\,T}}\right) \quad (10)$$

and

$$A = \mu_n C_{OX}\frac{W}{L}\left(\frac{K\,T}{q}\right)^2 e^{1.8} \quad (11)$$

Where, V_{TH} = threshold voltage, γ = body effect coefficient, η = DIBL coefficient, C_{OX} = Gate-Oxide capacitance, μ_n = mobility, V_{GS} = gate-to-source voltage, V_{BS} = bulk-to-source voltage, V_{DS} = drain-to-source voltage.

When sleep transistors (N_1, N_2 and P_1) are turned OFF in standby mode than the drain-to-source potential (V_{DS1}) of N_1 decreases, which results in less drain induced barrier lowering and negative body-to-source (V_{BS1}) of N_1 causing more body effect. In this way these stacking transistors are reduced the leakage current.

3.2 Diode based trimode MTCMOS:

In this section, we design our circuit with diode based Trimode MTCMOS technique. This technique consists of three parts:

- High threshold NMOS (N_1 and N_2) and high threshold PMOS (P_1) are used. Transistor N_2 is used as diode connected NMOS, which reduce the peak flicker noise.
- A wait mode is introduced between sleep-to-active mode transitions.
- Capacitor C_2 present between N_1 and N_2 to control the flow of drain current from transistor N_2 in mode transition.

In standby mode this sleep transistor (N_1, N_2 and P_1) will be turned OFF. This stacking transistor (N_1& N_2) will reduce the leakage current greatly. During mode transition, first stage (sleep-to-wait) turn ON the sleep transistor P_1 and sleep transistor N_1 and N_2 are turned OFF so that virtual ground voltage (V_{GND2}) will discharge. To complete the activation process, second stage (wait-to-active) turn OFF sleep transistor P_1 and sleep transistor N_1 and N_2 are turned ON. If the limited current is flowing through the sleep transistors then noise can further be reduced. A diode has a characteristic of current control. Diode current equation is:

$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right) \quad (12)$$

Where, I_S = diode reverse-biased saturation current, V_D = diode voltage, v_T = threshold voltage.

In Eq. (10), I_D decreases exponentially if we reduce V_D. Through this condition we control the drain current flow from sleep transistor, but this sleep transistor is not replaced by diode because of diode itself is not controllable. In practical circuit, if we connect drain and gate of transistor it works as a diode as shown in Fig.

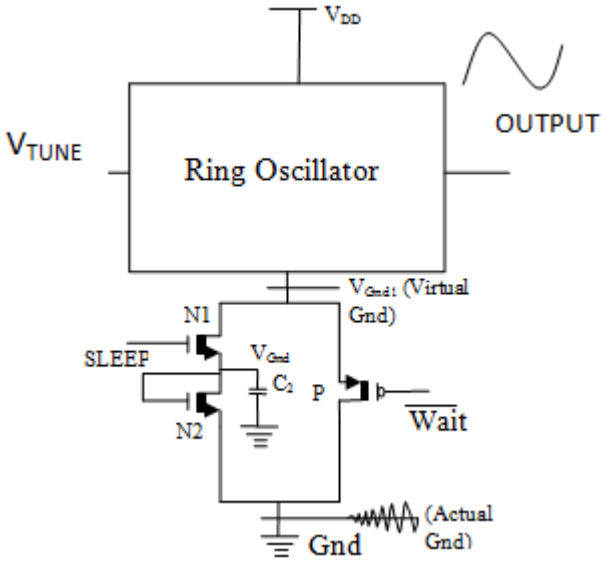


Figure 8: Diode Based MTCMOS Technique

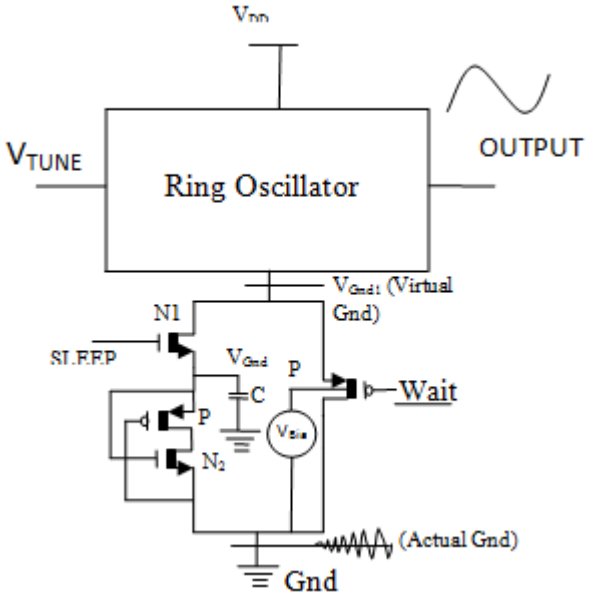


Figure 9: Ultra Low-Power Diode Based MTCMOS Technique

During wait-to-active mode transition, transistor N_1 is turned ON and capacitor C_2 starts charging. When capacitor C_2 will charge up-to threshold value of transistor N_2, now capacitor C_2 start discharging and transistor N_2 will turned ON ($V_{DS} = V_{GS}$). The drain current when transistor N_2 is turned ON is.

$$I_{D(N2)} = \mu_n C_{OX} \left(\frac{W}{L}\right)_{N2} \left[(V_{GS(N2)} - V_{TH(N2)})V_{DS(N2)} - \frac{V_{DS(N2)}^2}{2}\right] (13)$$

When $V_{DS} = V_{GS}$, then

$$I_{D(N2)} = \mu_n C_{OX} \left(\frac{W}{L}\right)_{N2} \left[\frac{V_{DS(N2)}^2}{2} - V_{TH(N2)}V_{DS(N2)}\right] (14)$$

Where, $V_{TH(N2)}$ = threshold voltage (N_2), C_{OX} = gate oxide capacitance, $V_{GS(N2)}$ = gate-to-source voltage (N_2), μ_n = mobility, $V_{DS(N2)}$ = drain-to-source voltage (N_2), W & L = width and length of transistor (N_2).

When, V_{DS} of sleep transistor is dropped then $I_{D(N2)}$ drops at quadratic manner (from Eq. (12)). So, dropping $I_{D(N2)}$ decreases voltage fluctuation at ground and hence ground bounce noise reduces.

3.3 SS-ULP DB MTCMOS

In this section we designed our circuit with Signal Stepped Ultra Low Power Diode Based (SS-ULP DB) MTCMOS technique. It consists of four parts:

- High threshold transistors (N_2& P_2) are used as Ultra Low Power Diode to reduce leakage current.
- Wait transistor P_1 (High-V_{TH}) is used to provide wait mode between mode transition (sleep-to-active).
- Capacitor (C_2) placed between sleep transistor (N_1) and P_2 to control the flow of drain current through transistor P_2 in mode transition.
- Forward Body Biased voltage (V_{BIAS}) applied to transistor P_1 which reduce its threshold voltage.

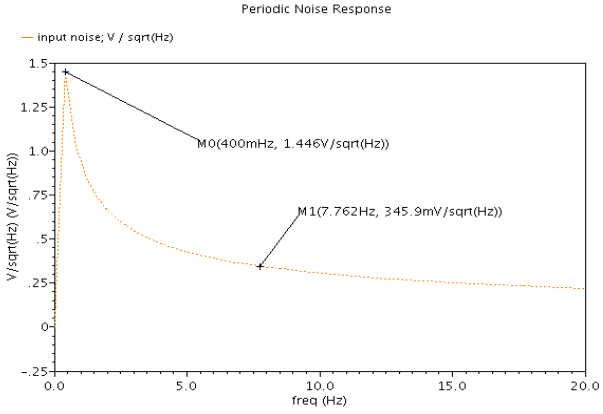
In standby mode, sleep transistors N_1, P_1, P_2 and N_2 are turned OFF. Due to present of Ultra Low-Power diode leakage current is greatly reduced. The mode transition is divided into two stages: sleep-to-wait and wait-to-active mode transition. In first mode (sleep-to-wait) transition, sleep transistor P_1 turned ON and sleep transistor N_1, P_2 and N_2 are turned OFF. Forward body biasing voltage (V_{BIAS}) applies to P_1 to reduce its threshold voltage without increasing the size and more voltage is discharge during this mode. In second mode (wait-to-active) transition, sleep transistor P_1 turned OFF and sleep transistor N_1, P_2 and N_2 are turned ON. Ultra low-power diode (P_2& N_2) reduces reverse current.

4. Result and Simulation

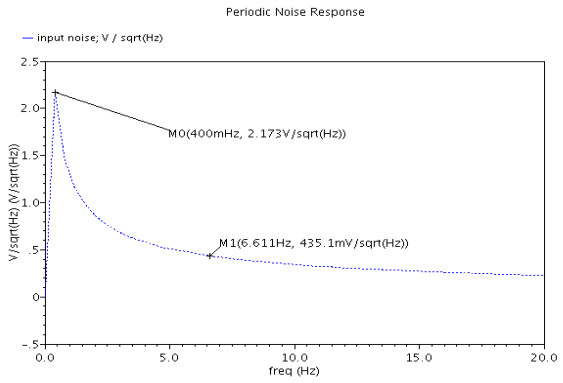
The results for different delay cells subjected to the well accepted MTCMOS technology for the design of ring oscillator are presented here.

4.1 Input Noise Analysis

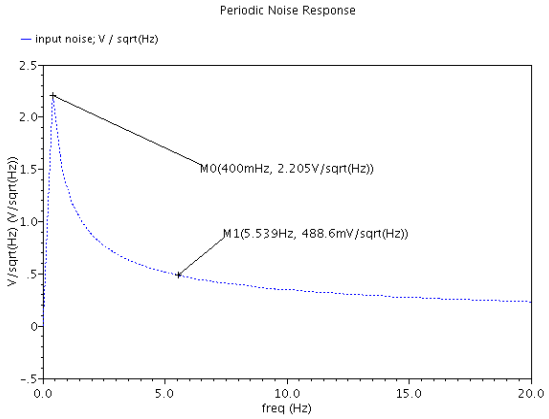
Input noise response of ring oscillator is shown in Figure 10(a), (b), (c) & (d) in which we can see that maneatis delay cell shows less input noise because its symmetric load and supply noise rejection and self biasing feature.



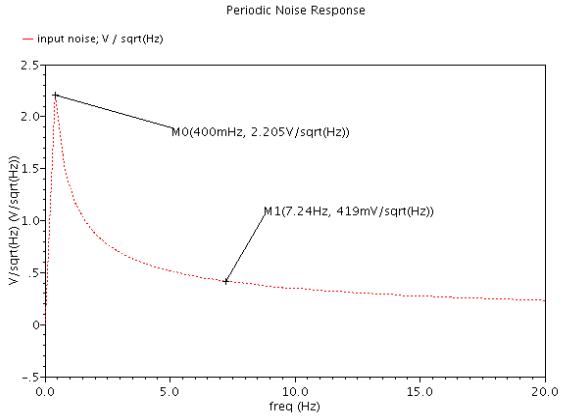
(a)



(b)



(c)



(d)

Figure10: Input noise response of Ring oscillator

4.2 Phase Noise Analysis

The phase noise of the ring VCO can be given by the impulse function and with the help of Lorentzian spectrum as given by the below equations. The phase shift per unit current for any oscillator is given by the following time dependant impulse function:

$$h_\varphi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \qquad (6)$$

Thus we can calculate the φ (t) as:

$$\varphi(t) = \int_{-\infty}^{\infty} h_\varphi(t,\tau) i(\tau) d\tau \qquad (7)$$

For the time up to t, φ (t) can be given as:

$$= \int_{-\infty}^{t} \frac{\Gamma(\omega_0\tau)}{q_{max}} i(\tau) d\tau$$

Now due due to white noise the single side band phase noise spectrum can be calculated as:

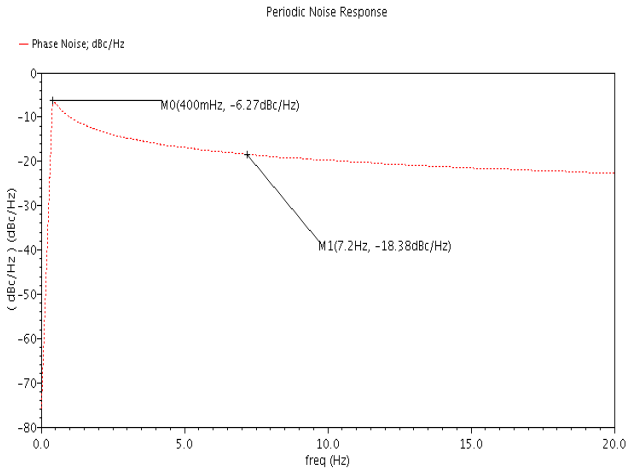
$$L(f_{off}) = \frac{\Gamma_{rms}^2}{8\pi^2 f_{off}^2} \cdot \frac{\frac{\overline{i_n^2}}{\Delta f}}{q_{max}^2} \qquad (8)$$

Where Γ_{rms} is root mean square value of impulse sensitivity function(ISF) and $\overline{i_n^2}/\Delta f$ represents the single side band spectral density of noise current source and it gives the total noise produced by individual sources and corresponding power spectral densities.

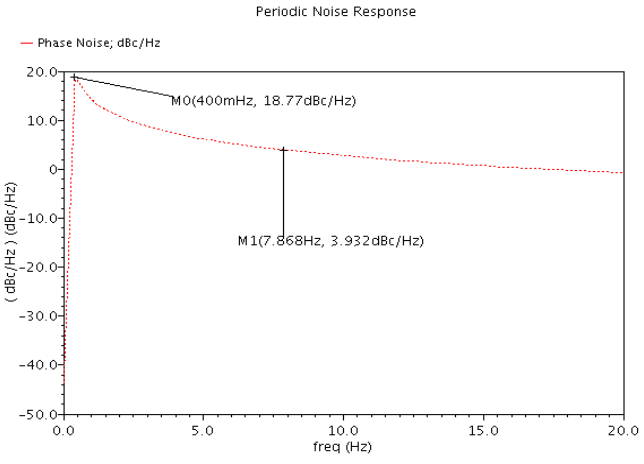
Phase noise can also be expressed as Lorentzian Spectrum as:

$$£(f) = \frac{1}{\pi} \cdot \frac{\pi f_{osc}^2 k}{(\pi f_{osc}^2 k)^2 + f^2} \qquad (9)$$

Where kis a scalar constant that describes the phase noise of the oscillator (in the absence of 1/*f* Noise and ignoring any noise floor).The Lorentzian spectrum has the property that the total power in £ from minus infinity to plus infinity is 1. This means that phase noise doesn't change the total power of the oscillator, it merely broadens its spectral peak. Phase noise of ring oscillator circuit using the delay cells shown in Figure (3)-(6)



(a)



(b)

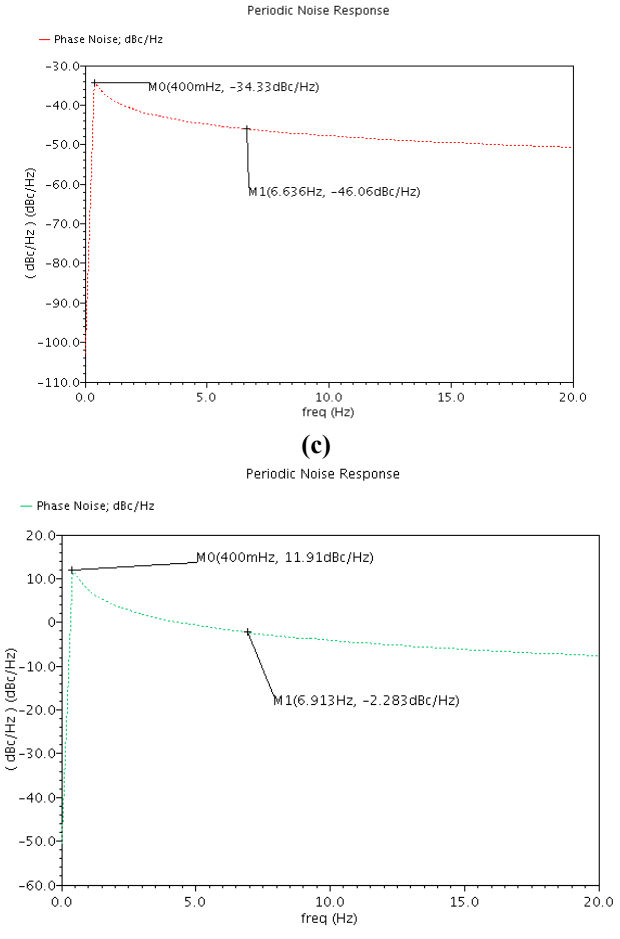


Figure 11: Phase noise response of Ring oscillator

Table1: Analysis and comparative study of ring oscillator according to phase noise.

Delay Cell	*Base case(db/Hz)*	*Fwd Body Bias MTCMOS (db/Hz)*	*Diode based Trimode tech(db/Hz)*	*SS-ULP DB MTCMOS (db/Hz)*
Delay cell-1	17.97	-15.67	-15.54	-7.963
Delay cell-2	18.77	-14.65	-19.34	-22.89
Delay cell-3	20.84	-7.963	-7.963	-34.33
Delay cell-4	21.78	-16.04	-12.43	-11.91

It can be seen from the table 1 that GBN is greatly reduced by using MTCMOS technique. This can be seen that phase noise is approximately 70 % reduced by using the Fwd body bias tech and 78% reduced by diode based technique and 85-88% reduced by using SS-ULP diode based MTCMOS technique as compared to the base case when measured for different delay cells at 45nm scale.

4.3 Leakage Power Analysis

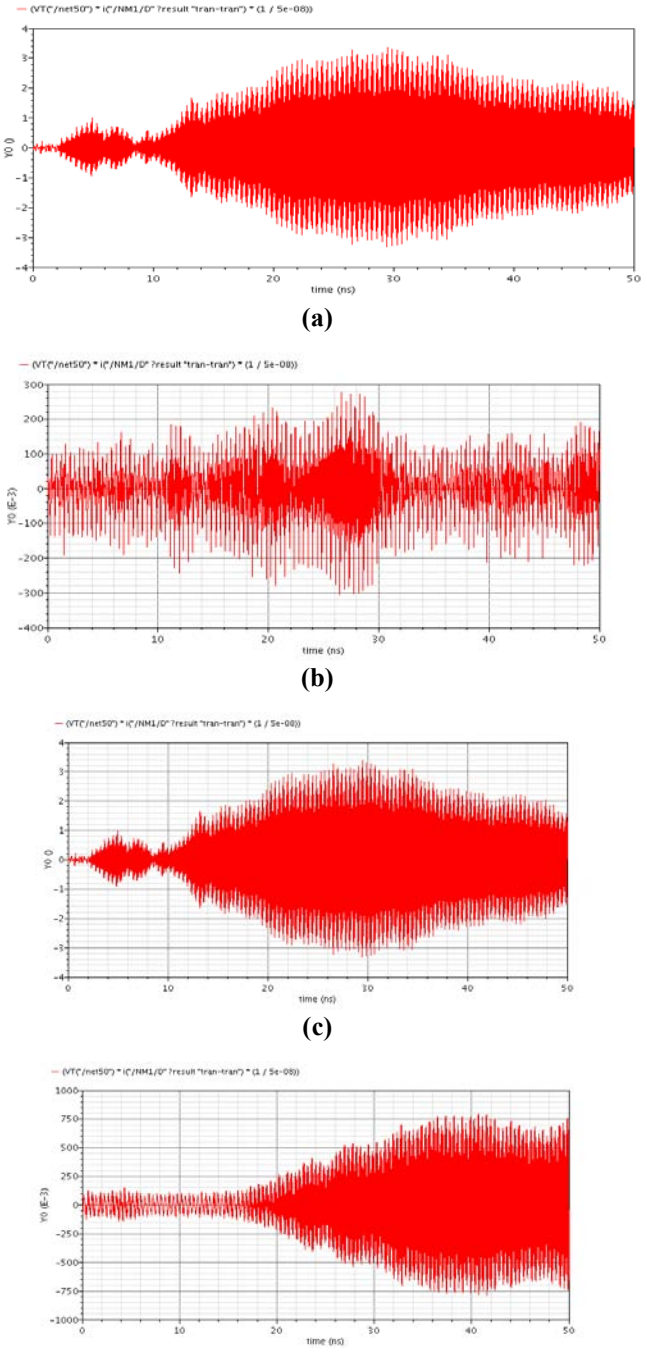


Figure 12: Avg. Leakage response of Ring oscillator

Table 2: Analysis and comparative study of ring oscillator according to leakage power

Delay Cell	*Base case(nW)*	*Fwd Body Bias MTCMOS*	*Diode based Trimode tech*	*SS-ULP DB MTCMOS*
Delay cell-1	8.872	2.23	1.97	1.24
Delay cell-2	8.923	2.09	1.96	1.27
Delay cell-3	8.818	2.13	1.95	1.34
Delay cell-4	8.761	2.41	1.99	1.38

It can be seen from the table 2 that a significant amount of avg. leakage power has been reduced by using power gating scheme. Leakage power is reduced 72% by using the Fwd body bias technology and 78% reduced by diode based

trimode technique and approx 85% reduced by using SS-ULP diode based MTCMOS technique as compared to the base case measured for different delay cells at 45nm scale.

5. Conclusion

A parallel analysis of input and phase noise of ring oscillators subjected to MTCMOS technique by using different delay cells is presented. Based on this analysis oscillators that are tolerant to supply/ground noise can be identified and used for low noise oscillator design. Phase noise expressions of CMOS ring oscillators are derived by using the impulse sensitivity functions. The effect of the different number of transistors and their topologies on the phase noise is analyzed using single ended differential ring oscillator. Phase noise due to substrate and supply noise and various other sources is discussed .Scope of reducing noise and reduction of leakage power due to various sources is discussed.

There are many other power reduction techniques like AVL, SVL, SAL, VTCMOS etc. Future scope includes using these techniques to mitigate the power dissipation and to conclude the best technique among these.

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