International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064

Modeling and Simulation of Single Stage Voltage Controlled Oscillator using Adaptive Voltage level Technique

Neeta Yadav[1], Nitin Saluja[2]

[1,2]Lingaya's University. Faridabad, Haryana

Abstract: ***A single stage source coupled CMOS voltage controlled oscillator is presented here using Adaptive voltage level technique (AVL) with the advancement of minimizing the power dissipation and generating rapidly high frequency of oscillation. The single stage VCO circuit has a low phase noise due to minimizing the noise sources. The voltage controlled oscillator is used in phase lock loop (PLL) as a frequency synthesizer to generate local oscillation frequency. Power dissipation is one of the most important performance parameter here, The Adaptive Voltage level techniques have applied in presented work mitigate the power dissipation. The simulation and performance analysis of proposed circuit is evaluated in Cadence virtuoso tool. In this simulator we use 45nm standard CMOS process technology. Simulation provides comparative study of different power reduction techniques on the basis of static and dynamic power. AVL technique provides 3.97fw static power and 38.02pw dynamic power for the 0.7v supply voltage at room temperature.***

Keywords: Voltage Control Oscillator; AVL; Power dissipation; Cadence Virtuoso

1. Introduction

Voltage controlled oscillator (VCO) [1]-[2]is a very critical component of PLL, voltage divider and other complex circuits which decides the power consumption and area taken by the PLL circuit [3]-[4]. As almost every circuit shows oscillatory behaviour, VCO comprises of a fundamental component in many RF transceivers and are commonly created with signal processing tasks like frequency selection and signal generation [5]. Now a day's RF transceivers have need of relay on phase locked loops (PLL) and programmable carrier frequencies to accomplish the same. These PLLs implant a less correct RF oscillator in a feedback loop, whose frequency can be proscribed with a control signal [6], [7]. Transceivers for wifi communication system have filters, low phase amplifiers, power amplifier, mixers, digital signal processing chips and PLL [8]. In communication systems, voltage controlled oscillators play significant role, specified that periodic signals requisite for timing in frequency translation and digital circuits in radio frequency circuits [9]. An ideal voltage controlled oscillator is a circuit whose output frequency is a linear function of its control voltage [10]. While practical oscillators exhibit periodically vary with time, this study is concerned with an electrical signal at a specific frequency. A conventional PLL circuit is made up of VCO, low pass loop filter, frequency divider and phase detector. The spectral purity of the PLL output depends heavily on that of the VCO [11]. Monolithic integration design of voltage controlled oscillators is desirable but always become most challenging task to be performed. The first requirement is to attain high frequency operation with reasonable power dissipation [12]. However, the most critical design constraint for the VCO is the phase noise performance. Finally small chip area is important to monolithic system integration. In modern electronics although LC tank oscillators have shown good phase performance with low power dissipation [13], [14] but there are some disadvantages, the tuning range of an LC oscillator is less in comparison to ring oscillators and secondly, the phase noise performance of oscillator chiefly depends on Q factor of on chip spiral inductors. To overcome this problem ring oscillator have used in recent year. The phase noise performance of ring oscillators is much poorer [15], at high oscillation frequencies; the power dissipation of ring oscillators may not kept low which is a key requirement for battery operated devices. To solve these complications, we work on single stage source coupled VCO without using an LC tank circuit [16]. Present work is done with major objective of reduced power consumption in design of VCO with different reduction techniques [8], [17]-[18]. Section 2nd shows basic operation and circuit description with different power reduction techniques. Simulation results have done on cadence tool in 45nm technology which is presenting in section 3rd. The conclusions will be summarized in section 4th.

2. Circuit Description

2.1 Single stage source coupled VCO

In the conventional ring oscillator design, two or more delay elements are employed to satisfy the Barkhausen oscillation criteria. On the other hand, to improve the oscillation frequency, the number of delay elements should be reduced. The suggested oscillator enhances the oscillation frequency by reducing the number of circuit stage to one. This property also lowers the power dissipation and improves the phase noise.

A single-stage source coupled voltage controlled oscillator circuit can be designed to dissipate less power than ring oscillator. The operation of the circuit described by figure 1, MOSFETs M1 and M2 act as switches, MOSFETs M3 and M4 pulled the output. The MOSFETs M5 and M6 behave as a constant current source. MOSFETs M2 is on and M1 is off, because the voltage of terminal 2 output (out2) is less than the terminal 1 output (out1), so the current in M4 is 2Id and capacitor will be changed by current Id, because M6 has id sinking current [19],[20]. When the voltage of Y and X capacitor terminal is same then capacitor is fully charged.

The figure 2 shows the layout of VCO ring oscillator. The current Id through C, cause point X to discharge down towards ground. When point X gets down, M1 and M2 turn off. VCO is combination of PMOS and NMOS circuit. PMOS and NMOS work in mainly in three regions, which are defined as.

$$I_D = 0 \quad (off: |V_{GS}| < |V_{TH}|) \quad (1)$$

$$I_D = k * \left(\frac{W}{L}\right)\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] (triode: |V_{DS}| \leq |V_{GS}| - |V_{TH}|) \quad (2)$$

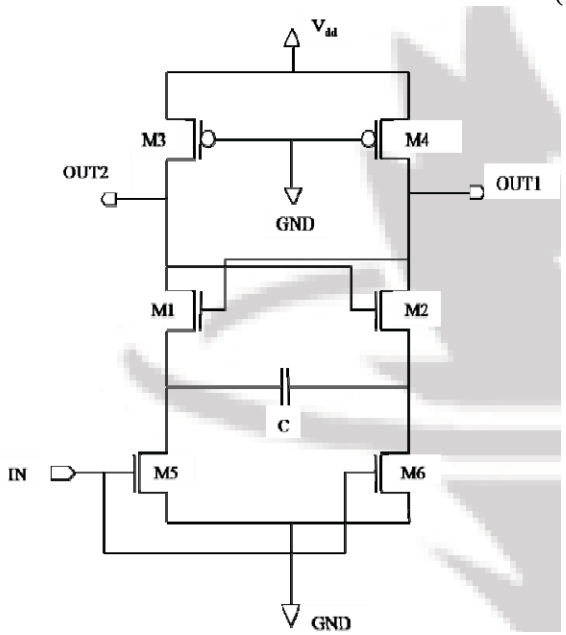


Figure 1: Circuit diagram of the single stage source coupled VCO

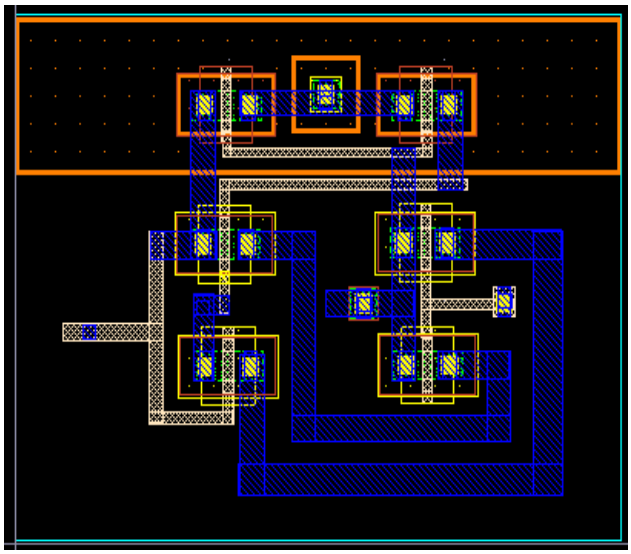


Figure 2: Layout of VCO Ring oscillator

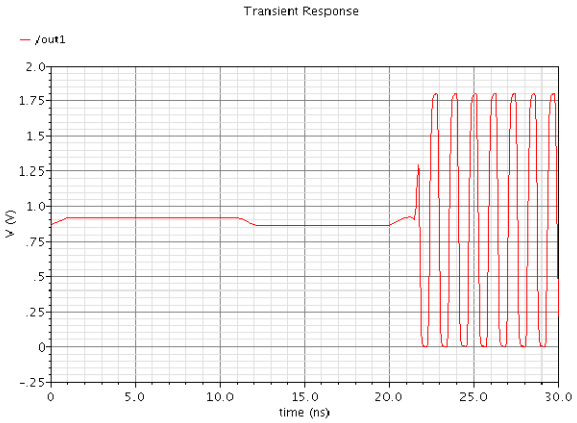


Figure 3: single ended output 1 waveform of VCO

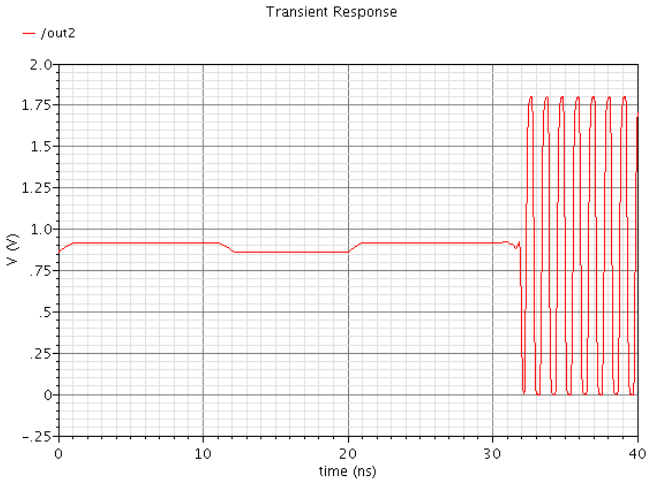


Figure 4: Single Ended Output 2 Waveform Of VCO

$$I_D = \left(\frac{k}{2}\right) * \left(\frac{W}{L}\right) * (V_{GS} - V_{TH})^2 * \left(1 + \lambda_{n,p} V_{DS}\right) (saturation: |V_{DS}| \geq |V_{GS}| - |V_{TH}|) \quad (3)$$

We have following regional relation

$$NMOS \begin{cases} V_{out} > V_{DD} - V_{Tn} : off \\ V_{in} < V_{DD} - V_{Tn} : triode \\ V_{in} \geq V_{DD} - V_{Tn} : saturation \end{cases} \quad (4)$$

$$PMOS \begin{cases} V_{in} < -V_{Tp} : off \\ V_{out} \geq -V_{Tp} : triode \\ V_{out} \leq -V_{Tp} : saturation \end{cases} \quad (5)$$

In above equation = gate to source voltage, = drain to source voltage, = threshold voltage

Frequency of oscillation for N stage Delay VCO is given by following equation as

$$F_{osc} = \frac{1}{NT_d} \quad (6)$$

$$t_d = \frac{1}{2 * N * f_o} \quad (7)$$

Where N is the Number of delay stages and is delay of each stage, Fosc is oscillation frequency.

The figure 3 and figure 4 shows the input–output waveform of source coupled VCO in 45nm technology (Vctrl=0.9V and Vdd=0.7V).

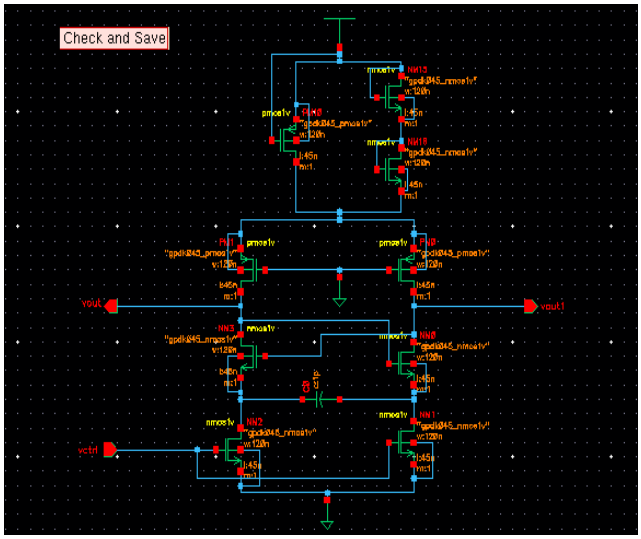


Figure 5: VCO using AVLS technique

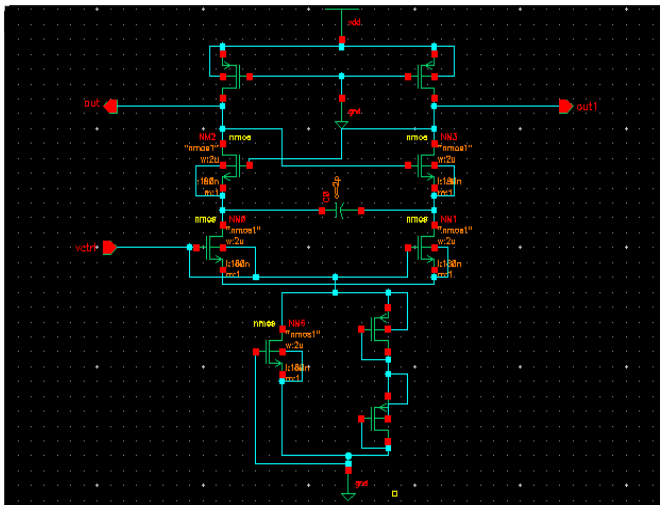


Figure 6: VCO using AVLG technique

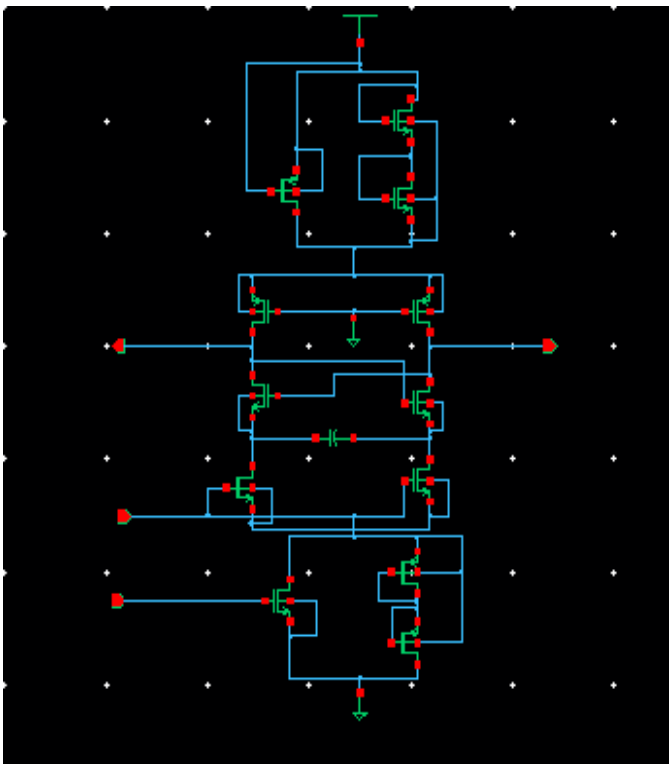


Figure 7: figure of VCO with AVL technique

Table 1: Static power of VCO

Voltage	*Simple VCO*	*AVLS*	*AVLG*	*AVL*
0.7V	2.24µW	3.78pW	1.35pW	1.35fW
0.8V	4.09µW	6.25pW	2.34pW	2.344fw
0.9V	6.47µW	7.76pW	2.98pW	2.98fw
1V	11.43µW	11.48pW	4.81pW	4.81fw

2.2 VCO with Adaptive voltage level technique

An adaptive voltage level control circuit can be used either at the upper end of the cell to reduce supply voltage (AVLS scheme) or at the lower end of the cell to raise the potential of the ground node (AVLG scheme). The impact of these two techniques on leakage currents is described in this section AVLS Technique in Single Stage Source Coupled VCO. To summarize, the AVLS approached, while more successful in reducing the gate leakage current, still leave two gate leakage current components in access transistors unaffected. It also leaves one sub-threshold current component in access transistor unaffected and results in an additional sub-threshold leakage current across the other access transistor [6], [21]-[22].

The figure 5 is show the Voltage control oscillator with Adaptive voltage level source technique with Vdd = 0.7V

2.3 AVLG Technique in Single Stage Source Coupled VCO

AVLG scheme has a better impact on gate leakage current reduction than the AVLS scheme in single stage source coupled VCO[23]-[24]. Fig. 6 shows a schematic of a single-stage source coupled VCO in which AVLG scheme is useful [25]. The switch provides 0 Volt at the ground node during the active mode and a raised ground level (virtual ground) during the inactive mode. This scheme is similar to the diode footed cache design scheme proposed to control gate and sub-threshold leakages in single stage source coupled VCO, in which a diode designed with high Vt MOS transistor was used to raise the ground level of VCO in the inactive mode [26][27]. The figure 7 is show the Voltage control oscillator with Adaptive voltage level ground technique with Vdd = 0.7V

VCO with AVL (AVLS & AVLG) technique
In this technique both AVLS and AVLG techniques are simultaneously applied to the VCO circuit. AVL technique provides better power reduction in comparison to AVLS and AVLG techniques.

3. Simulation Results

The circuit works simulated in cadence for 45nm technology, from the result table. In AVL technique, we are getting effective percentage reduction in parameter (static power, and dynamic power) as compared to SVL technique. The circuit for new design is simulated and analyzed with supply voltage ranges (0.7v to 1v) with Vdd=0.7v.

3.1 Power analysis

The total power dissipation includes dynamic and static components during the active mode of operation.

3.2 Static power dissipation

In the ideal mode, the power dissipation is due to the standby leakage current. Static power dissipation mainly due to sub threshold condition when the transistors are off, Above table 1 is show the parameter of static power on AVL technique in different voltage

3.3 Dynamic power dissipation

Dynamic power dissipation consists of two components. One is the switch power due to charging and discharging of load capacitance. The other short circuit power is due to the nonzero rise and fall time of input waveforms. Dynamic and leakage power of CMOS circuit is given by as tunneling current sub threshold condition when the transistors are off, tunneling current through gate oxide and leakage current through reverse biased diodes.

$$P_{LEAK} = I_{LEAK} V_{dd} \quad (8)$$

$$P_D = \propto f C V_{dd}^2 \quad (9)$$

Where α is the switching activity; f is the operation frequency; C is the load capacitance; Vdd is the supply voltage

Static and dynamic power in AVLG technique = (2.34pw and 0.37nw) at 0.9V (10)
Static and dynamic in AVLS technique= (6.25pw and 1.15nw) at 0.9V (11)
Static and dynamic power dissipation in AVL technique = (3.97fw & 38.02pW (12)

Table 2: Dynamic power of VCO

Voltage	*Simple VCO*	*AVLS*	*AVLG*	*AVL*
0.7V	524.8mW	1.18nW	0.74nW	0.74pW
0.8V	692.8mW	1.15nW	0.378nW	0.378pW
0.9V	699.8mW	1.19nW	0.462nW	0.462pW
1V	700mW	1.433nW	0.522nW	0.522pW

Above table 2 is show the parameter of dynamic power with SVL and AVL technique in different voltage

4. Conclusion

In this paper, present work has been done on single stage voltage controlled oscillator which did not use any spiral inductor. The oscillator was based on creating a (+ve) feedback between the sources of the coupled devices. The simulation results showed that the presented VCO with AVL power reduction technique could achieve low power dissipation, which improves the performance of single stage VCO. In the AVL technique static power in (fW) and dynamic power in (pW) at nominal temperature (27°C). Simulation results provide better result with AVL technique in comparison to other technique. The oscillator can be used for near to the ground voltage, low power applications.

References

[1] Design of low-voltage wide tuning range cmos multipass voltage-controlled ring oscillator by jie ren, dalhousie university halifax, nova scotia march 2011.
[2] L. S. Paula, S. Banpi, E. Fabris, and A. A. Susin, “A wide band CMOS differential voltage-controlled ring oscillators,” International IEEE Northeast Workshop on Circuits and System Design, Jun. 2008,pp. 9-12.2008.
[3] Hormoz Djahanshihi and C. Andre, “Differential CMOS circuit for 622 MHz-933MHzCDR application” ,IEEE J.solid –state circuits, june 2000.
[4] O.-C. CHEN, R. SHEEN, A Power-Efficient Wide-Range Phase-Locked Loop, IEEE Journal of Solid State Circuits, vol.37, 1, (2002), 51-,.
[5] Behzad Razavi, “design of analog CMOS integrated circuits”. Book by Tata MC Graw –Hill Edition, 2000.
[6] Y.-H. Chuang, S.-H. Lee, S.-L. Jang, Senior Member, IEEE, J.-J. Chao, and M.-H. Juang, Senior Member, IEEE “A Ring-Oscillator-Based Wide Locking Range Frequency Divider” IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 16, NO. 8, AUGUST 2006.
[7] Seema Butala Anand and Behzad Razavi, “ACMOS clock recovery circuit for 2.5Gb/s”. NRZ data, IEEE J.solid state circuits mar, 2001.
[8] William Shing Tak Yan, “A900MHz CMOS Low phase Noise voltage controlled ring oscillator”. IEEE transaction on circuits and system, Feb, 2001.
[9] Xiang Yi, Graduate Student Member, IEEE, Chirn Chye Boon, Senior Member, IEEE, Manh Anh Do, Senior Member, IEEE, Kiat Seng Yeo, Senior Member, IEEE, and Wei Meng Lim, “Design of Ring-Oscillator-Based Injection-Locked Frequency Dividers With Single Phase Inputs” IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 21, NO. 10, OCTOBER 2011.
[10] Rui Tao, Manfred Berroth, “5 GHz voltage controlled ring oscillator using source capacitively coupled current amplifier”. IEEE 2003.
[11] J.M.Rabaey, A.Chandrakasan, and B.Nikolic, “Digital Integrated circuits, upper saddle River”. N:pearson /prentice Hall, 2003.
[12] Neric Fong, et.al. “A low- voltage 40GHz complementary vco with 15% frequency tuning Range in SOI CMOS Technology”. IEEE journal of solid state circuits, vol.39, no.5, may 2004.
[13] D.Levacq,et.al, “potential af SOI intrinsic MOSFETs for ring VCO design”. SOI con. 2003, pp.17-18.
[14] Wei-HsuanTu, Jyh-Yjhyeh, Hung-Chieh Tsai and Chrng-Kuang Wang, “A1.8v 2.5-5.2GHz CMOS Dual –input two stage Ring VCO”. Asia-pacificconfrence an advanced system IC, IEEE Aug, 2004.
[15] B.Leung, “A novel model on phase noise of ring oscillator based on last passage time”. IEEE Trans. Circuits System International ,Fundamental Theory application , vol.51, No.3, pp.471-482, Mar .2004.
[16] L. S. Paula, S. Banpi, E. Fabris, and A. A. Susin, “A wide band CMOS differential voltage-controlled ring

oscillators," International IEEE Northeast Workshop on Circuits and System Design, Jun. 2008, pp. 9-12.2008.

[17] Rashmi K Patil, Vrushali G Nasre, "A Performance Comparison of current starved VCO and source coupled VCO for PLL in 0.18μm CMOS process". IJEIT, vol1,Issue2, feb 2012.

[18] M K Mandal, B C Sarkar," Ring oscillators: Characteristics and applications" Indian Journal of Pure & Applied Physics Vol. 48, February 2010, pp. 136-145 .

[19] Shyam Akashe, Sushil Bhushan, and Sanjay Sharma, "Implementation of Technology Scaling on Leakage Reduction Techniques Using Cadence Tools", J. Comput. Theor. Nanosci, 9, 2155-2159, 2012

[20] Rashmi K Patil, Vrushali G Nasre, "A Performance Comparison of current starved VCO and source coupled VCO for PLL in 0.18μm CMOS process". IJEIT, vol1,Issue2, feb 2012.

[21] M. Janaki Rani ,S. Malarkann" LEAKAGE POWER REDUCTION AND ANALYSIS OF CMOS SEQUENTIAL CIRCUITS" International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012.

[22] Manoj Kumar, Sandeep K. Arya, and Sujata Pandey," Low Power Voltage Controlled Ring Oscillator Design with Substrate Biasing", International Journal of Information and Electronics Engineering, Vol. 2, No. 2, March 2012.

[23] L. S. Yeop, S. Amakawa, N. Ishihara, and K. Masu, "Low-phasenoise wide-frequency-range ring-VCO-based scalable PLL with sub harmonic injection locking in 0.18 μm CMOS," IEEE International Microwave Symposium Digest, May 2010, pp. 1178-1181.

[24] Anurag-Bhargav, Shyam Akashe, and Sanjay Sharma, "A Low Power Static Random Access Memory Cell with High Read Stabilit", J. Comput. Theor. Nanosci., 9, 1049-1054, 2012.

[25] Asad A., Abidi, Fellow, IEEE, "phase noise and jitter in CMOS Ring Oscillator". IEEE journal of Solid –State Circuits, vol.41, No.8, Aug. 2006.

[26] S. Y. Lee and J. Y. Hsieh, "Analysis and implementation of a 0.9V voltage-controlled oscillator with low phase noise and low power dissipation," IEEE Transaction on Circuits and Systems II, vol. 55, no.7, pp. 624-627, Jul. 2008.

Author Profile



Neeta Yadav received a Bachelor in Engineering from YMCA Institute of Science and Technology, Faridabad in 2010 and carrying her Masters degree in Lingayas University, Faridabad. She is System Engineer in Tata Consultancy Services, Gurgaon. Her main research interest is VLSI



Nitin Saluja received a Masters in Engineering from the Thapar University in 2010 and carrying his Ph.D. degree. He is Assistant Professor at Lingaya's University, Faridabad. His main research interests are design and optimization of Microstrip antenna design, Microwave Design, Fractal Antennas, Multiband and wideband antenna and Wireless networks. He has published many papers in referred journals and conferences on Microstrip antenna and wireless networks. He is editor, reviewer and convener of conferences and reviewer of journals.