# Different Packaging Style Of Chips In Electronic System

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**Abstract:** ***This paper the state-of-the-art in packaging technology. A number of bar dice and multi chip module (MCM) stacking technologies are emerging to meet the ever increasing demands for low power consumption, low weight and compact portable systems. Technical issues such as silicon efficiency, complexity, thermal management, interconnection density, speed, power etc[1]. Prevailing conventional wisdom in today's chip packaging world presumes that only the chip design team is qualified to define IC package. That argument is compelling, since the chip design team is most familiar with the silicon chip, and therefore most qualified to determine the packaging. For purpose of this paper, an "optimized" or "optimal" board shall be defined as being the smallest in size, with shortest copper routing, fewest inner-layers operating at the highest performance, and potentially having the quickest development time to market[2].***

**Keywords:** MCM, IC package

## 1. Introduction

.In electronics manufacturing, integrated circuit packaging is the final stage of semiconductor device fabrication, in which the tiny block of semiconducting material is encased in a supporting case that prevents physical damage and corrosion. The case, known as a "package", supports the electrical contacts which connect the device to a circuit board.In the integrated circuit industry it is called simply packaging and sometimes semiconductor device assembly, or simply assembly. Sometimes it is called encapsulation or seal. The packaging stage is followed by testing of the integrated circuit.The term is sometimes confused with electronic packaging, which is the mounting and interconnecting of integrated circuits (and other components) onto printed-circuit boards.The earliest integrated circuits were packaged in ceramic flat packs, which the military used for many years for their reliability and small size. Commercial circuit packaging quickly moved to the dual in-line package (DIP), first in ceramic and later in plastic. Inthe1980s VLSIpin counts exceeded the practical limit for DIP packaging, leading to pin grid array (PGA) and leadless chip carrier (LCC) packages.Surface mount packaging appeared in the early 1980s and became popular in the late 1980s, using finer lead pitch with leads formed as either gull-wing or J-lead, as exemplified by small-outline integrated circuit — a carrier which occupies an area about 30 – 50% less than an equivalent DIP, with a typical thickness that is 70% less. This package has "gull wing" leads protruding from the two long sides and a lead spacing of 0.050 inches.

## 2. Methodology

### 2.1. TYPES OF CHIP PACKAGING

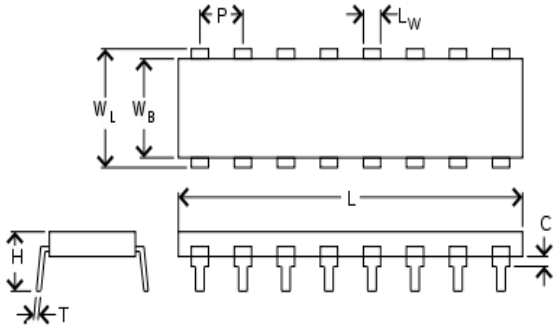
- **Through-hole package:**

Through hole technology uses holes drilled through the PCB for mounting the components. The component has leads that are soldered to pads on the PCB to electrically and mechanically connect them to the PCB.

1. Single in-line package (DIP)
2. Dual in-line package (DIP)
3. Ceramic Dual in-line package (CDIP)
4. Glass sealed ceramic (CERDIP)
5. Quadruple in-line package (QIP)
6. Zig-zag in-line package (ZIP)
7. Molded Dual in-line package (MDIP)

8. Plastic Dual in-line package(PDIP) Through hole.

**2.1.1. Through hole:**




C - Clearance between IC body and board
H Total Height
T - Lead Thickness
L - Total Carrier Length
$L_W$ - Lead Width
$L_L$ - Lead Length
P - Pitch
$W_B$ - IC Body Width
$W_L$ - Lead-to-Lead Width-

It has been suggested that portions of Surface-mount technology#Packages be split from it and merged into this article. (Discuss)

1.Ceramic Column Grid Array(CCGA)

3 2.Column Grid Array(CGA)

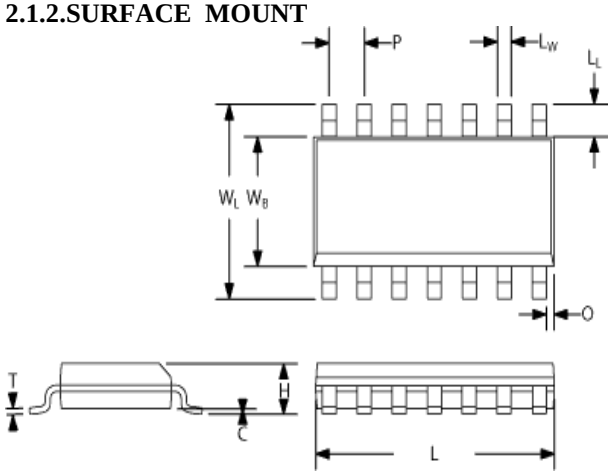
4 3.Lead-Less lead-Frame Package(LLP)

5 4.Land Grid Array(LGA)

6 5.Low Temperature Co-fired Ceramic(LTCC)

7 6.Multi-chip Module(MCM)

**8 2.1.2.SURFACE MOUNT**

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10 C- Clearance between IC body and PCB
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L- Total Carrier Length
$L_W$- Lead Width
$L_L$- Lead Length
P – Pitch

**11 CHIP PACKAGING USAGE COST**

12 To simplify the discussion of this paper, the based

13 assumption made is the cost of combine package solution

14 will be lower than individual package of each chip. The

15 gross die count per wafer(GDPW)[1] extraction for this paper is done based on 300mm diameter wafer. The analysis for multi chip packaging usage cost will be divide into 4 main category which differentiate by process as well as die size.

(1)

## 3. Packaging Evolution

**3.1.Single-chip Packaging:**

The overall packaging has evolved with dual-inline packages(DIPs) and wire bond in the 1970s, and ball-grid arrays in the 1990s.All this technologies, however, provide a silicon packaging efficiency of only about 10%.The use of chip-scale packaging (CSP), with packaging no bigger than an IC itself, as well as the use of bare-chip multichip module (MCP) packaging, will raise this efficiency to about 40%, still far from the goal of 100% efficiency.

**3.2.Multichip packaging:**

Multichip technologies are generally divided into three group based on ceramic, thin film, and printed wiring board (PWD) technologies. The wiring density per layer or iput/output connection density is highest for thin film technologies, followed by ceramic, and least for PWB technology.

## 4.Chip Packaging Issues

There are numerous issues yet to be solved before Chip Packaging can be adopted as a standard industry practice. Firstly, EDA chip pinout optimization software must be reliable and economically available for mainstream board designers to use. Sigrity demonstrated a version of such EDA chip optimization software during the June 2007 Design Automation Conference (DAC) in San Diego [5]. Another company, CAD Design Software demonstrated a version EDA chip optimization software during the July 2007 Semicon West show in San Francisco [6]. Other companies are working on creating versions of EDA chip optimization software. Assuming that the foregoing issue with EDA software is resolved, the next challenge of Chip Packaging 2.0 is how to assemble die with crossing "bird's nest" wire bonding that go across the die in every direction. A hallmark of Chip Packaging 1.0 is the neat and orderly wire bonding. However, in the Chip Packaging 2.0 environment, "neat and orderly" is replaced with apparently disorderly wires that cross over one other as.

## 5.Limitations:

**5.1.Thermal Management**

**As** the demand increases to build high performance systems, trends in electronics packaging design have moved toward larger chips, higher number ofI/O ports, increased circuit density, and improved reliability

**5.2.Design Comlexity**

Advances in interconnection technology have played a key role in allowing continued improvement in integrated circuit, performance, and cost. Over the last 20 years, circuit density has increased by a factor of approximately 10^4. According to Gorden Moore, CEO**5.3.COST**With the emergence of any new technology, there is an expected high cost involved in using it.As it is case with technology, the cost involved at present is high, due to the lack of infrastructure and the reluctance of manufactures to change to new technologies for reasons associated with risk factors.

## 6.Conclusion:

A technical vision for next – generation electronic packaging that reaches beyond MCM, flip – chip, and chip-scale packaging is proposed .. This vision is based on highly integrated single-level packaging that offers 10-fold improvement in the cost, size, performance, and reliability of electronics product. A similar vision for educating student as globally competitive engineers is proposed, with strong fundamental science and cross disciplinary engineering knowledge as well as system level training in manufacturing, business economics, and foreign language and culture.

Significant savings in power consumption, weight and physical volume can be achieve by adopting the packaging approach. A number of emergent bare dice and MCM stacking approaches have beereviewed

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