Role Of System On Chip(Soc) In Modern Electronics

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Abstract: ***An embedded processor system having a single-chip embedded microprocessor, with analog and digital electrical interfaces to external systems, that is suitable for implementation in various integrated circuit technology formats. A processor core uses pipelined execution of multiple independent or dependent concurrent threads, together with supervisory control for monitoring and controlling the processor thread state and access to other components. The pipeline enables simultaneous execution of multiple threads by selectively avoiding memory or peripheral access conflicts through the types of pipeline stages chosen and the use of dual and tri-port memory techniques. The single processor core executes one or multiple instruction streams on multiple data streams in various combinations under the control of single or multiple threads. The invention can also support a programmable clock mechanism, thread-level monitoring capability, and power management capability***

Keywords: Pipeline,Processor,Instruction

1. Introduction

SOC is a system on VLSI chip that has all needed analog as well as digitalcircuits,processor&software,for example: single chip mobile. SOC is not only chip but more on "system". SOC=chip + software + integration. The SOC chip includes: embedded processor, ASIC logics & analog circuitry embedded memory.
The SOC software includes: OS, compiler, simulator,firmware,driver,protocol,stackintegrated development environment, application interface(C/C++, assembly).
The SOC integration includes: the whole system solution, manufacture consult, technical supporting.
In the past, field programmable gate arrays (FPGAs) have been used to absorb glue logic, perform signal processing, and even to prototype system-on-chip (SoC) ASICs. Now with the advent of large, fast, cheap FPGAs, such as Xilinx Spartan-II (100,000 1 ns "gates" for $15, quantity one), it is practical and cost-effective to skip the ASIC and ship volume ROM -- the FPGA implements all of the system logic including a processor core. An FPGA SOC platform offers many potential advantages, including high integration, short time to market, low NRE costs, and easy field upgrades of entire systems, even over the Internet. A soft CPU core enables custom instructions and function units, and can be reconfigured to enhance SoC development, debugging, testing, and tuning. And if you control your own "cores" intellectual property (IP), you will be less at the mercy of the production and end-of-life decisions of chip vendors, and can ride programmable logic price and size improvement curves.
The design of a modern System-on-Chip (SoC) is a complex task involving a range of skills and a deep understanding of a hierarchy of perspectives on design, from processor architecture down to signal integrity.At a time when many organizations are walking away from (SoC) module which incorporates significant practical work on the system level design required to implement SoC, a course in this area is set to be given to third-year Computer Science, Computer Engineering and Computer Systems Engineering students at The University of Manchester in the UK. These students will have undertaken digital design in their first year and an introductory course in VLSI Design in their second year.
The module aims to show how correctly-working chips can be obtained by presenting and demonstrating the techniques and stages used in the design andimplementation of chips. Since leading-edge industry standard software tools and languages are taught and practiced, the skills gained with this course are directly transferable into companies and post-graduate research in this area.

2. Methodology

2.1.System-On-Chip Design Hierarchy

Both the lectures and the practical work follow thedesign methodology for top-down SOC design .This methodology partitions the design into a number ofstages where one level is designed, tested and modifieduntil correct. The process then repeats at the next leveldown, beginning with the translation of the design fromthe upper to the lower level; unfortunately, this translationis not always a direct translation. The generic designhierarchy used is summarized in Fig. 1.

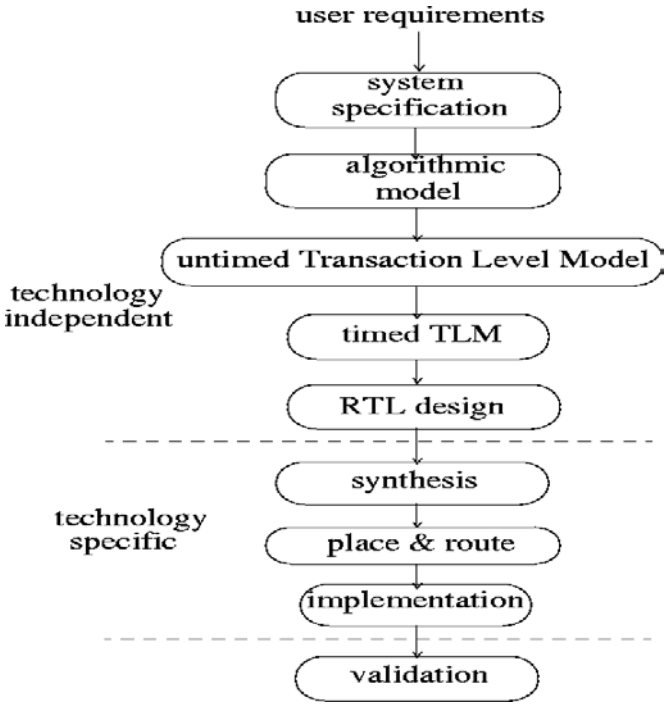
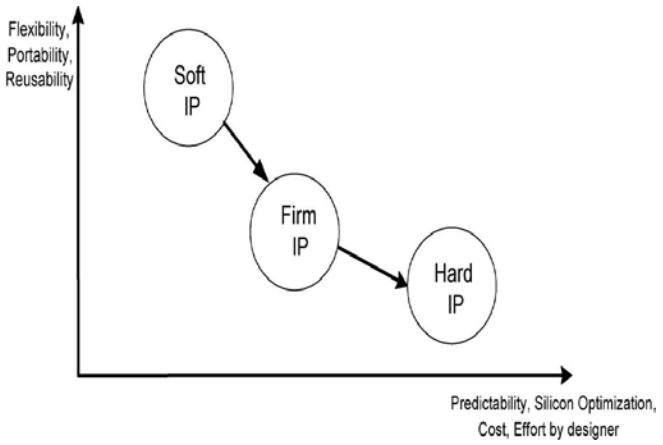


Figure1 Generic Design Hierarchy



These reusable IP cores may include embedded processors, memory blocks, interface blocks, analog blocks, that handle application specific processingfunctions. Corresponding software components are also provided in a reusable form and may include real-timeoperating systems and kernels, library functions, and devicedriversB. Analog/Mixed-Signal Design for Reuse-While design productivity can be improved significantlywith the use of digital IP blocks, another bottleneck exists if the designs include analog and mixed-signal components.Digital design has a well-defined, top-down design methodologybut analog/mixed-signal (AMS) design has traditionallybeen an ad hoc custom design process.One of the main advantages of the use ofAMS IP in SoCs is the potential reduction in power, whichis especially important in battery-operated applicationssuch as personal digital assistants (PDAs), wireless localarea networks (LANs), etc. An often-viewed competitor to SoC is the notion ofsystem-in-package (SiP) whereby separate chips arepackaged together into a system with a very small formfactor using a common two-dimensional (2-D) or threedimensional(3-D) substrate. It is most suitable for theintegration of heterogeneous technologies where singlechipintegration is difficult or too expeThe key issue is to decide which option provides the best solution for a given product. Moreover, an SoC can be part of an SiP or SoB solution if appropriate from cost, system performance, and time-tomarket perspectives. Fig. 2 illustrates first-order tradeoffs of the three options in terms of turnaround time, form factor, and power. The rest of this paper is organized as follows.

The RTL descriptions usually are configurable in that certain parameters are user-definable to tailor the block to the needs of the customer. This allows selective inclusion or exclusion of distinguishing features which can impact the final implementation's performance, cost, and power. In the case of a processor core, parameters such as the bus width, number of registers, cache sizes, and instruction set may vary from customer to customer, so the flexibility of soft IP allows for their modification before synthesis. Commercial tools exist for this purpose in whicha configurable processor with specific attributes can beautomatically generated [15]. Such flexibility provides
lower area, power, and improved performance, since the IPblock can be tuned for each application. In addition, somefeatures in a given IP block that are not needed by allcustomers can be removed. With some effort, the finaldesign generated from a soft IP block can be within 20%–30% of the power and timing of a hard IP implementation.
System-on-chip has been a nebulous term, that mystically holds out a lot of excitement, and hasbeen gaining momentum in the electronics industry. While the potential is huge, the complexitiesare several, and countering these to offer successful designs is a true engineering challenge.Witness these market trends:

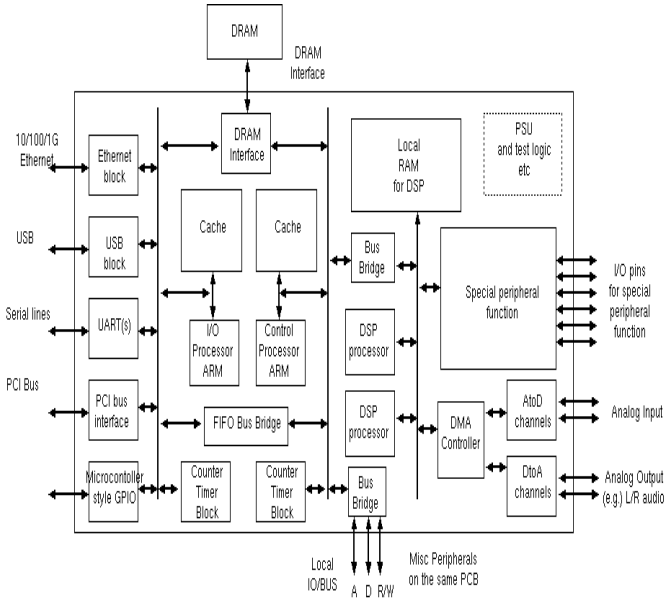
- Research agency In-Stat predicts robust market growth for System-on-Chips (SoCs), estimating that volumes will increase an average of 31% a year, reaching 1.3 billion units in 2004.
- SoCs make up 20% of chip market today, this will be 40% in 2004.

Semiconductor Companies are investing two-thirds of their R&D resources in theSystem-on-Chip arena

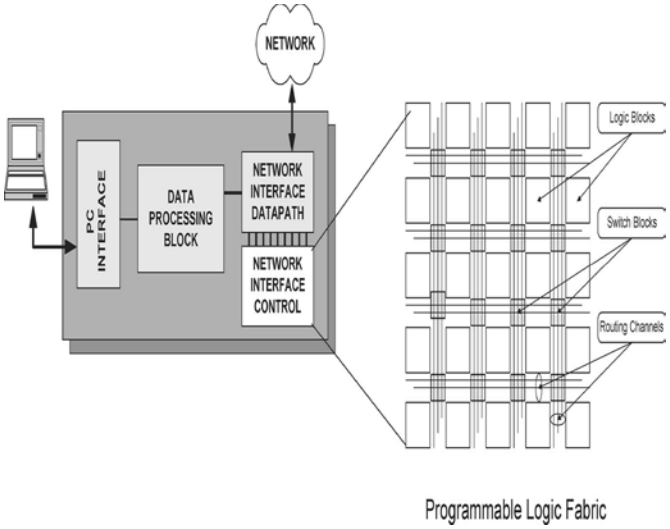
2.2.Soc Design-

A current-day system on a chip (SoC) consists of several different microprocessor subsystems together with Memories and I/O interfaces. This course covers SoC design and modeling techniques with emphasis on Architectural exploration, assertion-driven design and the concurrent development of hardware and embedded software. This is the \front end" of the design automation tool chain. (Back end material, such as design of individual gates, layout, routing and fabrication of silicon chips is not covered.)A percentage of each lecture is used to develop a running example. Over the course of the lectures, the exampleevolves into a System On Chip demonstrator with CPU and bus models, device

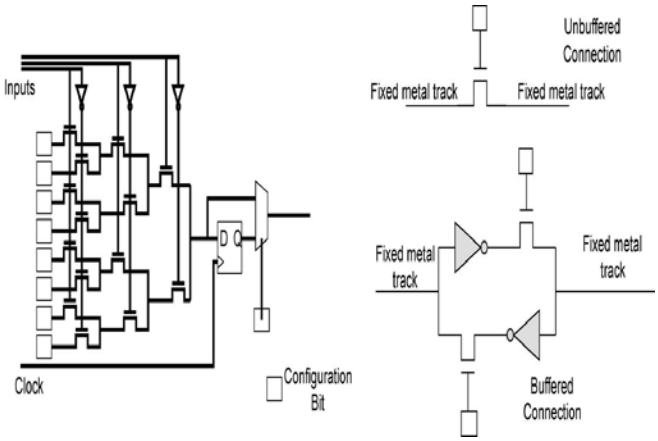
models and device drivers. AllCode and tools are available online so the examples can be reproduced and exercises undertaken. The mainlanguages used are Verilog and C++ using the SystemC library.Lecture Groups and Syllabus:Verilog RTL design with examples. Event-driven simulation with and without delta cycles, basics of synthesis to gates algorithm and design examples.Structural hazards, pipelining, memories andmultipliers.Systems overview. The major components of the SystemC, C++ class library for hardware modelingare covered with code fragments and demonstrations.Basic SoC Components and Bus Structures. CPU, RAM, Timers, DMA, GPIO, Network, Busstructure. Interrupts, DMA and device drivers.Examples Basic bus bridging,ESL + Transactional Modeling, Electronic systems level (ESL) design Architectural exploration,Firmware modelling methods. Blocking and non-blocking transaction styles. Approximate and loose timing stylesQueue and contention modelling.Examples-ABD: Assertions and Monitors. Types of assertion (imperative, safety, liveness, data conservation).Assertion-based design (ABD).PSL/SVA assertions.Temporal logic compilation of fragments to monitoring FSM. Further Bus Structures. Busses used in today's SoCs (OPB/BVCI, AHB and AXI). Glue logic synthesis. Transactor synthesis.Pipeline Tolerance.Network on chip. Easter Term 2011 1 System-On-Chip D/M.



Hardware Programmability: Hardware programmability is enabled by the incorporation of one or more programmable logic cores into an SOC . The programmable logic core is a flexible logic fabric that can be customized to implement any digital circuit after fabrication. Such an embedded core may look very much like theprogrammable fabric in a stand-alone field-programmable gate array (FPGA). Before fabrication, the designer embeds the fabric (consisting of many uncommitted gates and programmable interconnects between the gates) onto the chip. After the fabrication, the designer can then program these gates and the connections between them.



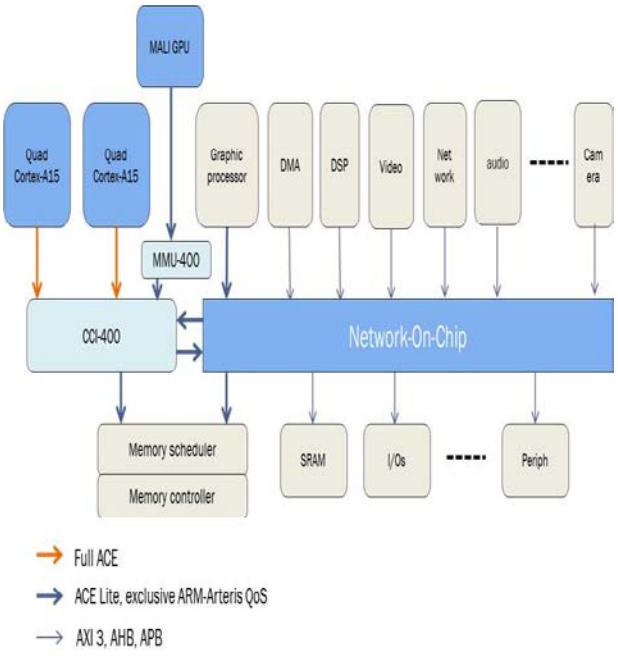
Programmable Logic Fabric



Software Programmability: Software is the most natural form of programmability for an SoC. Embedded software allows a single SoC to have different Personalities[and serve different customers or market segments. From a design perspective, as much of the solution should be implemented in software as possible tomaximize the flexibility of the design. Complex control functions are better suited to software implementationswhereas data operations are better implemented in hardware. If performance is an issue, then hardwaremust be used for the implementation which can take the form of a programmable logic fabric, which is roughly five times faster than software, or an ASIC implementation, which is typically 50 times faster than software.

2.3.Architecture Strategy

A key dependency that actually defines an SOC architecture is the kind of processor that one uses as the central processing element. At Wipro, significant focus has been on the ARM processor technology, since we believe that will drive the evolving market for embedded applications, mobile devices and next generation information appliances. Our expertise with ARM cores and technology is also a derivative of our long standing association with ARM, and our status as an approved ARM Design Center.



2.4.Network On Chip-

A more structured interconnect fabric is being pursued in the research community for commercial designs that must integrate a large number (10–100) of IP blocks in a single SoC. Today, there exist many SoC designs that contain a number of processors in applications such as set-top boxes, wireless base stations, HDTV, mobile handsets, and image processing. Such systems behave as multiprocessors, and require a corresponding design methodology for both their hardware and software implementations. Power budgets and cross-chip signaling constraints are forcing the development of new design methodologies to incorporate explicit pipelining and provide a more structured communication fabric. Many researchers have suggested that future designs will be dominated by arrays of processors that form the basis of new multiprocessor SoC platforms (the so-called MP-SoCplatforms.
The Benefits • There are several benefits in integrating a large digital system into a single integrated circuit . • These include – Lower cost per gate . – Lower power consumption . – Faster circuit operation . – More reliable implementation . – Smaller physical size . – Greater design security .

3.Advantages-

- Partitioner entirely on chip
- Transparent process
  -no extra designer effort
  -no disruption to standard tool flows
- Can use existing compilers while partitioning
- Can tune system to actual usage and data values
- Can adapt to new usage over time
- Supports legacy programs

3. Conclusion

SoC is a highly challenging topic for including in a degree course. It includes many difficult concepts and hardware languages which are unfamiliar to students and thus represents a large, steep learning curve. Nevertheless,the course described does illustrate that given a strictly bounded design, the major problems in SoC design can be demonstrated, with students gaining the techniques necessary to solve these. These design skills together with a practical knowledge of industry-standard tools are directly transferable to firms working in this area

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