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A Brief Overview of Different LDPC Code

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Abstract: ***This paper corresponds to a brief survey of LDPC codes. Many error detection and correction codes have been studied. There are vast classes of such codes; some of them are hamming codes, turbo codes, BCH codes and LDPC codes. But among these codes LDPC codes achieve better performance and lower decoding complexity. LDPC codes were originally discovered by Robert G. Gallager. But after the rediscovery of LDPC codes by Mackay and Neal in 1995 interest on LDPC codes increases because of its bit error performance approaches asymptotically the Shannon limit. An LDPC code is a special class of linear block codes whose parity-check matrix H has low density of ones i.e. sparse. Due to this sparsity in LDPC codes there is low complexity decoding and its implementation is also simple. Also LDPC codes provides large degree of parallelism that can be exploited in the decoder and in LDPC codes information block length are long enough. In addition LDPC codes provides wide range of trade-offs between performance and complexity. A major drawback of LDPC codes is their high encoding complexity.LDPC codes find its application in many areas such as satellite transmission of digital television. LDPC codes also used for 10 GBase-T Ethernet which sends data at 10 gigabits per second over twisted pair cable.***

Keywords:*LDPC, Gbase-T, MIMO.*

1. Introduction

In information theory, a low density parity-check (LDPC) codes is a linear error correcting code, a technique of transmitting a message over a noisy transmission channel. LDPC codes were invented by Robert Gallager in his PHD thesis. LDPC ode is linear error correcting code i.e. a method of transmitting a message over a noisy channel. An LDPC code is constructed using a sparse bipartite graph. LDPC codes are capacity approaching codes, which means that practical construction exist that allow the noise threshold to be set very close to theoretical maximum for symmetric memoryless channel [4]. The noise threshold defines an upper bound for channel noise up to which the probability of lost information can be made as small as desired. By using iterative belief propagation techniques, LDPC codes can be decoded in time linear to their block length [7]

The two most important advantages of LDPC codes are absence of low-weight code words and iterative decoding of lower complexity. With regards to the issue of low-weight code word, we usually find that a small number of code words are undesirably close to the given code word. Due to this closeness in weights channel noise causes the transmitted code word to be mistaken for a nearby code word which is responsible for the error floor. LDPC codes can be easily constructed so that they do not have such low-weight code words, and they can therefore achieve vanishingly small bit error rates. Also LDPC codes use a simple parity -check trellis that has just two states. Consequently, the decoders for LDPC codes are significantly simpler. Moreover, being parallelizable, LDPC decoding may be performed at greater speeds [3]. In LDPC codes larger girth improves the computational and bit error rate (BER) performance [4]. However, a practical objection to the use of LDPC codes is that for large block lengths, their encoding complexity is high [3].

2. Literature Review

In a paper presented **by Hisashi Futaki and Tomoaki Ohtsuki in 2003** transmit diversity schemes have been studied for high spectral-efficiency and high bit-rate transmission, such as multi-input multi-output (MIMO) systems. In the MIMO systems, forward error correction coding is essential for high quality communications. Recently, low-density parity-check (LDPC) codes have attracted much attention as good error correcting codes like turbo codes. LDPC codes have been applied to the MIMO systems, where they refer to the system as the MIMO-LDPC. In this paper, they propose a new MIMO-LDPC system with iterative turbo decoding (MIMO-LDPC-TD) using two LDPC encoders and two LDPC decoders to improve the performance of the MIMO-LDPC. Since each decoder in the MIMO-LDPC-TD is smaller than that in the MIMO-LDPC, the decoding complexity at each decoder in the MIMO-LDPCTD is less than that in the MIMO-LDPC. They also compare the performance of the MIMO-LDPC with that of the turbo coded MIMO systems (MIMO-turbo) on flat Rayleigh fading channels. They show that the MIMO-LDPC-TD can achieve the good error rate performance with reduced decoding complexity at each decoder on a flat Rayleigh fading channel, particularly on a slow fading channel. They also show that the MIMO-LDPC can achieve the better error rate performance than the MIMO-turbo on a fast Rayleigh fading channel **[1].**

A paper by **Gabofetswe Malema, Michael Liebelt** presents a programmable semi-parallel architecture for Low-Density Parity-check{LDPC) codes. Communication conflicts are avoided by edge-coloring the code graph and grouping of edges/physical connections by color. The architecture model is easily scalable and programmable for larger block sizes. Though the communication hardware cost is high, the model can be easily reconfigured to reduce hardware cost at the

expense of flexibility in code design and decoding performance. The hardware cost, latency, code flexibility and code performance tradeoffs can be varied over a wide range to suit a wide range of applications. Simple execution control and mapping are other advantages of this model **[2].**

Dong-U Lee and Wayne Luk etc describe a flexible hardware encoder for regular and irregular low-density parity-check (LDPC) codes in their paper. Although LDPC codes achieve better performance and lower decoding complexity than Turbo codes, a major drawback of LDPC codes is their apparently high encoding complexity. Using an efficient encoding method proposed by Richardson and Urbanke, they present a hardware LDPC encoder with linear encoding complexity. The encoder is flexible, supporting arbitrary H matrices, rates and block lengths. An implementation for a rate 1/2 irregular length 2000 LDPC code encoder on a Xilinx Virtex-II XC2V4000-6 FPGA takes up 4% of the device. It runs at 143MHz and has a throughput of 45 million codeword bits per second (or 22 million information bits per second) with a latency of 0.18ms. The performance can be improved by exploiting parallelism: several instances of the encoder can be mapped onto the same chip to encode multiple message blocks concurrently. An implementation of 16 instances of the encoder on the same device at 82MHz is capable of 410 million codeword bits per second, 80 times faster than an Intel Pentium-IV 2.4GHz PC **[3].**

José M.F. Moura, Jin Lu, and Haotian Zhang considers the problem of designing un-oriented bipartite graphs with large girth. These graphs are the Tanner graphs associated with the parity-check matrix H of low density parity-check (LDPC) codes or Gallager codes. Larger girth improves the computational and bit error rate (BER) performance of these codes. The article overviews several existing methods in the literature and then describes two new constructions for LDPC codes with large girth—geometry based and turbo structured LDPC codes **[4].**

Heng Tang, Jun Xu presents three algebraic methods for constructing low-density parity-check (LDPC) codes. These methods are based on the structural properties of finite geometries. The first method gives a class of Gallager codes and a class of complementary Gallager codes. The second method results in two classes of circulant-LDPC codes, one in cyclic form and the other in quasi-cyclic form. The third method is a two-step hybrid method. Codes in these classes have a wide range of rates and minimum distances, and they perform well with iterative decoding **[5].**

Mong-Kai Ku, Huan-Sheng Li presented a genetic algorithm (GA) based LDPC code search algorithm with hardware considerations. Regular quasi-cyclic LDPC codes are used due to its friendliness to hardware implementation. Their hardware architecture design schedules pipeline LDPC decoding operation to boost the hardware utilization efficiency (HUE) of LDPC decoder **[6].**

New algebraic methods for constructing codes based on hyperplanes of two different dimensions in finite geometries are presented by **Heng Tang,Jun Xu,** . The new construction methods result in a class of multistep majority-logic decodable codes and three classes of low-density parity-check (LDPC) codes. Decoding methods for the class of majority-logic decodable codes, and a class of codes that perform well with iterative decoding in spite of having many cycles of length 4 in their Tanner graphs, are presented. Most of the codes constructed can be either put in cyclic or quasi-cyclic form and hence their encoding can be implemented with linear shift registers **[7].**

Mohamed Adnan Landolsi presented a comparative performance and complexity study between low-density parity check (LDPC) codes and turbo product codes (TPC) of short block length (within 2048 bits) on his paper . The LDPC codes are of the semi-random (SR) type, characterized by low encoder complexity, and are further optimized by eliminating short cycles of length 4 (minimum girth 6). The TPC codes are obtained from 2D and 3D constructions chosen to match the LDPC codes' parameters. The numerical results show that the SR-LDPC codes have slightly better error performance (to within 0.5dB, at a BER of 10-5) while demonstrating lower computational complexity per decoder iteration, but the required number of decoding iterations is larger. However, this disadvantage is significantly reduced for moderately high signal-to-noise ratios (starting from 2.5dB). It is therefore concluded that SR-LDPC codes have a more competitive performance complexity over all **[8].**

In the paper presented by **Lei Yang, Hui Liu, and C.-J. Richard Shi**, a 9-k code length multi-rate LDPC decoder architecture is presented and implemented on a Xilinx field-programmable gate array device. Using pin selection, three operating modes, namely, the irregular 1/2 code mode, the regular 5/8 code mode, and the regular 7/8 code mode, are supported. Furthermore, to suppress the error floor level, a characterization on the conditions for short cycles in a LDPC code matrix expanded from a small base matrix is presented, and a cycle elimination algorithm is developed to detect and break such short cycles. The effectiveness of the cycle elimination algorithm has been verified by both simulation and hardware measurements, which show that the error floor is suppressed to a much lower level without incurring any performance penalty. The implemented decoder is tested in an experimental LDPC orthogonal frequency division multiplexing system and achieves the superior measured performance of block error rate below 10 7 at signal-to-noise ratio of 1.8 dB **[9].**

3. Survey of LDPC Code in Tabular form

Table 3: Survey of LDPC Code

S. No.	Paper Title	Publication	Author Name	Advantages	Disadvantages
1	Structured Low-Density Parity-Check Codes, Methods to design regular LDPC codes with large girth	IEEE SIGNAL PROCESSING MAGAZINE, 2004	José M.F. Moura, Jin Lu, and Haotian Zhang	1. LDPC codes are good because in these bit error rate performance approaches asymptotically the Shannon limit. 2. An LDPC code is a special class of linear block codes whose parity-check matrix has a low density of ones, i.e., is sparse. 3. The regularity and structure of LDPC codes utilize memory more efficiently and simplifies the implementation o LDPC decoder. 4. Larger girth improves the computational and bit error rate (BER) performance of LDPC codes. 5. Large girth speeds the convergence of iterative decoding and improves the performance at least in the high SNR range, by slowing down the onsetting of the error floor.	1. Geometry based designs of LDPC codes (GB-LDPC) have low SNR than turbo-structured LDPC codes (TS-LDPC).
2	Low-Density Parity-Check (LDPC) Coded MIMO Systems with Iterative Turbo Decoding	IEEE,2003	Hisashi Futaki, Tomoaki Ohtsuki	1. Low Density Parity Codes are good error correcting codes. 2. LDPC codes can achieve the near Shannon limit performance with the practical decoding complexity like turbo codes on an additive white Gaussian noise (AWGN) channel. 3. The MIMO-LDPC-TD can achieve the good error rate performance with reduced decoding complexity at each decoder on a flat Rayleigh fading channel, particularly on a slow fading channel.	1. BER of the MIMO-LDPC is worse than that of the MIMO turbo on a slow fading channel, while the MIMO-LDPC can achieve the better BER than the MIMO-turbo on a fast fading channel. 2. Decoder in the MIMO-LDPC-TD is smaller than that in the MIMO-LDPC; the decoding complexity at each decoder in the MIMO-LDPCTD is less than that in the MIMO-LDPC.
3	On Algebraic Construction of Gallager and Circulant Low-Density Parity-Check Codes	IEEE TRANSACTIONS ON INFORMATION THEORY, VOL. 50, NO. 6, JUNE 2004	Heng Tang, Member, IEEE, Jun Xu, Member, IEEE, Yu Kou, Shu Lin, Life Fellow, IEEE, and Khaled Abdel-Ghaffar, Member, IEEE	1. Cyclic or quasi-cyclic LDPC codes have encoding advantage over other types of LDPC codes. Their encoding can be implemented using simple shift registers with complexity linearly proportional to the number of parity bits.	
4	A Flexible Hardware Encoder for Low-Density Parity-Check Codes	Proceedings of the 12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'04)	Dong-U Lee and Wayne Luk, Connie Wang, Christopher Jones, Michael Smith, and John Villasenor	1. LDPC codes achieve better performance and lower decoding complexity than Turbo codes. 2. LDPC codes have excellent performance and the large degree of parallelism that can be exploited in the decoder. 3. Information block lengths are long enough in LDPC. 4. LDPC codes exhibit an asymptotically better performance than Turbo codes and admit a wide range of tradeoffs between performance and complexity	1. Major drawback of LDPC codes is their apparently high encoding complexity. Complexity means number of mathematical operation required per bit.

5	Codes on Finite Geometries	IEEE TRANSACTIONS ON INFORMATION THEORY, VOL. 51, NO. 2, FEBRUARY 2005	Heng Tang, Member, IEEE, Jun Xu, Member, IEEE, Shu Lin, Life Fellow, IEEE, and Khaled A. S. Abdel-Ghaffar, Member, IEEE	1. Finite-geometry codes have reasonably good minimum distances and are simple in decoding with majority-logic. 2. Finite-geometry codes allow relatively low-speed implementation at higher cost than BCH codes and Reed-Solomon codes. 3. Finite-geometry LDPC codes have good minimum distances and their Tanner graphs are free of cycles of length. These properties allow them to perform well with iterative decoding using the sum–product algorithm (SPA). 4. Long finite-geometry codes decoded with SPA perform close to Shannon's theoretical limit, which is the minimum signal-to-noise ratio (SNR) required to achieve essentially error-free communication. 5. A very important feature of finite-geometry LDPC codes is that they are either cyclic or quasi-cyclic. As a result, their encoding can be implemented in linear time with feedback shift registers. 6. Finite-geometry LDPC codes can be decoded with various other decoding methods besides SPA, such as majority-logic (MLG) decoding, bit-flipping (BF) decoding, weighted MLG decoding, weighted BF decoding, and a posteriori probability (APP) decoding.	
6	Programmable Low-Density Parity-Check Decoder	IEEE, 2004	Gabofetswe Malema, Michael Liebelt	1. These architectures trade off error correcting performance for reduced implementation complexity through structured code construction. 2. Semi-parallel and scalable LDPC architectures provide the framework that allows the designer to trade off code flexibility, hardware costs and area. 3. It also offers flexibility in structured code design, easy execution control and node mapping. 4. The architecture is easily reconfigured from fixed to full flexibility. 5. Partly or semi-parallel designs reuse hardware to reduce cost.	1. Semi-parallel and scalable LDPC architectures impose constraints on the code matrix to extract some parallelism and scalability and avoid communication conflicts. 2. Partly or semi-parallel designs have to deal with the issue of memory conflicts and complex control and addressing.

7	CODE DESIGN AND DECODER IMPLEMENTATION OF LOW DENSITY PARITY CHECK CODE	IEEE,2005	Mong-Kai Ku, Huan-Sheng Li, Yi-Hsing Chien	1. LDPC codes provide excellent error correcting capabilities. 2. LDPC codes provides implementation friendly decoding algorithm. 3. By changing the block size and rate of LDPC code, it is easy for system designers to make trade-offs between error correcting performance and hardware complexity, making the LDPC code suitable for a wide range of applications. 4. The regular quasi-cyclic LDPC parity check matrix also simplify the hardware architecture, and make overlapping pipelining and multithread decoding easier to handle. 5. LDPC code exhibits equal or better performance to randomly generated LDPC codes with short to medium block sizes. 6. The overlapped pipelining architecture with Jump-Reset scheduling provides very high hardware utilization with efficient memory usage.	
8	Code Construction and FPGA Implementation of a Low-Error-Floor Multi-Rate Low-Density Parity-Check Code Decoder	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 53, NO. 4, APRIL 2006	Lei Yang, Student Member, IEEE, Hui Liu, Senior Member, IEEE, and C.-J. Richard Shi, Fellow, IEEE	1. The LDPC decoding algorithm is inherently parallel and is easy to be implemented. 2. It can be applied in optical networking, magnetic recording, digital video broadcast satellite (DVB-S) communications and other fields.	
9	A Comparative Performance and Complexity Study of Short-Length LDPC and Turbo Product Codes	IEEE,2006	Mohamed Adnan Landolsi	1. The LDPC codes are of the semi-random (SR) type, characterized by low encoder complexity, and are further optimized by eliminating short cycles of length 4 (minimum girth 6). 2. The SR-LDPC codes have slightly better error performance (to within 0.5dB, at a BER of 10-5) while demonstrating lower computational complexity per decoder iteration. 3. SR-LDPC codes have a more competitive performance-complexity advantage overall. 4. SR-LDPC codes have slightly better SNR performance (to within half a dB, at BER of 10-5) while at the same time having lower computational complexity per decoder iteration.	1. In SR-LDPC codes required number of decoding iteration is larger.

4. Conclusion

Survey of above listed paper in tabular from we concluded the following

In error correction and detection codes bit error performance should approach asymptotically the Shanon limit, LDPC codes fulfils these criteria. Also the implementation of decoder should be simple. The regularity and structure of LDPC codes simplifies the decoder.

In communication SNR (signal to noise ratio) must be high. In LDPC codes large girth improves the SNR, but geometry based design of LDPC codes provides low SNR than turbo structured LDPC codes. Bit error rate (BER) performance of any error correction codes must be high. Multi-input multi-output LDPC (MIMO-LDPC) can achieve better BER than multi-input multi-output turbo (MIMO-Turbo) on fast fading channel. Decoder of any error detection and correction codes must smaller. Multi-input multi-output LDPC turbo (MIMO-LDPC-Turbo) incorporates smaller decoder.

Major drawback of LDPC codes is its high encoding complexity i.e. number of mathematical operation required per bit, which should be less. Also semi-parallel LDPC architecture imposes constraints on the code matrix to extract some parallelism and avoid communication conflicts which may be advantageous but drawback of these

is memory conflicts and complex control and decoding. In semi-random LDPC (SR-LDPC) codes required number of decoding iteration is larger which must be smaller. But advantage of SR-LDPC is that it provides high SNR.

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