Design and Implementation of Phase Frequency Detector with High Performance

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Abstract: ***In this paper introduced the Design and implementation of Phase Frequency Detector with high performance. The Phase Frequency Detector is the major part of Phase Locked Loop (PLL). A PLL is a close loop frequency system that lock the phase or frequency of an output signal to an input reference signal .The term lock refers to a constant or zero phase or frequency signal difference. In the PLL, Phase Frequency Detector is compares the output frequency / phase with the input frequency/ phase. The Phase Frequency Detector (PFD) is the first block of the PLL. The PLL is noise sensitive electronic device, and due to noise, performance of the PLL is poor. To overcome this we used PFD (Phase Frequency Detector) is have 4states. The PLL is work in different mode, the Lock mode and Unlock mode. It also have better phase characteristics. This design and implementation work is done in Zeni Electronic Design Automation (EDA) environment tool.***

Keywords: Phase Locked Loop, Phase Frequency Detector, Voltage Control Oscillator ,Charge Pump.

1. Introduction

Over the last decades, the path of CMOS technology scaling has been accompanied by the trend of digitization in the hardware realization of circuits and system to exploit the finest process node available for the cost reduction [1]. A Phase-Locked Loop (PLL) is an electronic feedback system that generates a signal, the phase of which is locked to the phase of an input reference signal. A DPLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. [5]

A DPLL is can be utilized for frequency synthesis, frequency multiplication, carrier recovery, frequency division and frequency demodulation. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant [16].

A basic form of a DPLL consists of five main blocks Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), Voltage Controlled Oscillator (VCO), Frequency divider[7].

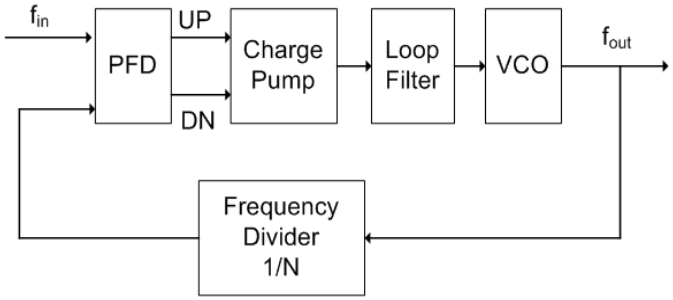

Figure 1: Basic block diagram of PLL

A challenging work in the CMOS technology is to design a low phase noise ring oscillator for a charge pump Phase Locked Loop using CMOS technology. A design is to improve the overall characteristics of DPLL.A charge pump circuit is used to convert the digital signal from the phase frequency detector to analog signal .The output of which is used to control the frequency of the voltage control oscillator.

The Loop filter (LF) that smoothes the PD output signal and applies it to the VCO input. Voltage-controlled oscillator (VCO).The output frequency of these devices is a monotonic increasing function of its input voltage .Frequency divider (FD). The output of the frequency divider is a signal with a frequency equal to the VCO output frequency divided by a division factor N. The first component of PLL is the PFD (Phase Frequency Detector), which has been designed

to improve of the PLL because it has been minimizing the dead zone.

2. PLL Architecture

A PLL is essentially a feedback loop that locks the on-chip clock phase to that of an input clock or signal.[14] Phase locked loop is closed loop control system that compares the output phase with the input phase. A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock.

A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL is a negative feedback control system circuit.[14].

A basic form of a PLL consists of five main blocks:

- Phase Frequency Detector(PFD)
- Charge Pump(CP)
- Loop Filter(LF)
- Voltage Controlled Oscillator(VCO)
- Frequency Divider(FD)

2.1 Phase Frequency Detector

The phase frequency detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. If there is a phase difference between the two signals, it generates up or down synchronized signals to the charge pump/ loop filter.

2.2 Charge Pump

A charge Pump circuit is used to convert the digital signal from the phase frequency detector to analog signal. The output of which is used to control the frequency of the voltage. It have two input UP and DN. When PFD goes "UP" signal high ,the PMOS will turn on. This will connect the current the current source to the loop filter. It is in similar way when the PFD "DN" signal goes high.

2.3 Loop Filter

The function of the loop filter is to covert the output signal of PFD to control voltage and also to filter out any high frequency noise introduces by the PFD.

2.4 Voltage Controlled Oscillator

The operation of Voltage Controlled Oscillator is similar to the ring oscillator. It is the heart of Phase Locked Loop.If the error signal from the PFD is an up signal, then the charge pump pumps charge onto the LF capacitor which increases the voltage V control. On the contrary, if the error signal from the PFD is a down signal, the charge pump removes charge from the LF capacitor, which decreases V control[14]. V control is the input to the VCO.

2.5 Frequency Divider

The frequency of oscillation is divided down to the feedback clock by a frequency divider. The phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock. Because the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is N times the reference clock.[7]

3. Methodology

The Phase Frequency Detector (PFD) is the first block of Phase Locked Loop (PLL), where we compare the reference signal and the feedback signal with respect to phase and frequency. In this PFD it is the arrangement of D_FF , Inverter and Buffer.

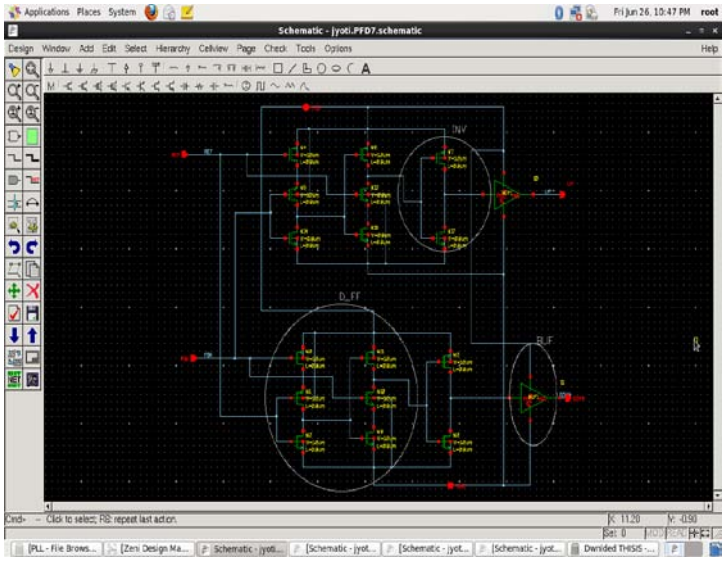

Figure 2: Schematic of Phase Frequency Detector

The new proposed PFD have 2 input REF signal and FBK

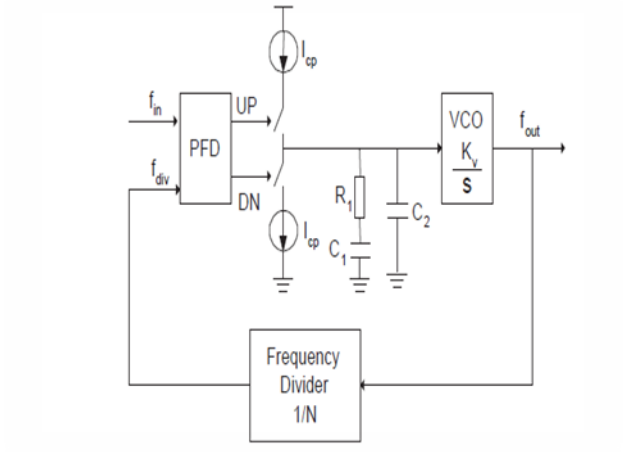

Figure 3: Charge Pump Phase Locked Loop

Signal and 2 output signals UP signal and DN signal. Where PFD is response in the form of UP signal and DN signal with respect to REF signal and FBK signal.

1. When REF signal is lead from the FBK signal then UP is response and give high pulse.
2. When FBK signal is lead from the REF signal then DN is response and give high pulse.
3. When REF signal is same phase and frequency with FBK signal, at that time both pulse is seems like small hike pulse.

This type of arrangement is used in Charge Pump Phase Locked Loop. This is very efficient type of Phase Locked Loop.When the PFD is in positive state (UP is high), a current *Icp* flows out of the charge-pump and charge the loop filter. When the PFD is in negative state (DN is high), a current *Icp* flows in the PFD and discharges the loop filter. when the PFD is in zero state means no phase error is occur there is no current flows in or out of the charge pump , there for the loop filter voltage keep constant[16]. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an ―up signal, the VCO speeds up. On the contrary, if a ―down signal is generated, the VCO slows down.

4. Output Waveforms

In the Designing and Implementation of Phase Frequency Detector with high performance in Zeni EDA tool and successfully run in 180 nm technology. For high performance Phase Frequency Detector we use 3 state of working, by this we are minimize the error signal as well as dead zone problem. High speed phase frequency detector is proposed for PLL design. The proposed phase frequency detector is simple in its structure and has no glitch output as well as better phase characteristics.

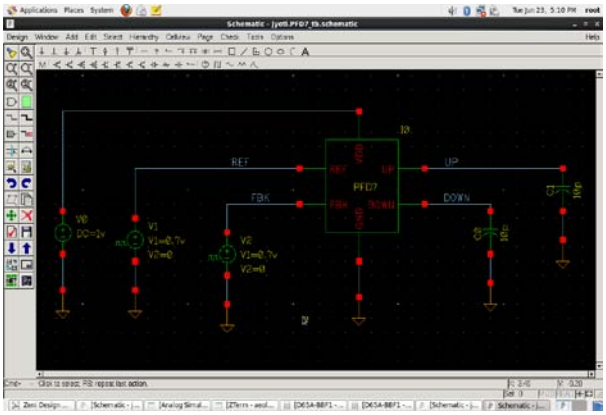

Figure 4: PFD with Input and Output

. For UP Response;

- When the Phase of "ref" signal is leading from "fbk" signal then "up" signal will going to high.
- The Inputs are as "ref" signal is in Green signal and "fbk" signal is in Yellow signal.
- The Outputs are as "up" signal is in Blue signal and "down" signal is in Pink signal.
- Error signal is generated in PFD in form of "up", in that below figure "ref" signal is lead from the "fbk" signal.

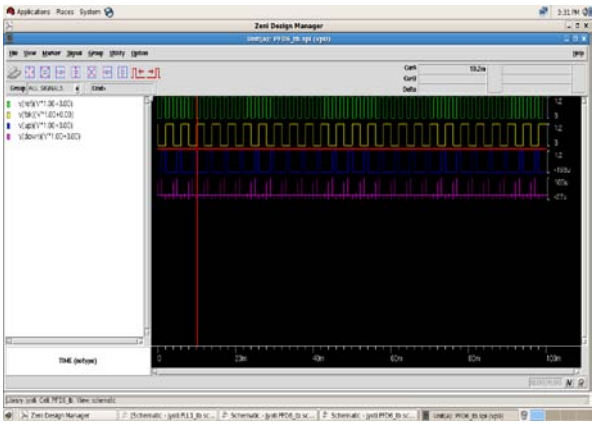

Figure 5: PFD "UP" is responding

2 For Down Response;

- When the Phase of "ref" signal is lagging from "fbk" signal then "down" signal will going to high.
- The Inputs are as "ref" signal is in Green signal and "fbk" signal is in Yellow signal.
- The Outputs are as "up" signal is in Blue signal and "down" signal is in Pink signal.
- Error signal is generated in PFD in form of "down", in that below figure "FBK" signal is lead from the "REF" signal.

Figure 6: PFD "down" is responding

3 For Same Phase & Frequency

- When the Phase of Reference signal is lagging from Feedback signal then "DOWN" signal will going to high.
- The Inputs are as Reference signal is in Green signal and Feedback signal is in Yellow signal.

- The Outputs are as UP signal is in Blue signal and DOWN signal is in Pink signal. Error signal is not generated.
- In this state PFD is in Zero state, means the "ref" signal is same in phase/ frequency to the "fbk" signal.

(3) For Same Phase & Frequency

- When the Phase of "ref" signal is lagging from "fbk" signal then "down" signal will going to high.
- The Inputs are as "ref" signal is in Green signal and "fbk" signal is in Yellow signal.
- The Outputs are as "up" signal is in Blue signal and "down" signal is in Pink signal. Error signal is not generated.
- In this state PFD is in Zero state, means the "ref" signal is same in phase/ frequency to the "fbk" signal.

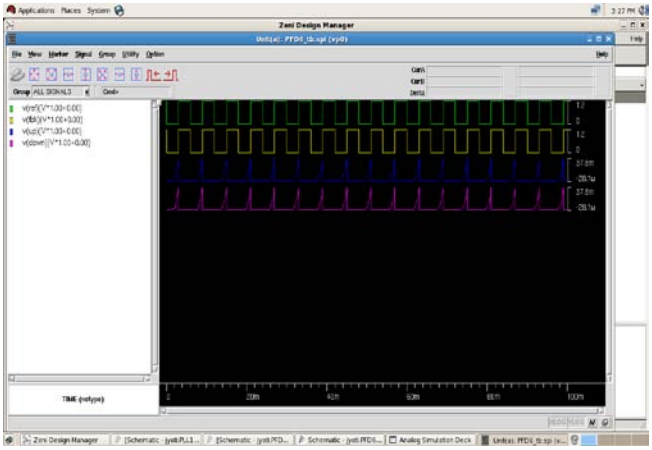

Figure 7: PFD for same Phase/Frequency signal

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