6. Conclusion

From the literature survey, the research done and the results obtained we can easily deduce that though using Vedic multiplier itself implemented in CMOS logic was providing us with the reduced power dissipation implementing it using the DCPAL logic would further reduce the power dissipation by a massive 61.44%. Thus it would be more practical if we could use the DCPAL logic in combination with the CMOS logic as there will be power recovery too happening due to the DCPAL logic and faster processing and improved latency due to the Vedic methodology.

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