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Optimized Design of a 2x2 Multiplier using a Combination of Vedic Mathematics and DCPAL Logic

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Abstract: ***Modern day processing requireshigh speed and less power consumption logic techniques. For a DSP, a microprocessor, an FFT or any other application where speed is needed we can use a multiplier. Vedic mathematics has served us well in making the mathematical calculations easier and simpler. We use Urdhwa-Tiryagbhyam sutra from the Vedic mathematics to implement a 2x2 Vedic multiplier. The adiabatic logic has been playing a prominent role in the reduction of the power dissipation using the energy recovery technique. We in our paper propose an efficient 2x2 multiplier by combining these two techniques.***

Keywords: Vedic mathematics, DCPAL logic, CMOS, Urdhwa-Tiryagbhyam Sutra

1. Introduction

A detailed description about the multiplication algorithms have been discussed in the literature [2]. It states that Baugh-Wooley multiplier is suitable for less bit operands and for higher bit operands we just use the booth algorithm. But it should be kept in mind that the booth algorithm incurs higher power dissipation any other modern techniques currently being used also incur a lot of power dissipation. Though Wallace tree multiplier combined with modified Booth algorithm achieves better speed it is not practical to rely on it because of the increased number of interconnects resulting in greater chip area and thus higher power dissipation.[4]

The Vedic mathematics has given a compact and reliable path for modern day computations by providing us the sutras extracted from the ancient Vedas. The Urdhwa-Tiryagbhyam sutra adopted from the latter gives us an efficient from of achieving increased speed and reduced power in the multipliers when compared with the Baugh-Wooley multipliers[5][6].

The adiabatic logic is a highly reliable methodology for low power applications. The circuit recovers full or partial energy from the nodal capacitances using a special power clock [6] the power clock basically has two functions it provides energy to the circuit and also maintains the timing across the pipelined circuit. In the implementation we use Differential Cascode Pre-resolve Adiabatic Logic (DCPAL) method [8] which provides enhanced energy recovery and reduces the non adiabatic loss. This is achieved as there is no direct path between the supply rails. Using four phase clocking provides better efficiency. But we just need two phase clocking for the implementation of our design.

The paper is divided into four sections Section I dealt with the introduction, Section 2 shall put light upon the different Vedic sutras, Section 3 shall be dealing with the implementation of a 2x2 Vedic multiplier in CMOS logic and Section 4 shall explain about the combination of Vedic and DCPAL logic. Section 5 shall show the simulation results and shall also be dealing with the comparison of results.

2. Vedic Mathematics

Vedic mathematics is extracted from the four Vedas (book of wisdom). The sutras extracted from these gives us a complete explanation of several mathematical terms including arithmetic, geometry, trigonometry, quadratic equation, factorization and even calculus.
Vedic mathematics is divided into 16 different sutras dealing with variousbranches of mathematics like arithmetic, geometry etc.The sutras along with their brief meanings are enlisted below:

1. (Anurupye) shunyamanyat- If one is in ratio, the other is zero.
2. Chalana kalanabhyam - Differences and Similarities.
3. Ekadhikina Purvena - By one more than the previous one, it is used to find the square of numbers and divisions like 1/19 or 1/29….. 1/199.
4. Ekanyunena Purvena - By one less than the previous one.
5. Gunakasamuchyah - The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product, to verify the answer obtained.
7. Nikhilam Navatashcaramam Dasatah - Nikhilam means positive. It is used to subtract number from the nearest power of 10 i.e., 10,100,1000 etc. i.e.,all from nine and last from ten
8. Paraavartya Yojayet - Transpose and adjust, divide large number from smaller.
9. Puranapuranabhyam - By the completion or noncompletion
10. Sankalana – Vyavakalanabhyam - By addition and subtraction
11. Shesanyakena Charamena - The reminders of the last digit
12. Shunyam Saamyasamucccaye - When the sum is the same that sum is zero
13. Sopaantyadvayamantyam - The ultimate and twice the penultimate
14. Urdhva – Tiryagbhyam – Vertically and Crosswire
15. Vyashtisamanstih – Part and whole
16. Yaavadunam – Whatever the extent of its deficiency, to find the square of number near or lesser to powers of 10.

Of all the available sutras we are using the Urdhva Tiryagbhyam sutrawhich is a general multiplication formula is applicable to all cases of multiplication.It literally means vertically and crosswire, which provides parallelism in generation of partial products and their summation.It has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Thereforeit is time, space and power efficient.

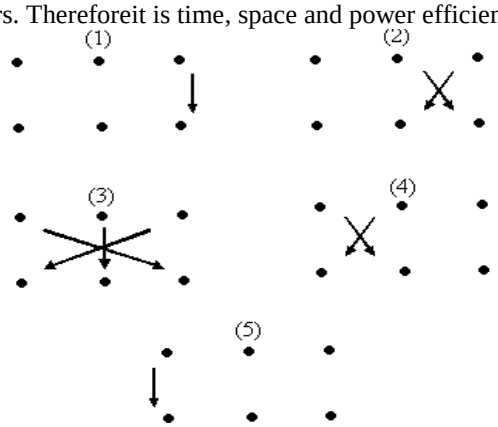


Figure 1: Figure showing the general method followed in UT system of multiplication.

3. CMOS implementation of a 2x2 Vedic multiplier

The Vedic multiplier is implemented using six AND gates and one XOR gate. The truth table of the vedic 2x2 multiplier leaves us with the following Boolean equations. For the implementation we have used Cadence Virtuoso tool (IC615) and for simulation, MMSIM v.13 was used. The technology used was gpdk180. The VDD given for Vedic multiplication was 5V.

Q0 = (A0 AND B0)
Q1 = (A0 AND B1) XOR (B0 AND A1)
Q2 = (A1 AND B1) AND (A0 AND B0)
Q3= (A1 AND B1) AND (A0 AND B0)

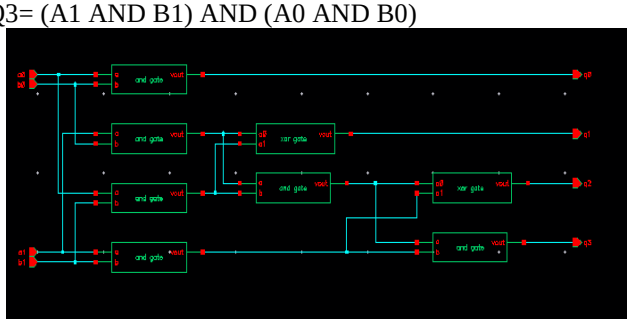


Figure 2: Figure showing the CMOS implementation of a Vedic multiplier (the gates used are designed using CMOS technology)

4. Combination of Vedic multiplication method with the DCPAL logic

The DCPAL logic recovers energy from the nodal capacitances. This method is used to design individual blocks such as logic gates and adders. DCPAL is a dual rail pre-resolve logic circuitry designed using NMOS based Differential Cascode Voltage Switch (DCVS) tree structure and PMOS sense amplifier memory recharge scheme that helps achieving efficient energy recovery. The specialty of this circuit is that it produces both the output and its compliment in the same circuit. Thus reducing complexity of the circuit and improving the overall latency [8].

For a better understanding we present a DCPAL NAND/AND circuit in fig 3.

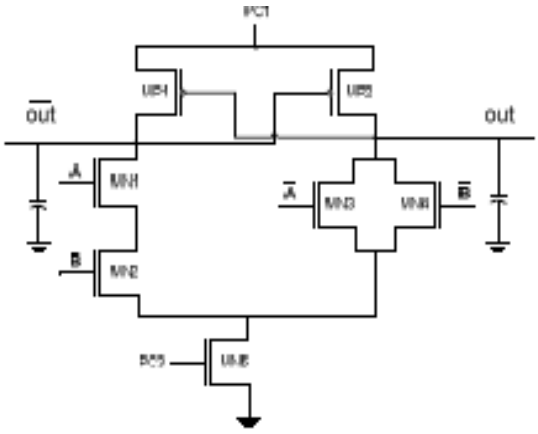


Figure 3: Figure showing the circuit implementation of a DCPAL NAND/AND block.[1]

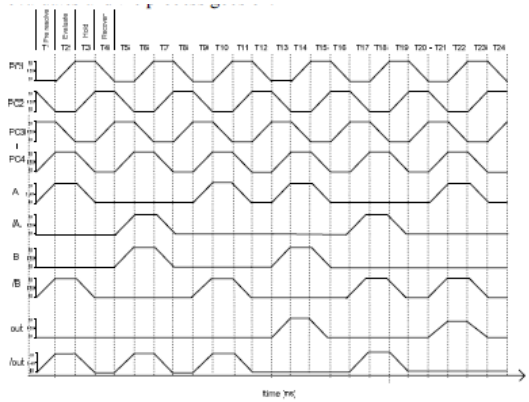


Figure 4: Figure showing the results of a DCPAL NAND/AND circuit. [1]

The fig 4 shows the graphical representation of the results obtained for the DCPAL NAND/AND logic circuit. The circuits can be simulated in any suitable simulator tool. The circuit works as follows. The circuit works as follows, when the inputs is at hold phase and the PC1 clock is at the evaluate phase the logic is evaluated to zero or one according to the inputs provided. At this phase the charge shall be stored at one node and shall be recovered in the recovery phase when the PC3 clock shall be at the evaluate phase. The DCPAL logic was again implemented in Cadence Virtuoso (IC615) at 180 nm technology. PC1 and PC3 were 180^0 mutually phase shifted clocks at 50% duty cycle, having a peak value of 5V.

When we combine these two logic families because of time reduction and latency improvement of Vedic circuits and the energy recovery logic of the DCPAL logic, a drastic reduction in power was seen which could change the path of current design industry.

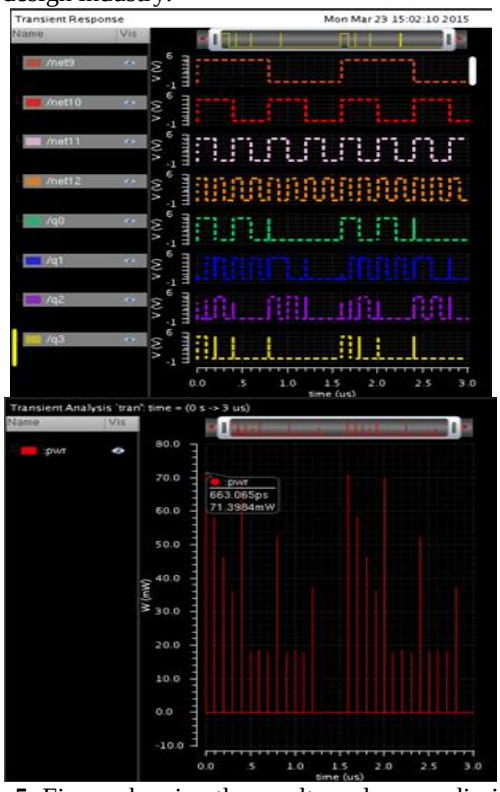


Figure 5: Figure showing the results and power dissipation of a CMOS logic Vedic multiplier circuit. [1]

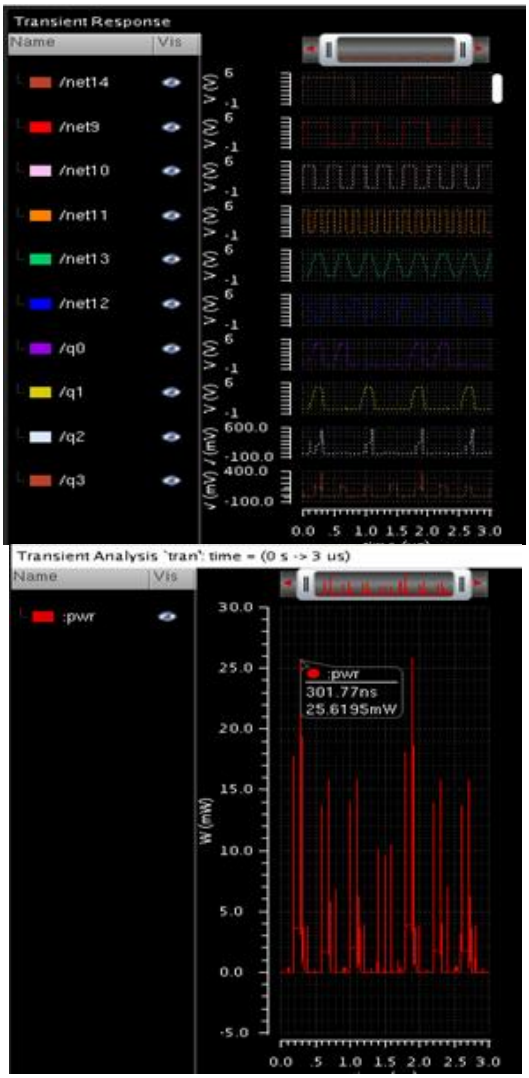
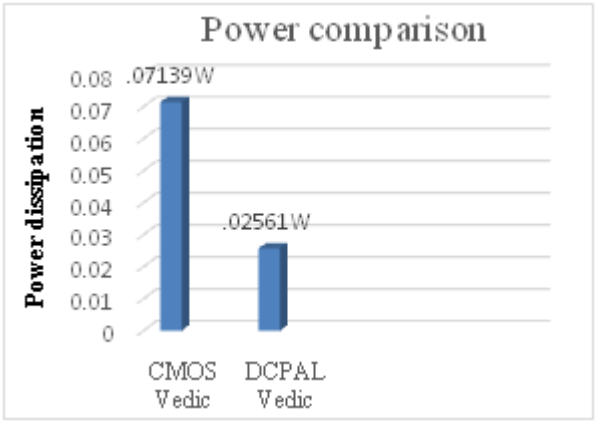


Figure 6: Figure showing the results and power dissipation of a DCPAL logic Vedic multiplier circuit.

5. Results comparison

The circuit that used only CMOS logic to implement the Vedic multiplier showed us a power dissipation of 71.3984mW and the circuit that used DCPAL in combination with the Vedic logic gave us a power dissipation of 25.6195mW. Table 1 shows the comparison of the results obtained for two different cases i.e., CMOS Vedic multiplier and

Table 1: Comparison of power dissipation between CMOS Vedic multiplier and a DCPAL Vedic multiplier



6. Conclusion

From the literature survey, the research done and the results obtained we can easily deduce that though using Vedic multiplier itself implemented in CMOS logic was providing us with the reduced power dissipation implementing it using the DCPAL logic would further reduce the power dissipation by a massive 61.44%. Thus it would be more practical if we could use the DCPAL logic in combination with the CMOS logic as there will be power recovery too happening due to the DCPAL logic and faster processing and improved latency due to the Vedic methodology.

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