Negative Feedback with an Integrator as A Central Element

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Abstract: *Negative feedback is introduced with an integrator as the central element by the intuitive connection with the way we are aware of the difference between the desired and actual values and constantly this so that it reaches the desired value. In contrast to the traditional use of a memoryless High Gain Amplifier as the central element, it is with this approach from the outset a clear thing that negative feedback circuits take the time to respond have a limited bandwidth), some excessive delay that can be tolerated, while larger on delays lead to ringing, and finally, political instability, and the negative feedback circuits can be stabilized by slowing. Time domain intuition and analysis lead to important conclusions with regard to the stability margin of negative feedback circuits. This approach complements the conventional frequency domain approach by the as the entry point, the results, from this. The presented approach is better suited for the synthesis of the most important negative feedback blocks such as amplifiers, and the Phase Locked Loop.*

Keywords: Negative feedback, integrator

1. Motivation

A graduate course in analog integrated circuit design includes a discussion about negative Feedback circuits and stability, Design of operational amplifiers, and their frequency compensation schemes. This white paper describes a system for the development of these themes, the differs from the traditional approach in teaching and textbooks (for example, the [1], [2]). The reasons for the participation in this approach are as follows:

- Time domain argument is intuitive, but the precise analysis with any signals is usually difficult or even impossible. Spectral analysis is easier, but at a higher level of abstraction. Therefore, it is often best to introduce students to the natural intuition in the time period in the first statements that you anticipate the results, and continue with the frequency range for exact calculations with the help of the Laplace transformation.
- The participants grasp the material better if they said, Why the system is as it is, rather than simply to show that you and analyzing it.

None of the results in this paper is new. It is well known and taught for decades, usually using the traditional frequency domain approach. What is shown here is an alternative perspective with regard to negative feedback circuits which the author believes is more intuitive and more efficient in terms of communication of key concepts in the classroom. Important results on negative feedback systems can be derived from this time

Domain approach, it can also be an introduction to the topic. How is later in this document, this method, it is clear right from the beginning that negative feedback circuits take the time to reply (i.e. you have a non-zero time constant or a finite bandwidth), that some delay can be tolerated while larger delays lead to ringing, and finally instability that negative feedback circuits can be stabilized by slowing you down, and the negative feedback circuits are usually slower than open circuit. Frequency domain approach for accurate analysis of complex circuits you can this introduction. The results of the by the Commission for certain electrical circuits can be connected to the earlier General conclusions from the time domain analysis. The presented approach is better suited for the synthesis of the most important negative feedback blocks such as the Phase Locked Loop[3).

The next section gives an overview of the traditional classroom introduction to negative Feedback circuits and discussed certain shortcomings in the field of it. Section III uses them to determine the nature of the negative feedback system by drawing analogies with manual adjustment of quantities in everyday life. It is seen that the central element of the negative feedback system is an integrator. The prototype negative feedback amplifier is in section IV. The op amp is introduced as a practical building block of negative feedback systems in Section V Section VI briefly describes the step response of the amplifier in the ideal case. The behavior of the system with an additional delay in the loop is discussed in Section VII and intuitively the results of its analysis are set out in section VIII. The proposed flow of the topics in the classroom and in the connections between the time domain analysis presented here and the traditional frequency range view are in Section IX. Section X concludes the paper.

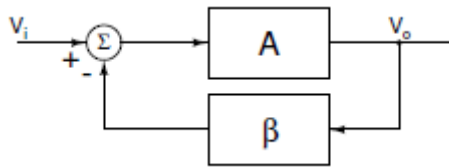## 2. Traditional introduction in negative feedback circuits

Figure 1: Block diagram traditionally used, a negative feedback

Traditionally([1], [2]) Negative Feedback circuits are introduced by the classical block diagram in fig. with 1, analysis of it, and showing that the loop gain *Vo/ Vi* approaches 1 /Î² if a beta≫1. Replacing a by a operational amplifiers and beta by a resistor divider results in the classic, non-inverting amplifier.

The author feels that this approach has some shortcomings in the use in the classroom - especially when some questions unanswered until later, if you want to make a complete analysis has been carried out, including details of the electrical circuits. Without justification why the topology is as it is in Figure 1. Many times, the negative feedback action is described under the assumption that there is a value other than zero error voltage *Ve and* indicating that the feedback will be in the opposite polarity, that somehow have reduced . But, the circuit is so algebraic, and does not allow an error Ve , is developed in the course of time (for a constant input signal). In addition, if a delay is added to the loop as in Figure 1, the system is unstable for arbitrarily small values of delay. This is in contrast to our intuition, the view that the system should remain stable for the small enough delays. Finally, no negative feedback system has a frequency independent behavior implied in Figure 1, whereas a large class of them has a first order(1 / s) frequency dependence in some significant range of frequencies. For this reason, it is only fair to treat depending on the first, or an integrator with similar behavior as an essential feature and are not considered to be a failure to cope with.[1]

3. Integrator as the controller in a negative feedback system

The intuitive idea of negative feedback as a system that detects that the output, compares it with the desired value, and always drives the Output until it reaches the desired value is very easy to explain to the students. For example, when driving a car or listening to a radio, you can feel the difference between the desired and actual speed or volume and continuously adjusts the latter until the desired values are reached. Figure 2 (a) describes the idea. It should be noted that you do not know how the output immediately to the correct value as implicit of figs. 1, BUT the it is the process of continuous recording and setting that as a driver for the output to the correct value. Also, intuitively, if the measured performance is very close to the desired value, you can ride the output slightly downwards, so that it slowly (for example the car is accelerated slightly) if the measured performance is far from the desired value, it is so strong that the output changes faster.

The problem is now in the hands is, the nature of the controller in figure 2 (a). The simplest way to do this is by assuming that the output of the sensor is blocked. In this case the error input to the controller is a constant (Figure 2 (b)) and the output(fig. 2 (C)) is constantly on the increase. This is analogous to the continuous acceleration and increase in speed when the speedometer is stuck. For a smaller error, the output was up dimensions) more slowly. The rate of change of the controller the controller output is proportional to the error between the measured and the desired output. From this, it can be deduced that the desired shape of the driver in Fig 2 (a) is an integrator. The output of the controller is the integral of the input(error between the desired and actual outputs) in the course of time. Figure 2 (d) shows the feedback system with an integrator as the controller.
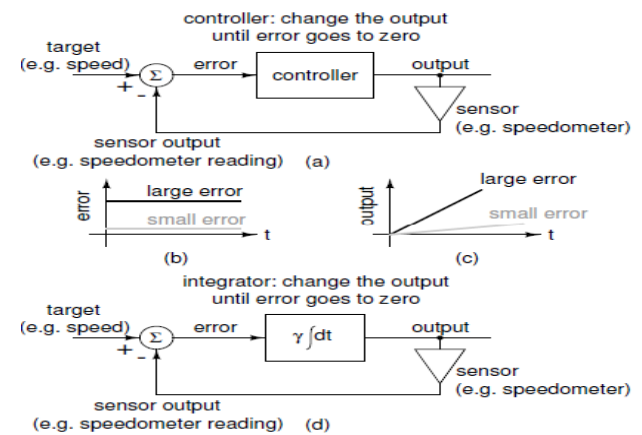

Figure 2: (A) conceptual diagram of a negative feedback system, (b) errors in the sensor is stuck, (c) is output when the sensor is stuck, (d) Negative Feedback system with an integrator as a controller(Î³ is a constant with the appropriate

Figure. 2 (A) is the classic block diagram textbooks used in the control systems, the concept of feedback-control(e.g. [4, Fig. 1.13]). What is in this paper is that the idea of continuous adjustment leads to the controller, an integrator(fig. 2 (D)) and that the system with the help of an integrator is used leads to a gentler introduction to negative feedback in the classroom with a memoryless as the amplifier (fig. 1).
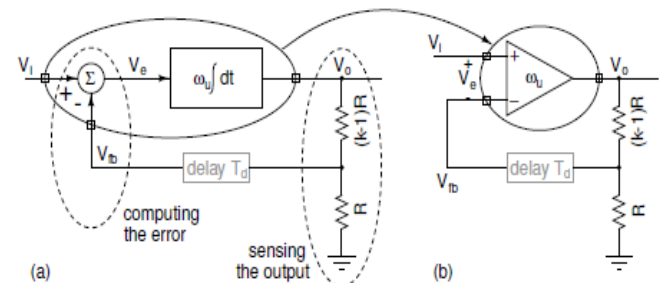

Figure 3: Computing error

4. Integrator as the controller in a negative feedback system

In terms of design, we are mainly interested in with negative

feedback amplifier. An amplifier of gain K with an output voltage Vo and an input voltage VI (is assumed to constant over time) follows the ratio $Vo = KVI$. For the implementation of this with negative feedback, we define the desired value to be VI and the measured value to be Vo/k ,so that, if the measured value is driven to be equal to the desired value, the relationship from is valid. Translation of 2 (c) With these definitions, the prototype negative feedback amplifier in Fig. 3 (a). The sensor is a resistive voltage divider $1/k$. By inspection, it is clear that, steady-state occurs only when $Vo = KVI$ and all other values of the Vo leads to a permanent change in the output.

Fig. 3. (A) negative feedback amplifier with an integrator. Ω_u $_{is}$ a constant with the dimensions of the frequency. Assume that the delay TD is zero until Section VIII. (B) Operational amplifiers as a combination of error calculation and integration. The resulting amplifier. is the classic non-inverting amplifier.

5. Integrator as the controller in a negative feedback system

The essential operations in a negative feedback amplifier are: (a) the difference between the desired and the measured values for the calculation of the error and (b) the integration of the error. The combination of these features a circuit has been a very useful building block, and is nothing other than the ubiquitous op amp(fig. 3 (B)). Ω_u is a parameter of the op amp. It is the slope of the output for a unit. It is also the *Unity Gain Frequency of the* operational amplifiers the magnitude.[2]

6. Step response to the negative feedback amplifier

If a step size VP is applied as the input VI *with the* amplifier in the picture. 3, assuming a zero initial condition, the error voltage Ve is equal to the input step at $T = 0 +$. rampsup to a set ω_{EIA}, and the feedback signal Vfb ramps up to a set $(\Omega_u$ $_{/k})$ VP. As *the VFB* increases, Ve reduced, and the speed at which the number of Vo (and Vfb) reduced. The system has a time constant $(k/\omega_u$ $_)$ asymptotically reached steady-state with $Vo = KVI$ (and $Vfb = vi$). This is the well-known behavior is detected by the differential equation and its solution (for a step VP) as below

$$\frac{1}{\omega_u}\frac{dV_o}{dt} = V_i - \frac{V_o}{k} \qquad (1)$$

$$V_o(t) = kV_p\left(1 - e^{-\frac{\omega_u}{k}t}\right) \qquad (2)$$

7. Bare with delay in the loop –Intuition

So far, the description of the negative feedback amplifier (fig. 3) implies that the actual output is immediately detected and the controller responds instantaneously to the resulting error between the desired and the measured value. In practice, there are delays in the loop. The qualitative effects are easy enough to present themselves. Again it is assumed that the first condition zero for the integrator and a step input amplitude VP. There will be a non-zero delay Td in the feedback path. After the step is applied for a duration of TD, the feedback *for Vfb* remains at zero and the error V $_e$ $_{remains}$ at VP. In the delay-free case, the feedback signal would have started, and take the exit to top of t $= 0 +$ at a rate $(\Omega_u$ $_{/k})$ VP. For a small delay $(TD \ll k/\omega_u)$, the delay-free feedback at $T = TD$ would be approximately $(\Omega_u$ $_{/k})TdVp$ and the corresponding error would be $VP - (\Omega_u$ $_{/k}) \approx$ $TdVpVP$. Because of the difference in the error signal between the delay-free and delayed feedback cases is small, one would expect that, for TD $\ll (k/\omega_u$ $_)$, the behavior is similar to the delay-free case.

For larger delays, say $TD = (k/\omega_u$ $_)$, for the period up to the TD , the output builds kVp, the desired steady-state output. Since Ve starts to decrease from the initial value VP only after t $= TD$, the output ?on the desired value and continues to rise due to the positive value of Ve.The error voltage Ve is to reduce negative and causes Vo only if the late feedback Vfb crosses vp at $T = 2$ TD The output Vo then crosses CIP *in* the other direction, but there is a delay of TD before this reversal is fed back .The performance varies around the desired steady state of the CIP .

From this, one can deduce that, should the TD is so large that Vo shoots two times in the steady-state value of the kVp or greater, the system would never recover, because the excess in each direction is always greater. Similarly, if the excess is only a small fraction of the steady-state value of the kVp, the shoots are always smaller and eventually die. As already described, the difference between the feedback signals in the delayed and undelayed cases $(\Omega_u$ $_{/k})TdVp$. To reduce this difference, one must either (a) reduce the delay (if possible), or (b) to reduce $(\Omega_u$ $_{/k})$ (the rate at which the feedback signal ramps first), d. h. "Slow down" the integration, not much will change over the duration of the delay. These two points capture the essence of the stabilisation techniques negative feedback system. The second point above also shows that there is a technical limitation of the speed or bandwidth of a negative feedback system, since the minimum delay, is feasible in the respective technology. As already mentioned in the introduction, appreciate these points before diving into the analysis offers a much better motivation to use the second method.

8. Bare with delay in the loop –Intuition

With a non-zero delay in Fig 3 (a), the differential equation for the amplifier is

$$\frac{1}{\omega_u}\frac{dV_o(t)}{dt} = V_i - \frac{V_o(t - T_d)}{k} \qquad (3)$$

This is a delay differential equation, delayed feedback[6]. This equation can be solved in the time domain with a little

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Algebra and familiarity with the ordinary differential equation in eq. 1. Due to lack of space, the analysis is not shown here. The main features of the solution are (*e* is the natural exponent):

- For TD < $1 / E \cdot k/\omega_u$ the step response shows no overshoot. This is analogous to overdamped Josephson contacts which are operated Josephson-contacts, answer in a second order system.
- When td = $1 / E \cdot k/\omega_u$ the step response shows no overshoot. This is analogous to critical muted response in a second order system. $TD = 1 / E \cdot k/\omega_u$ $_{is}$ the maximum deceleration possible without overshoots.
- $1 / E \cdot k/\omega_{u <} TD < \pi /2 \cdot k/\omega_u$ the step response rings before. This is analogous to the underdamped response in a second order system.
- For $\pi /2 \cdot k/\omega_{u <} TD$ the step response flying around and the amplifier is unstable.
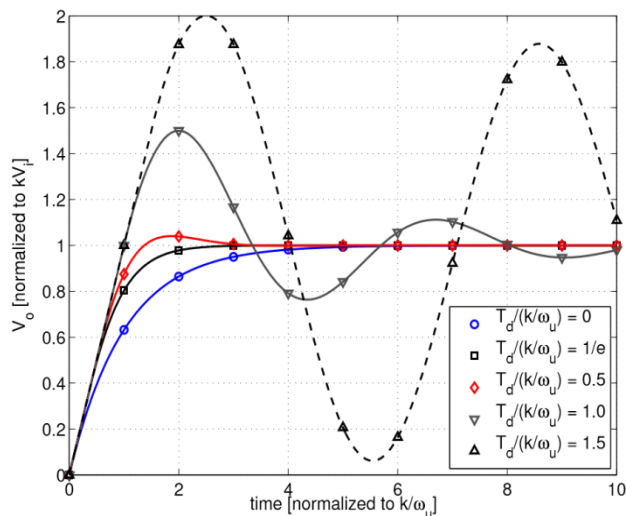

Figure 4: Transient response of the Fig. 3 (a) for different values of the delay with a step input *Vi and zero*

The above results confirm the intuitive conclusions from the previous section. Figure 4 shows the step responses for different values of the delay is less than the instability limit π /2 ·k/ω_u. Table I shows the delay time *TD* normalized to the amplifier time constant k /ω_u for various values of the overrun. The delay that can be tolerated is limited by the amount of the permissible overrun

Table 1: Delay for a certain exception

% Overshoot	1	2	4	10	20
$TD/(k/\omega_u$)	0.445	0.465	0.5	0.585	0.695

9. Development of topics in the classroom

The discussion of negative feedback you can begin with the development of the negative feedback amplifier and the time domain analysis in sections III to VIII. The behavior of the system can be visualized intuitively in the time period before it is mathematically derived. Spectral analysis of the Fig. 3 (a) leads to connections between the unit and the time constant loop gain frequency and bandwidth of the closed loop system.

This is followed by an attempt to in the synthesis of the integrator with a voltage controlled power source and a condenser. Naturally, this leads to a single-stage operational amplifiers. The effect of finite output resistance a real current source leads to discussion of the limited dc-gain and the resulting steady-state error. Attempt to improve the DC-gain in terms of reduction of the steady-state error leads to more complex operational amplifier topologies, as manufactured in several stages and operational amplifiers.

Parasitic effects in the circuit such as the parasitic capacitance *cp* at the output of the resistor divider leads to discussion of the effects of parasitic Pole in the negative feedback amplifier. The transient response of the loop gain at ABB. 3 (A) is a ramp with a slope of $\omega_{u /k}$. With parasitic Pole $p_{2 , 3 ,...}$, *N* in the loop, the step response of the open-loop gain is a ramp with a delay$\sum_{m=2}^{N} 1/_{after the}$ transient p m die. The restriction to the delay *TD* (as a part of the k/ω_u)for the desired overshoot can be translated into a constraint on the location of the parasitic Pole in relation to $\omega_{u /k}$. These results can be connected, in comparison to conventional spectral analysis in the phase margin. Outstanding ideas of a stabilizing negative feedback loops and the resulting borders(last paragraph to Chapter VII) can be strengthened.

A useful and frequently used idea is the ideal operational amplifiers may be discussed soon after Fig. 3 (a) will be introduced. In the memoryless model of the feedback amplifier in Fig 1, the amplifier will shut down in the ideal operational amplifiers in the Limit $A \to\infty$. If the op amp is modeled as an integrator, it is by definition ideal for dc, because of the infinite dc gain of the integrator. It can also ideal for all frequencies by the limit $\omega_u \to \infty$.

10. Conclusions

Detection of the error between the desired and actual values and continuous adjustment of the latter to reduce the error leads to the integrator, the central element of a negative feedback amplifier. Time domain analysis of this system provides central results of the behavior of negative feedback system. Try naturally lead to the realization of the Integrator op amp topologies. The author has this concept successfully in [7] and is of the view that students' interest was better, because (a) synthetic development of the negative feedback amplifier and individual circuits, and (b) a general overview of the main results of Time domain analysis before the rigorous analysis of the same for specific cases in the frequency range

References

[1] Adel S. Sedra and Kenneth C. Smith, microelectronic circuits, 6th ed. , Oxford University Press 2009.
[2] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, analysis and design of analog integrated circuits, 5. Ed., Wiley 2009.
[3] Nagendra Krishnapura, "synthesis based on introduction to operational amplifiers and Phase Locked loops", Proc. *2012 IEEE ISCAS*, May 2012.
[4] Karl J. ASTROM export-import P. R. and Richard M. Stallman. Murray, "feedback systems: A Introduction for scientists and engineers", available:

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http://www.cds.caltech.edu/~Murray/amwiki/index.php / Main_Page

[5] Barrie Gilbert, "Op Amp myths" are available: http://pe2bz.philpem.me.uk/Parts-Active/IC-Analog/op/OpAmpMyths/c007-OpAmpMyths.htm

[6] Hal Smith, *an introduction to delay differential equations with applications in the Life Sciences*, 1. Ed., Springer 2010.

[7] Nagendra Krishnapura, "ee5390: Analog Integrated CircuitDesign",available:http://www.ee.iitm.ac.in/~nagendra/videolectures

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