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# An Optimal Reconfigurable Cross Bar Switch for PCB Applications

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**Abstract:** ***This paper presents the technique and method to develop a reconfigurable crossbar switch (RCS) architecture for network processors. The main purpose of this paper is to increase the performance and flexibility of crossbar and reduce the excess power consumption. The method we proposed to reduce the power consumption at the runtime of crossbar switch is to enable only those link connection of crossbar which are necessary for the circuit or switch to perform and the unnecessary connection link turn off or disable by sending signal. We implemented a parameterized register transfer level design of reconfigurable crossbar switch. In this paper we showed the result of 4×4 crossbar switch. The result includes the VHDL simulation of RCS on Xilinx ISE software tool.***

**Keywords:** Interconnection network, on-chip communication, Reconfiguration, Crossbar Switch.

## 1. Introduction

Before the end of nineties, network equipment generally used as a general-purpose processors. But the need of quality-of-service (QoS) and the high speed data transmission asked for a quick evaluation of network equipments. Thus, the Network processor (NP) was created. Network processor takes the place of general-purpose Processors and Application specific Integrated circuits in network equipments. This are used to improve the two important issues flexibility and performance. These two features of processors are essential to process the packets, and the network processor is a best option to get them.

As industries build multi-core architecture involving number of cores in the future, on-chip interconnection network becomes a number one candidate for solving the problem facing on current multiprocessor chip. However one of the major challenges currently faced by on-chip interconnection is the power consumption. NoC architecture classified by the links for packet data transmission and router for storing, arbitration and switching functions performed by input buffer, arbiters and the crossbar respectively power is consumed from both communicating

The motivation is to increase the above two features cited before. With the help of reconfigurable crossbar switch in a network processor it could be achieved. Hence, using network processor with a reconfigurable crossbar switch as interconnection structure, it is possible to increase the throughput and reduce the power consumption of the network processor and also reduce the latency in communication packet transfer. The main objective of this paper is to reconfigure crossbar switch, a reconfigure crossbar switch architecture used to connect different inputs and outputs in interconnection and communication networks, and to implement dynamically topologies in two reconfiguration level.

The reconfigurable crossbar switch was described in VHSIC Hardware Description Language and implemented in the Field Programmable Gate Array. The outputs show the behavior of the application which contains transfer of packets that perform a collective broadcast operation on the reconfigurable crossbar switch.

## 2. Previous Work

There are number of commercial network processor of many companies available at the market. Some of this companies and their respective network processor are IBM (NP4GS3), Motorola/C-port (C-5 family), Lucent/Agere (FPP/RSP/ASI), and Sitera/Vitesses (IQ2000), Chamelean (CS2000), EZChip (NP-1), Intel (IXPI1200) and many more. None of them gives reconfigurability except the CS2000 of Chamelean [6]. But it does not have reconfigure crossbar switch. Network processor architecture has blocks to execute The related works presents result of previously implemented crossbar switch on FPGA. Our proposed platform for implementing crossbar switch with reduced energy consumption, flexibility but it did not change the core architecture. The work proposed is based on signal handling but the reconfiguration is depended on the FPGA. The Flex bar work propos to modify schedules and network hardware level, but the crossbar architecture is similar to a traditional crossbar switch (TCS). This paper done not relate the FPGA and reconfigure switch as a feature of flex bar. The Figure. 1 shows architecture of FPGA- Reconfigurable Crossbar Switch. Figure.1 shows some connection nodes of the reconfigurable crossbar switch, which if closed compose a circuit. This circuit represents a topology in space. Differ from the traditional crossbar switch where it is possible to close only one node per line or per column regarding the implemented topology, the Reconfigurable Crossbar Switch permits that more than one node can be closed per line or column at the same time . The reconfigurable crossbar switch uses a  bits to implement the topology in the space. This

topology is used to create the connection as for the circuit. The reconfigurable bits set are capable of reconfiguring or implement a new topology in reconfigurable crossbar switch whenever it required.

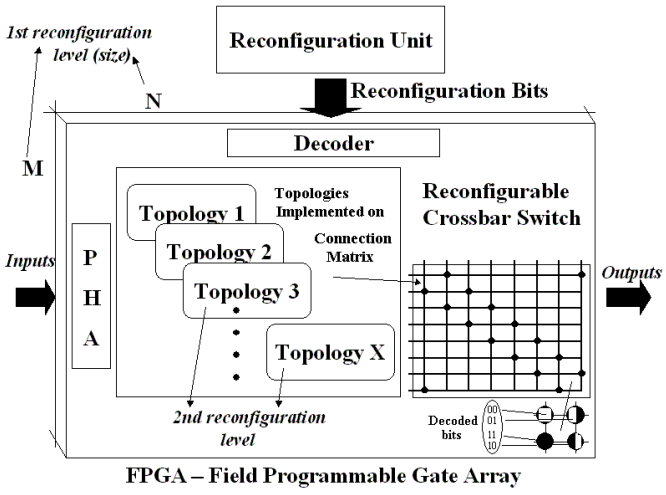


**Figure 1:** FPGA – Reconfigurable Crossbar Switch

Figure .2 shows the architecture of a bidirectional channel network-on-chip (BiNoC) router model. This part of network is used to enhance the performance of on-chip communication. In BiNoC, every communication channel allows itself to be dynamically reconfigured to transmit fits in one direction.

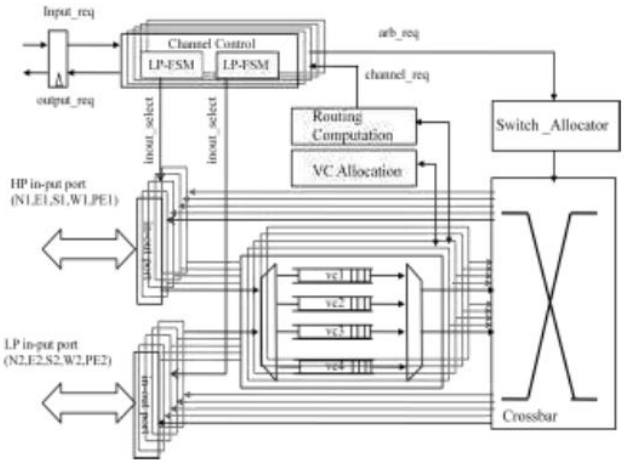


**Figure 2:** Modified four-stage pipelined router architecture for proposed BiNoc router with VC flow-control technique

This added flexibility, better bandwidth utilization, lower packet delivery latency and higher packet consumption rate. NoC router architecture is developed to support self configuration of the bidirectional traffic flow in the network processor. The flow direction at every channel-direction-control protocols (CDC). This channel-direction-control protocol provides high performance, free of deadlock and free of starvation. Figure.2 also illustrates reconfigurable crossbar switch components of a BiNoC router.

a) Crossbar Traversal

Flits that grant passage on the crossbar passed to the switch. The transversal time taken will be minimum as per requirement.

b) Switch Allocation

Individual flits arbitrate for access to all physical characters via the crossbar on each cycle. Arbitration may be performed in two different stages. The first stage reflects the sharing of a single crossbar port by V-input arbitrate between winning request from each input for each output channel. The request for a particular output port is routed from the VC which wins the second stage of arbitration. In order to improve fairness, the stage of the V-input the second stage of arbitration. We have to assume this organization wherever multiple stage of arbitration is presents.

c) Arbiter

Arbiter controls the arbitration of the ports and resolves connection problem. It keeps the update status of all the ports are free and which ports are communicating with each other. Figure.3 shows the arbiters used in the Reconfigurable Crossbar Switch.

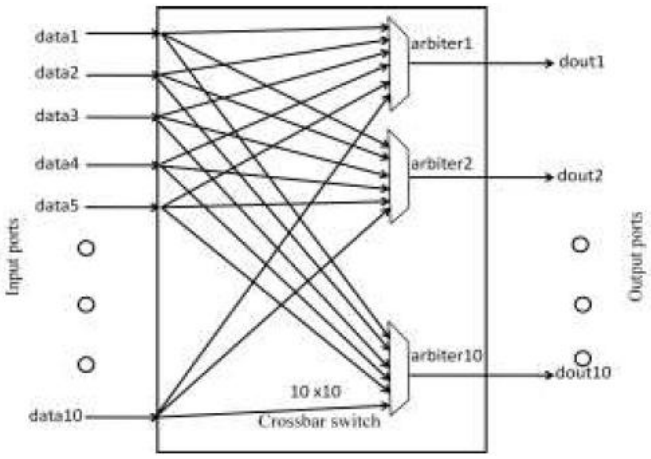


**Figure 3:** Arbiters in Crossbar Switch Model

Packets with the same priority and destined for the same output port are scheduled with round-robin arbiter.

**a) Crossbar**

A crossbar switch is a switch connecting multiple inputs to multiple outputs in a matrix manner. The design of crossbar switch has 4 inputs and 4 outputs. In architecture illustration in Figure.2 each input port is forced to share a single crossbar port even when multiple flits could be sent from different virtual-channel buffer. This restriction allows keeping crossbar size small and independent of the number of virtual-channel.

## 3. Reconfigurable Crossbar Switch Architecture

The Figure4 shows the Reconfigurable RISC Network processor (R2NP) architecture. R2NP is generally used as a base for developing or design of our reconfigurable crossbar switch architecture. Thus, design of our reconfigurable crossbar switch was based on the R2NP in network processor.

Reconfigurable crossbar switch shown in Figure 1, has mainly three blocks: (1) connection matrix, where all the topologies are implemented; (2) decoder, that converts the

reconfigurable bits for a matrix bits set and (3) pre-header analyzer. Network processor can add this third block in the packet with the output destination. Reconfigurable crossbar switch (RCS) uses reconfiguration bits to implement the topology in the space. Only the Reconfiguration Unit and instruction set of the network processor are able to change those bits in order to implements new topologies. Although one instruction can modify the 01 and 10 formats the 00 format is restricted to reconfiguration unit.

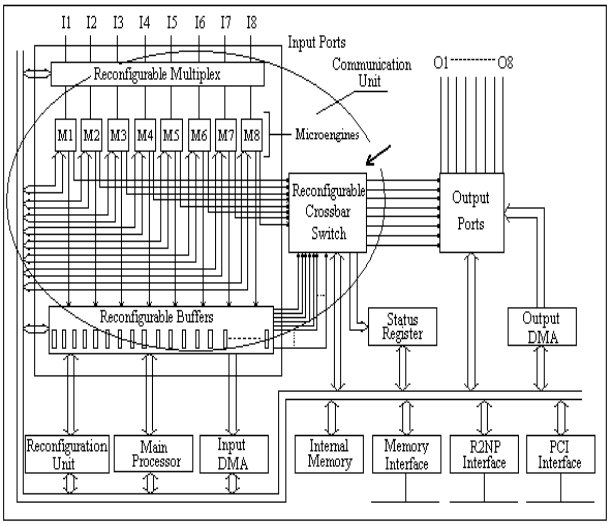


**Figure 4:** FPGA – R2NP Architecture

### 3.1 Proposed Work

This paper we proposed a method to develop reconfigurable crossbar switch architecture for network processor. In this paper we used 4×4 crossbar switch.

4×4 crossbar switch for 4 inputs and 4 outputs 16 connections are formed. If the 12 connections enable and other connections are disable although the power is consumed by all the connection in the switch. This power consumption is very big when the crossbar switch is used in very large scale. This becomes a disadvantage for crossbar switch. So in our proposed method we check whether the packet data comes from input is normal data or configured data. If the input packet is normal data then we allow it pass, but if the input packet is configured data then we stop the next packet and convert it into crossbar matrix.

### 3.2 Experimental Result

In our first result we have demonstrated the output of a normal packet from sources, 00, 01, 10 and 11 to 01,10,11,00 respectively. Our results show that the data goes properly from the given source towards the destination. The normal packets have MSBs as 0000.

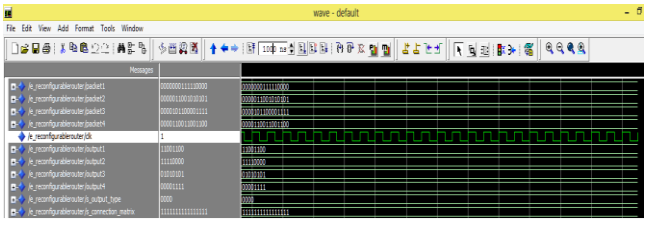

**Figure 5:** output of a normal packet from sources

In our next result, we demonstrate the reconfiguration; here we can observe that the connection matrix changes thereby the links which are turned off cannot communicate between each other.

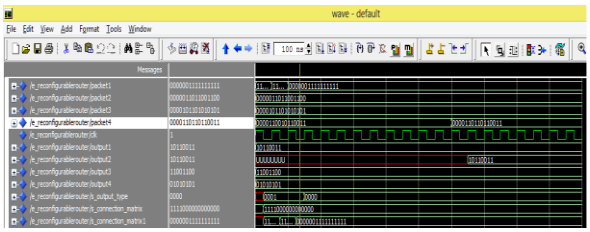

**Figure 6:** output of a optimized packet from sources

## 4. Conclusion

In our design we have optimized the power of a normal cross bar switch by disabling the unwanted data connections thereby optimizing the data activity on the data lines. This leads to an optimum crossbar structure for network on chip device.

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