Implementing of 16-Bit Pyramidal Adder for Arithmetic Applications

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Abstract: *Adders plays vital role in DSP processing applications and FPGA based VLSI environment where power,delay,speed and area are important parameters,so we need to reduce all parameter values as possible as possible. In all arithmetic operations power, delay, speed and area all are important and depend on multiplier which in turn depends on adders.So if we modify the adders namely half adder and full adder we can reduce parameter values.By implementing nomal half adder and full adder we can reduce the delay.*

Keywords: multiplexer (MUX), half adder (HA), full adder (FA), field programmble gate aray (FPGA), digital signal processing (DSP)

1. Introduction

In arithmetic operations addition is the major operation to perform arithmetic operations like multiplication, subtracting, dividing, comparing and finding a square root.In multiplication operation , addition is the basic operation to find multiplication of two binary bits. Addition plays crucial rule in DSP processor applications, in FPGA based binary multipliers and in computer application In all applications power,dealy and area requirement all are depend on multipliers which in turn depends on adders.

In multiplication operation multiplication of two bits carried out by completely with adders, multiplication includes generation of partial products, adding of partial products, methods such as parallel computing of partial products and carry propagating, all these approches are implemented with combinational devices.

Binary half adder is hardware formed complex circuit with five logic elements, if we use such half adder in mullti-combinational adders it gives more complex circuit for example for 1024-bit DSP processor,and also speed is reduced due to serial connecting logic elements. For nxn bit multiplier, nxn AND gates and n (n-1) OR gates are required, in terms of adders n half adders and n(n-1) full adderes are required.

Improving the performance of digital adder is needed because execution of binary operation completely depends on adders, there are so many adders are implemented such that to meet the requirements of FPGA based VLSI environment and DSP Processor operations.

Ripple carry adder: It is simplest adder among all adders but slowest adder, it requires o(n) and delay of o(n),where n represent the operand size

Carry look ahead adder: It has good area o(nlogn) and good delay of o(logn),but suffers from irregular layout design

Carry select adder: It has area of o(n) and delay with $o(n^{1+2/l+1})$, and it is the best adder in terms of area and delay

Carry save adder: Requires area o(n) and delay of o(logn)

Carry select adder is ths fast adder as it reduces computation time for operation among all adders but suffers from fanout limitation.The sorting problem is defined as the rearrangement of N input values so that they are in ascending order, merge sort method uses divide and conquer algorithm and uses recursion to perform sorting.

2. Existing Work

Hardware complexity of multipliers can be geatly reduced by using so many hardware structures and in those one of the structure is pyramidal adder.
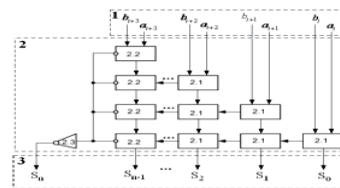

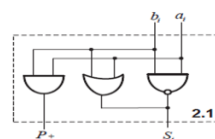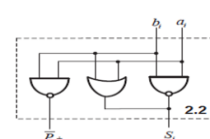Fig.(a):Structure of Pyramidal Adder with normal 2.1 and 2.2 blocks

Fig.(b):Half Adder   Fig.(c):Full Adder

Figure 1: Pyramidal adder with half adder and full adder

It contains single input 2n bit bus carrying inputs ($a_0b_0,\ a_1b_1$ $a_2b_2\ a_3b_3…..a_nb_n$), the pyramidal structures contains three single bit aders namely 2.1 block-to direct transfer of outputs, 2.3 block-to transfer inverse outputs,and 2.3block-to inverter the output bus of combinary adder (S_0 $S_0,S_1S_2S_3…..S_n$), here 2.1 and 2.2 blocks acts as half adders as compared to half adder with five logic gates ,so there is a reduction of gate count in the mulipliers with 2.1 and 2.2 blocks.if binary braun multiplier is implemented with pyramidal adder the gate count is reduceed and speed of operation also increased.

2.1Block

It uses NAND gate, AND gate and OR gate, its function is
$S_i=(a_i x b_i)x\ (a_i+b_i)= =a_i\ 'xb_i+a_ib_i'$
$P_+= a_i x b_i$

Where S_i is the sum and P_+ is the carry

2.2 block
It uses two NAND gates and one OR gate
It uses NAND gate, AND gate and OR gate, its function is
$S_i= (a_i x b_i)' x (a_i+b_i) = a_i 'x b_i+a_i b_i'$
$P_+= (a_i x b_i)'$

The P_+ is given to inverter to get final carry P_+

For standard 4x4 bit Braun multiplier using half adders and full adders consists there are 120 gates if multiplier is Implemented with pyramidal adder the gate count is 76 .but we can get reduced delay compared to standard multiplier then we will go for 16x16bit pyramidal adder.

3. Implementation of 16 Bit -Pyramidal Adder

This time for 16 bit pyramidal both gate count and delay is reduced compared to standard 16 bit adder which uses normal half adders and full adders.16 bit
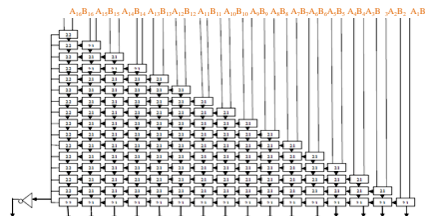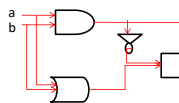

Fig.(a):16x16-bit Pyramidal adder
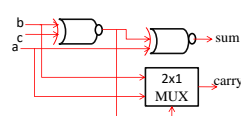

Fig.(b): Half Adder

Fig.(c): Full Adder

Figure 2: 16x16-bit Pyramidal adder with 2.1 and 2.2 blocks

16 bit pyramidal adder consists two 16 bit inputs a and b respectievely and they generate 16 sum output and 1 carry output, here 2.1 block and 2.2 blocks acts as half adders hence ech block generates one sum and one carry bit.

Let a and b be the inputs and sum and carry are the outputs
$Sum=((a\&b)')x(a+b)$
$=(a'+b')x(a+b)$.........using demorgans law
$=(axa')+(a'xb)+(bxb')+(axb')$
$=a'xb+axb'$
$=a \wedge b$
$Carry=(a\&b)$
$=axb$

Here this modified half adder acts as normal adder with less number of gates, so my using this modified half adder the gate count can be reduced.

Let a, b and c are the inputs and sum & carry are the outputs of modified full adder
$Sum=(bXNORc)XNORa$
$=(b'c'+bc)XNORa$
$=(b'c'+bc)a'+(b'c'+bc)a$
$=(b'c')(bc)'a'+ (b'c'+bc)a$
$=[(b')'+(c')']]b'+c']a'+(b'c'+bc)a$
$=[b+c][b'+c']a'+(b'c'+bc)a$

$=[bb'+bc'+b'c+cc']a'+(b'c'+bc)a$
$=[bc'+b'c]a'+(b'c'+bc)a$
$=a \wedge b \wedge c$
$Carry=[b'c'=bc]b+[b'c'+bc]'a$
$=[b'c'+bc]b+[b'c+bc']a$
$=bc+ab'c+abc'$
$=(a+a')bc+ab'c+abc'$
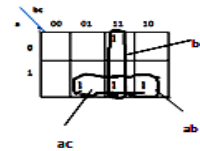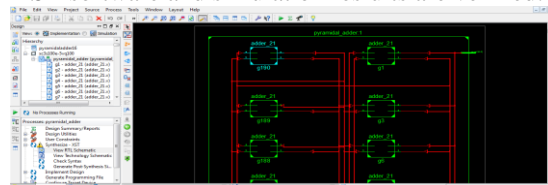

By using map
$Carry=ab+ac+bc$

Here modified full adder sum and carry values are same as normal full adder but topology isdifferent.The use XNORS mux delay is reduced, as the mux function is select to select output among inputs.

To generate s_0 no gate is required and to generate s_1 one half adder and one full adder required,partial products are given to adders to generate s_1 and two carries c_1 and c_2 respectievely.To generate s_3 one half adder and two full adders are used and generates carries c_3,c_4,and c_5 ,and as the partial product increases number of half adder and full adders also increases,here with modified half adder and full adder the outputs are obtained with minimum delay.

4. Simulation Results of 16-Bit Pyramidal Adder

16x16-bit pyramidal adder is designed and implemented xilinx ISE software and simulation res ults are verified.

Fig(a) RTL analysis of 16x16-bit Pyramidal Adder

Fig(b) Graphical representation of 16x16 -bit Pyramidal Adder

Figure 3: RTL and simulation results of 16x16-bit Pyramidal Adder

5. Conclusion

Binary multipliers are widely used in DSP processors and FPGA based VLSI domain environment, where area, power, speed and delay are important parameters. Power, area, speed and delay of multipliers can be controlled by implementing adders, there are so many adder structures are there for binary multipliers .pyramidal addrer is the one structure to reduce hard ware complexity and delay.In this thesis normal half adder and full adders are modified with

XNOR gates and MUX results minimum delay for 16 –bit pyramidal adders .

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