Implementing of 16-Bit Pyramidal Adder for Arithmetic Applications

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Abstract: Adders plays vital role in DSP processing applications and FPGA based VLSI environment where power, delay, speed and area are important parameters, so we need to reduce all parameter values as possible as possible. In all arithmetic operations power, delay, speed and area all are important and depend on multiplier which in turn depends on adders. So if we modify the adders namely half adder and full adder we can reduce parameter values. By implementing normal half adder and full adder we can reduce the delay.

Keywords: multiplexer (MUX), half adder (HA), full adder (FA), field programmable gate array (FPGA), digital signal processing (DSP)

1. Introduction

In arithmetic operations addition is the major operation to perform arithmetic operations like multiplication, subtracting, dividing, comparing and finding a square root. In multiplication operation, addition is the basic operation to find multiplication of two binary bits. Addition plays a crucial role in DSP processor applications, in FPGA based binary multipliers and in computer application. In all applications power, delay and area requirement all are depend on multipliers which in turn depends on adders.

In multiplication operation multiplication of two bits carried out by completely with adders, multiplication includes generation of partial products, adding partial products, and in computer application. All these approaches are implemented with combinational devices.

Binary half adder is hardware formed complex circuit with five logic elements, if we use such half adder in multi-combinational adders it gives more complex circuit for example for 1024-bit DSP processor, and also speed is reduced due to serial connecting logic elements. For nxn bit multiplier, nxn AND gates and n(n-1) OR gates are required, in terms of adders n half adders and n(n-1) full adders are required.

Improving the performance of digital adder is needed because execution of binary operation completely depends on adders, there are so many adders are implemented such that to meet the requirements of FPGA based VLSI environment and DSP processor operations.

Ripple carry adder: It is simplest adder among all adders but slowest adder, it requires o(n) and delay of o(n), where n represent the operand size.

Carry look ahead adder: It has good area o(nlogn) and good delay of o(logn), but suffers from irregular layout design.

Carry select adder: It has area of o(n) and delay with o(n^2 logn), and it is the best adder in terms of area and delay.

Carry save adder: Requires area o(n) and delay of o(logn)

Carry select adder is the fast adder as it reduces computation time for operation among all adders but suffers from fanout limitation. The sorting problem is defined as the rearrangement of N input values so that they are in ascending order, merge sort method uses divide and conquer algorithm and uses recursion to perform sorting.

2. Existing Work

Hardware complexity of multipliers can be greatly reduced by using so many hardware structures and in those one of the structure is pyramidal adder.

![Pyramidal Adder](image)

Figure 1: Pyramidal adder with half adder and full adder

It contains single input 2n bit bus carrying inputs (a_0b_0, a_1b_1 a_2b_2 a_3b_3.....a_nb_n), the pyramidal structures contains three single bit adders namely 2.1 block-to direct transfer of outputs, 2.3 block-to transfer inverse outputs, and 2.3 block-to inverter to output bus of combinatory adder (S_0 S_1 S_2 S_3.....S_n), here 2.1 and 2.2 blocks acts as half adders as compared to half adder with five logic gates, so there is a reduction of gate count in the multipliers with 2.1 and 2.2 blocks, if binary braun multiplier is implemented with pyramidal adder the gate count is reduced and speed of operation also increased.

2.1 Block

It uses NAND gate, AND gate and OR gate, its function is S_i=(a_i b_i)x (a_i+b_i)= a_i'. b_i'

P_i=a_i b_i

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Where \( S_i \) is the sum and \( P_e \) is the carry

2.2 block

It uses two NAND gates and one OR gate

It uses NAND gate, AND gate and OR gate, its function is

\[ S = (a \cdot b) \cdot (a + b) = a \cdot b + a \cdot b, \]

\[ P = (a \cdot b) \cdot (a + b) \]

The \( P \) is given to inverter to get final carry \( P_e \).

For standard 4x4 bit Braun multiplier using half adders and full adders consists there are 120 gates if multiplier is implemented with pyramidal adder the gate count is 76 but we can get reduced delay compared to standard multiplier then we will go for 16x16bit pyramidal adder.

3. Implementation of 16 Bit -Pyramidal Adder

This time for 16 bit pyramidal both gate count and delay is reduced compared to standard 16 bit adder which uses normal half adders and full adders. 16 bit

\[ S = (b'c+bc')a+bc \]

\[ P = (b'c+c')a' + (b'c'+bc)a \]

Carry = \[ (b'c)' + (c')' \] \( b'c' \)

\[ = (a+a')bc+ab'c+abc' \]

By using map

\[ \text{Carry} = ab+ac+bc \]

Here modified full adder sum and carry values are same as normal full adder but topology is different. The use XNORS mux delay is reduced, as the mux function is select to select output among inputs.

To generate \( s_i \) no gate is required and to generate \( c_i \) one half adder and one full adder required, partial products are given to adders to generate \( s_1 \) and two carries \( c_1 \) and \( c_2 \) respectively. To generate \( s_2 \) one half adder and two full adders are used and generates carries \( c_3, c_4, \) and \( c_5 \) and as the partial product increases number of half adder and full adders also increases, here with modified half adder and full adder the outputs are obtained with minimum delay.

4. Simulation Results of 16-Bit Pyramidal Adder

16x16-bit pyramidal adder is designed and implemented xilinx ISE software and simulation results are verified.

5. Conclusion

Binary multipliers are widely used in DSP processors and FPGA based VLSI domain environment, where area, power, speed and delay are important parameters. Power, area, speed and delay of multipliers can be controlled by implementing adders, there are so many adder structures are there for binary multipliers. Pyramidal adder is the one structure to reduce hard ware complexity and delay. In this thesis normal half adder and full adders are modified with
XNOR gates and MUX results minimum delay for 16 –bit pyramidal adders.

References


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Thokala Mohan Rao Received B-TECH degree from Vaagdevi Engineering College Warangal, obtained M-TECH with VLSI System Design from Anurag Engineering College, Kodhad. Currently working as Assistant Professor in Annamacharya Institute of Technology &Sciences, Hyderabad,Telangana state.Has published five papers in UGC journals. Areas of interest include Digital signal processing, low power Very large scale integration.