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# Modeling and Analysis of DC-DC Buck Converter for Mobile Applications

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**Abstract:** ***This paper presents the modeling of DC-DC buck converter system based on the mathematical model and analysis the dc-dc buck converter system for mobile device that powered by fixed battery DC supply. The aim of the modeling is the mathematical representation of a power electronic circuit for synchronous buck converter that controlled by fixed switching frequency in pulse width modulation. The state-space representation is used for modeling because of population, and it is essential to define the state variable of a circuit, state variable is the element storage of energy such as inductor and capacitor. This modeling included the parasitic resistances in mathematical representation of power circuit elements. In this work, it analyzed and studied the stability and the dynamic behavior response of buck converter output voltage model by using MATLAB/m.files simulation based on Bode plot frequency response and Root Locus method. This simulation illustrated the effectiveness performance of the buck converter when switching frequency changing, load resistance variation, and parasitic resistance changing for main inductor and capacitor through theoretical verification, graphical performance and MATLAB simulation.***

**Keywords:** Buck Converter Model; State-Space; Parasitic Resistance; MATLAB Simulation

## 1. Introduction

The diversities in functionality of smartphone applications need for numerous components; most of these components have different voltage levels and rising power demands for specific operation. At the same time, consumers want smaller phones with maximum battery life and minimal battery charge time. All of these requirements have driven development of various high performance and/or highly specialized power management integrated circuits (ICs) as in **Figure (1)**, MT6329 is a power management system chip, involves 15-buck converters and 21 LDOs, which are dedicated for specialist 2G/3G/smart phone subsystems, [1].


**Figure 1:** Power management integrated circuit.

And the power management IC PM7540 in **Figure (2)**, integrates all wireless smartphones power management, general housekeeping, and user interface support functions into a single mixed signal IC. Its versatile design is suitable for CDMA and non-CDMA smartphones, and other wireless products such as PC PDAs.

The power management portion accepts power from common sources-battery, external charger, adapter, USB_VBUS, coin cell backup and generates all the regulated voltages needed to power the appropriate smartphones electronics.

It monitors and controls the power sources, detecting which sources are applied, verifying that they are within acceptable operational limits, and coordinates battery and coin cell recharging while maintaining the smartphone electronics supply voltages. On-chip voltage regulators generate 24 programmable output voltages using a combination of switched-mode power supplies and low-dropout voltage regulators, all derived from a common trimmed voltage reference. One regulator is dedicated for generating microphone bias voltages. The features of PM7540 consists of, One boost (step-up) switched-mode power supply (SMPS) for driving white LEDs and hosting USB-OTG, Four buck (step-down), switched-mode power supplies for efficiently generating MSMC1, MSMC2, MSME, and PA supply voltages, Supports dynamic voltage scaling (DVS) for MSMC1, MSMC2, and PA outputs, 18 low-dropout regulator circuits with programmable output voltages, implemented using three different current ratings: 300 mA (four), 150 mA (ten), and 50 mA (four) [2].

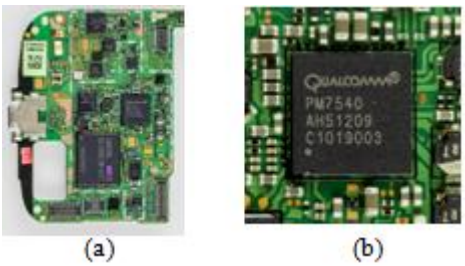



**Figure (2)**: (a) power management IC on smartphone PCB layout (b) PM7450

The substations of buck converter modules are dedicated and embedded in single chip power management IC as shown in **Figure (3)**, each buck converter module deliver the regulated and stabilized power for specific application such as CPU, Wi-Fi, Bluetooth, 3G, Display, …. etc.

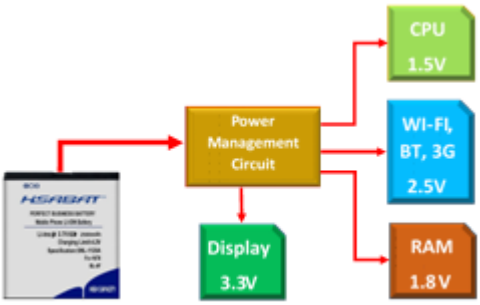



**Figure 3:** Typical block diagram of power distribution on a power management chip

## 2. Buck Converter Mathematical Model:

In general, the DC-DC Buck converter can be classified into the Step down or Chopper circuits. In actually the output voltage (Vo) of the buck converter is less than input voltage source (Vg), because the input voltage source (Vg) stepping down through the factor (Δ), [3].

Having a precise and complete model, which contain all of the system parameters (such as the active switch turn-on resistance, resistance of inductor and capacitor) is the main step in designing a non-conservative robust controller for Buck convertors. So that in this work we are considering all parasitic resistance of elements in order to obtain more accurate model, [4].

**Figure (4)** shows the buck converter power circuit that it consists of two active n-channel MOSFETs power switches (Q1) and (Q2), The schematic diagram indicates Q1 as a MOS switch and Q2 as a MOS synchronous rectifier, which replaces the diode rectifier in order to increase the circuit efficiency, main inductor (L), main capacitor (C), load resistance (R). As mentioned previously for obtaining nearly accurate model of buck converter, it considers the most parasitic resistance like inductor resistance ($r_L$), capacitor resistance ($r_C$) and switch resistance ($rs_{on}$) for both active switches (Q1, Q2). Further, input voltage source ($V_g$), output voltage ($V_o$), capacitor voltage ($V_C$), and inductor voltage ($V_L$). In the description of buck converter operation, it is assumed the converter operates in continuous conduction mode (CCM), in (CCM) the inductor current is continuous over one switching period, [5].

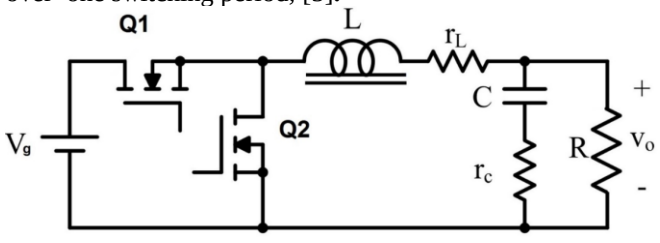



**Figure 4:** Power circuit diagram of Synchronous DC-DC buck converter

A state space description is a canonical form for writing the differential equations that describe a system, [6]. In modeling of the state space, the state variables, which are, represent the elements that store the energy of circuit (inductor current as magnetic field and capacitor voltage as electrical field), have significant importance, [7].

In switching regulator circuits, there are two states; the ON and OFF time state. The on time indicated by ΔT=T1, and the off time is indicated by (1-Δ)T=T2, in which T is the period of steady state output voltage ( T=T1 + T2 ), by Consideration $i_L$, $V_o$ as state variables ($\dot{X} = [i_L \quad V_o]$) that elaborate the states of linear circuits.

**a)** During On State in **Figure (5),** when Q1 is ON and Q2 is OFF, at a time period t<T1, and by applying Kirchhoff's voltage law, the circuit analysis can be described as follows:

$$V_g - i_L.rs_{on} - L\frac{di_L}{dt} - i_L.r_L - V_o = 0 \quad (1)$$

**b)** During OFF State in **Figure (6),** when Q1 is OFF and Q2 is ON, at a time period T1<t<T2 , and by applying Kirchhoff's voltage law the circuit analysis can be described as follows:

$$-i_L.rs_{on} - L\frac{di_L}{dt} - i_L.r_L - V_o = 0 \quad (2)$$

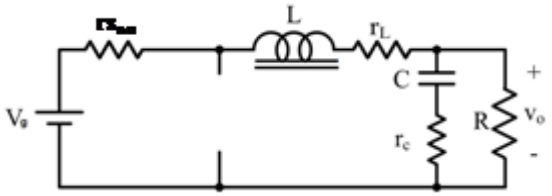



**Figure 5:** Power circuit diagram of Synchronous DC-DC buck converter during ON state.

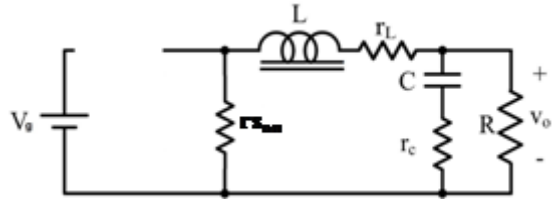



**Figure 6:** Power circuit diagram of Synchronous DC-DC buck converter during OFF state.

So Δ = [0 to 1] therefore the Eq. (1) written as follow:

$$\Delta V_g - i_L.rs_{on} - L\frac{di_L}{dt} - i_L.r_L - V_o = 0 \quad (3)$$

$$L\frac{di_L}{dt} = \Delta V_g - i_L.rs_{on} - i_L.r_L - V_o$$

$$\frac{diL}{dt} = \frac{\Delta V_g - Vo}{L} - iL\frac{(rs_{on}+r_L)}{L} \quad (4)$$

Let $x_1 = i_L$, then $\dot{X}_1 = \frac{di_L}{dt}$ , $x_2 = V_o$, then $\dot{X}_2 = \frac{dv_o}{dt}$

$$\dot{X}_1 = \frac{\Delta V_g - x_2}{L} - x_1\frac{(rs_{on}+r_L)}{L} \quad (5)$$

$$V_o = i_l.X_{load} \quad (6)$$

$$X_{load} = \frac{R\,X_c}{R+X_c} \text{ Where } X_c = \frac{1}{CS} + r_c = \frac{1+CSr_c}{CS} \quad (7)$$

$$X_{load} = \frac{R\frac{1+CSr_c}{CS}}{R+\frac{1+CSr_c}{CS}} \quad \text{then} \quad X_{load} = \frac{R+CS\,r_c\,R}{CS(R+r_c)+1}$$

Substituting $X_{load}$ in Eq. (6). Then

$$V_o = i_L\frac{R+CS\,r_c\,R}{CS(R+r_c)+1} \quad (8)$$

$$\frac{dV_o}{dt}C(R+r_c) + V_o = i_L R + \frac{di_L}{dt}C\,r_c R$$

$$\frac{dvo}{dt} = \frac{\frac{di_L}{dt}C\,r_c R + i_L R - V_o}{C(R+r_c)} \quad (9)$$

Substituting $\frac{di_L}{dt}$ in Eq. (4) with Eq. (9) then

$$\frac{dvo}{dt} = \frac{C\,r_c R\left[\frac{\Delta V_g - V_o}{L} - iL\frac{(rs_{on}+r_L)}{L}\right] + i_L R - V_o}{C(R+r_c)} \quad (10)$$

$$\dot{X}_2 = \frac{C\ r_C\ R}{C(R+r_C)}\left[\ \frac{\Delta V_g}{L} - \frac{x_2}{L} - x_1\frac{(rs_{on}+r_L)}{L}\ \right] + \frac{x_1\ R}{C(R+r_C)} - \frac{x_2}{C(R+r_C)}$$

$$\dot{X}_2 = \frac{LR-CR\ r_C(rs_{on}+rl)}{LC(R+r_C)}\ x_1 + \frac{-CR\ r_C-L}{LC(R+r_C)}\ x_2 + \frac{Rrc\ \Delta}{L(R+r_C)}\ V_g \quad (11)$$

$$\dot{X}_1 = -\frac{(rs_{on}+r_L)}{L}x_1 - \frac{1}{L}\ x_2 + \frac{\Delta}{L}\ V_g \quad (12)$$

$$\dot{X} = A.\ X + B.\ V_g,\ Y = C\ .X \quad (13)$$

$$A = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} = \begin{bmatrix} \frac{-(rs_{on}+rl)}{L} & -\frac{1}{L} \\ \frac{LR-CR\ r_C(rs_{on}+rl)}{LC(R+r_C)} & \frac{-CR\ r_C-L}{LC(R+r_C)} \end{bmatrix} \quad (14)$$

$$B = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} \frac{\Delta}{L} \\ \frac{Rrc\ \Delta}{L(R+r_C)} \end{bmatrix} V_g \quad (15)$$

$$V_o = \begin{bmatrix} 0 & 1 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix},\ C = \begin{bmatrix} 0 & 1 \end{bmatrix} \quad (16)$$

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \end{bmatrix} = \begin{bmatrix} \frac{-(rs_{on}+r_L)}{L} & -\frac{1}{L} \\ \frac{LR-CRrc(rs_{on}+r_L)}{LC(R+r_C)} & \frac{-CR\ r_C-L}{LC(R+r_C)} \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \frac{V_g}{L} \\ \frac{R\ r_C\ V_g}{L(R+r_C)} \end{bmatrix}\Delta \quad (17)$$

Now will make representation of the Eq. (17) in to S-domain:

$$\text{Lap.}\ (\dot{X}) = s\,X(s) = A.X(s) + B.V_g(s) \quad (18)$$

$$Y(s) = C.X(s) + D.V_g(s) \quad (19)$$

$$X(s)\ [Is - A] = B.V_g(s) \quad (20)$$

$$X(s) = [Is - A]^{-1}\ B.V_g(s) \quad (21)$$

Substituting Eq. (21) in Eq. (19) then

$$Y(s) = C\ [Is - A]^{-1}\ B.V_g(s) + D.V_g(s) \quad (22)$$

Where [I] is a unit matrix, and D = 0

$$\frac{Y(s)}{V_g(s)} = C\ [Is - A]^{-1}\ B \quad (23)$$

$$[Is - A] = \begin{bmatrix} s & 0 \\ 0 & s \end{bmatrix} - \begin{bmatrix} \frac{-(rs_{on}+r_L)}{L} & \frac{-1}{L} \\ \frac{LR-CR\ r_C(rs_{on}+r_L)}{LC(R+r_C)} & \frac{-CR\ r_C-L}{LC(R+r_C)} \end{bmatrix} = \begin{bmatrix} s + \frac{(rs_{on}+r_L)}{L} & \frac{1}{L} \\ -\frac{LR-CR\ r_C(rs_{on}+r_L)}{LC(R+r_C)} & s + \frac{CR\ r_C+L}{LC(R+r_C)} \end{bmatrix} \quad (24)$$

$$[Is - A]^{-1} = \frac{Adj[Is-A]}{|[Is-A]|} = \frac{\begin{bmatrix} s+\frac{CR\ r_C+L}{LC(R+r_C)} & -\frac{1}{L} \\ \frac{LR-CR\ r_C(rs_{on}+r_L)}{LC(R+r_C)} & s+\frac{(rs_{on}+r_L)}{L} \end{bmatrix}}{\left(s+\frac{(rs_{on}+r_L)}{L}\right)\left(s+\frac{CR\ r_C+L}{LC(R+r_C)}\right)+\left(\frac{LR-CR\ r_C(rs_{on}+r_L)}{L^2C(R+r_C)}\right)} \quad (25)$$

Substituting Eq. (15), Eq. (16) and Eq. (25) in Eq. (23), then the continuous-time transfer function model is written as follow:

$$\frac{Y(s)}{\Delta(s)} = Vg\ \frac{\frac{R\ r_C}{L(R+r_C)}s + \frac{R}{LC(R+r_C)}}{s^2 + \left(\frac{rs_{on}+r_L}{L} + \frac{L+CR\ r_C}{LC(R+r_C)}\right)s + \frac{R+rs_{on}+r_L}{LC(R+r_C)}} \quad (26)$$

From Eq. (26) evaluate the natural frequency ($\omega_n$) and damping ratio ($\zeta$) as follow:

$$\omega_n = \sqrt{\frac{R+rs_{on}+r_L}{LC(R+r_C)}} \quad (27)$$

$$\zeta = \frac{L+C\ r_L\ r_C+CR\ r_C+CR\ r_L+CR\ rs_{on}+C\ r_C\ rs_{on}}{2\omega_n\ LC(R+r_C)} \quad (28)$$

Then the time constant:

$$\tau = \frac{1}{\omega_n\ \zeta} \quad (29)$$

## 3. Stability and Dynamic Characteristics of Buck Converter Model

Since DC-DC buck converter appears between load and the main voltage supply, it needs to be stable and fast response along with dynamic characteristics behavior of the system, [8]. The stability analysis of DC-DC buck converter can be achieved using plotting bode plots. Hence, the stability of the system is defined in the terms of phase margin and gain margin where the Gain Margin is the difference between unity gain (zero dB) and the actual gain when the phase reaches 180°. The phase margin, however, determines the transient response of the output voltage in response to sudden changes in the load and the input. Phase Margin is equal to 180 degree plus the phase of Loop Gain. The system is said to be stable if its gain margin (GM) and phase margin (PM) are positive values otherwise unstable, [9]. The dynamic characteristics analysis can be achieved by finding the step response of the buck converter model and study the effect of the frequency, load resistance and parasitic resistance on the transient and steady state characteristics of the model (time constant, settling time, etc.). By depending on mathematical model in Eq. (26) of buck converter model, the stability and dynamic behavior of buck converter model can be studied. Therefore, three ready model specifications are adopted for the study as demonstrated in **Table 1** for 40Khz (**Model1**), **Table 2.** for 80Khz (**Model2**) and **Table 3.** for 120Khz (**Model3**), [10], [11].

**Table 1: Model1**, Electronics components values of the buck converter model at switching frequency 40 kHz [10], [11].

| Description | Symbol | Value | Unit |
|---|---|---|---|
| Inductance | L | 100 | µH |
| Capacitor | C | 150 | µF |
| Load Resistance | $R_{load}$ | 2.345 | Ω |
| Inductor Effective Series Resistance | $r_l$ | 0.19 | Ω |
| Capacitor Effective Series Resistance | $r_c$ | 25 | m Ω |
| MOS-on resistance | $rs_{on}$ | 2.1 | Ω |
| Supply voltage | V-supply | 3.75 | V |

**Table 2: Model2**, Electronics components values of the buck converter model at switching frequency 80 kHz [10], [11]

| Description | Symbol | Value | Unit |
|---|---|---|---|
| Inductance | L | 47 | µH |
| Capacitor | C | 68 | µF |
| Load Resistance | $R_{load}$ | 2.345 | Ω |
| Inductor Effective Series Resistance | $r_l$ | 0.13 | Ω |
| Capacitor Effective Series Resistance | $r_c$ | 55 | m Ω |
| MOS-on resistance | $rs_{on}$ | 2.1 | Ω |
| Supply voltage | V-supply | 3.75 | V |

**Table 3: Model3**, Electronics components values of the buck converter model at switching frequency 120 kHz [10], [11].

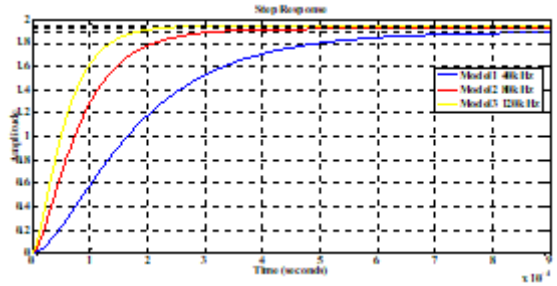
| Description | Symbol | Value | Unit |
|---|---|---|---|
| Inductance | L | 33 | µH |
| Capacitor | C | 47 | µF |
| Load Resistance | $R_{load}$ | 2.345 | Ω |
| Inductor Effective Series Resistance | $r_l$ | 0.066 | Ω |

| | | | |
|---|---|---|---|
| Capacitor effective Series Resistance | $r_c$ | 70 | m Ω |
| MOS-on resistance | $rs_{on}$ | 2.1 | Ω |
| Supply voltage | V-supply | 3.75 | V |

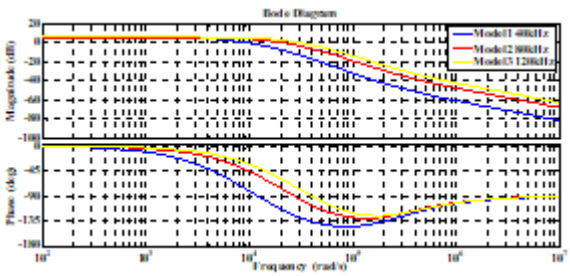
### 3.1 Effect of Switching Frequency on Buck Converter Model Response

In this section the effect of switching frequency will be studied on the open-loop response of the Buck Converter Model. **Figure (7-a)**, shows the dynamical behavior of the buck converter models **Model1**, **Model2** and **Model3** output voltage for unit step change open-loop response. When increasing the switching frequency the models exhibit different responses in the transient and steady state regions. The transient response in **Model3** (bigger switching frequency) is showing faster response compared to **Model**2 and **Model1** and likewise **Model2** is showing faster transient response than **Model**1. Worth to mention, the system is showing a stable response in all three models but there is high steady state error (voltage difference with the set-point).

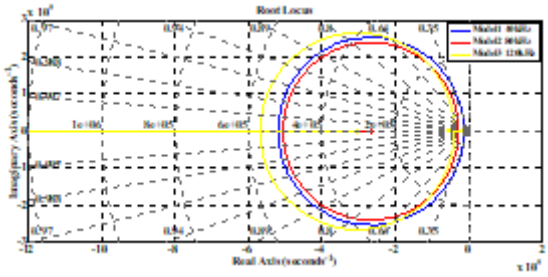
**Figure (7-b)** shows the Bode plot frequency responses of three models (open-loop transfer function) in the MATLAB control system toolbox. The frequency response of buck converter model at different frequencies is used for verifying the stability of the system. The Bode plot in the figure shows that the three models are showing stable behaviors because the loop gain, crossover frequency and phase margin are positive values. On the other hand, **Figure (7-c)** shows the Root Locus responses of the three models, which determine how each system behaves as the gain of the input to the plant, is varied from zero to infinity. In three models the physical behaviors reveal that these systems are stable because in each model two poles are conflict then one go to zero and other one goes to infinity (no pole or zero will end up in the right hand side of the z-plane).




(a)




(b)



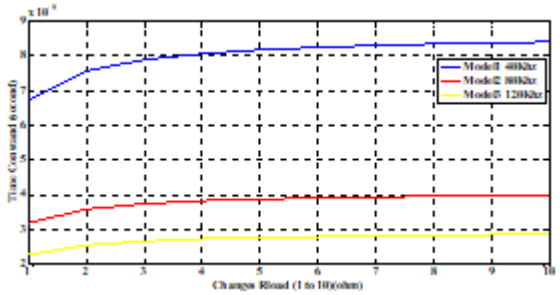

(c)

**Figure 7:** Open-loop response of buck converter model to switching frequency, (a) step change open-loop response; (b) Bode plot frequency response; (c) Root Locus response.

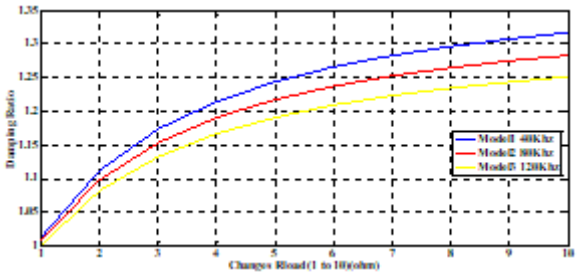
### 3.2 Effect of Load Resistance (R) on Buck Converter Model Response

This section will present the effect of load resistance changes on the response of the buck convert model. **Figure (8)** shows the effect of load resistance variation in terms of the time constant, damping factor and natural frequency on open-loop response of buck converter models, **Model1**, **Model2** and **Model3** assume the load resistance varies from 1Ω to 10Ω as load disturbance. As can be seen in the figure, the three models show similar pattern behaviors for the load resistance changes where they all increase the time constant of the system with the increase of the load resistance. Therefore, the system response becomes slower and also the steady state time increases. It is also observed that the effect of increasing the load resistance is relatively high for lower values (1 to 4 Ohm) compared to the increase afterward (4 to 10 Ohm).

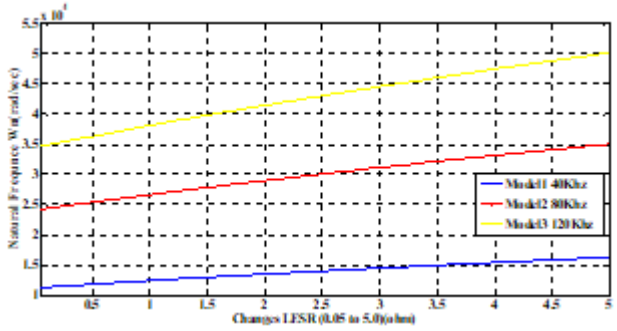
The damping factor of the system exhibit an increase with the increase of the load resistance but the natural frequency of the system decrease with the increase of the load resistance for the three Models as can be seen in **Figure (8-b)** and **Figure (8-c)**. These are also expected behaviors and they are in line with (Eq. 27 and 28).




(a)

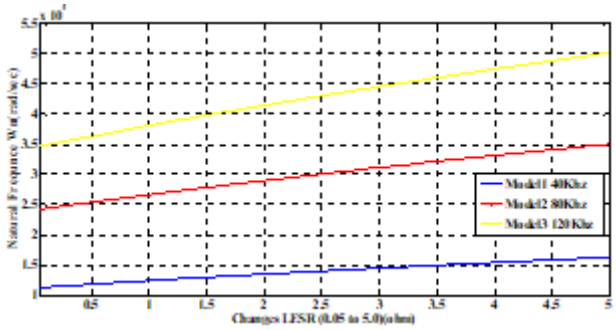



(b)




(c)

**Figure (8):** Effect of load resistance changes on (a) time constant (b) damping ratio (c) Natural frequency.

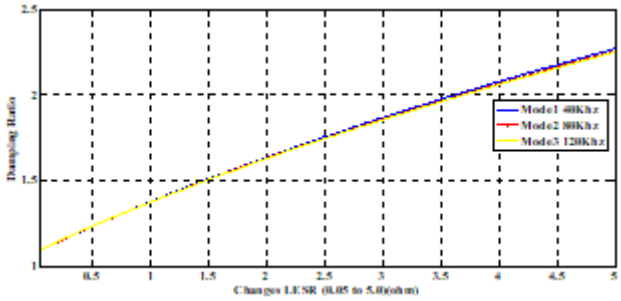



(c)

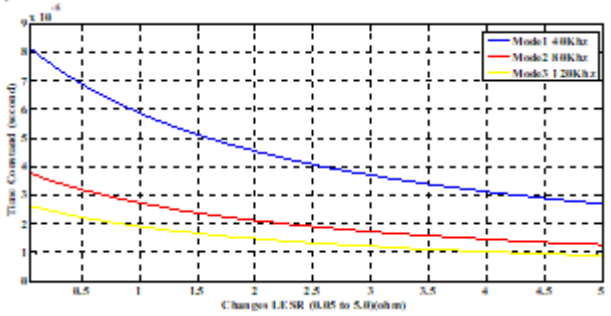
**Figure (9)**: effect of inductor resistance changes on (a) time constant (b) damping ratio (c) Natural frequency.

### 3.3 Effect of inductor resistance ($r_L$) on Buck Converter Model response

**Figure (9)** presents the effect of inductor resistance variation in term of the time constant, damming factor and the natural frequency on the open-loop response of buck converter models **Model1**, **Model2** and **Model3.** The inductor resistance is varied from 0.05Ω to 5Ω which in real life events could represent the variation due to the temperature, pressure or switching noise on the system. **Figure (9-a)** shows that the time constant of the system is decreased with the increase of the inductor resistance for all the three models. The decrease in **Model1**, however, is more prominent (more than 50%) than **Model2** and **Model3**. Moreover, the decrease is nonlinear as the rate of change is higher for low values (<2 Ohm) and then decreased for higher values (>2 Ohm). The decrease in the time constant is expected as the inductor and inductor resistance is inversely proportional to the time constant of the system (see Eq. 29). In contrast to the time constant, the damping factor and natural frequency of the system exhibit an increase with the increase of the inductor resistance for the three Models as can be seen in **Figure (9-b)** and **Figure (9-c)**. These are also expected behaviors and they are in line with (Eq. 27 and 28).




(a)



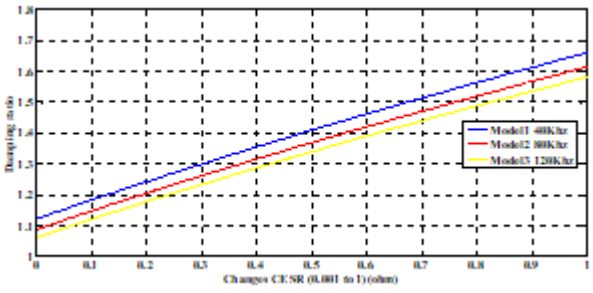

(b)

### 3.4 Effect of capacitor resistance ($r_C$) on Buck Converter Model response:

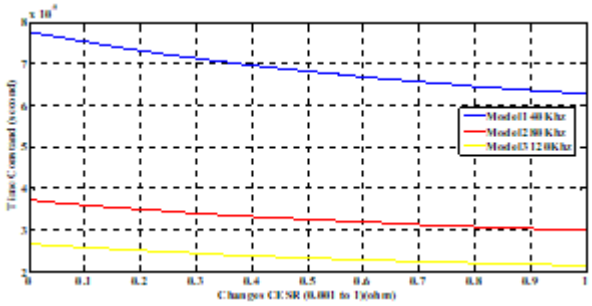
**Figure (10)** shows the effect of capacitor resistance variation in terms of the time constant, damping factor and natural frequency on the open-loop response of buck converter models **Model1**, **Model2** and **Model3.**

The capacitor resistance is varied from 0.001Ω to 1Ω. This variation can be attributed to the temperature, pressure or switching noise effect on the system. **Figure (10-a)** shows that the time constant of the system is decreased with the increase of the capacitor resistance for all the three models. The decrease in the time constant is expected as the capacitor and capacitor resistance is inversely proportional to the time constant of the system (see Eq. 29). In contrast to the time constant, the damping factor of the system exhibit an increase with the increase of the capacitor resistance for the three Models as can be seen in **Figure (10-b)**, and the natural frequency of the system exhibit an decrease with the increase of the capacitor resistance for the three Models as can be seen in and **Figure (10-c)**. These are also expected behaviors and they are in line with (Eq. 27 and 28).

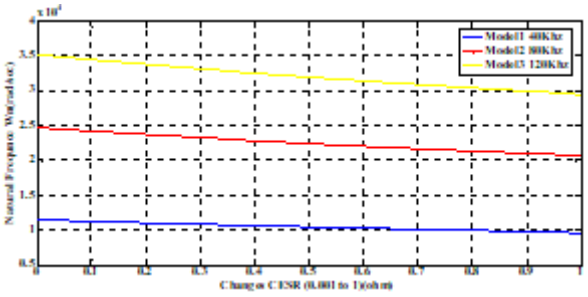
(a)




(a)




(b)




(c)

**Figure (10)**: effect of capacitor resistance changes on (a) time constant (b) damping ratio (c) Natural frequency.

The proposed study depends on **Model2** to its availability in trade markets. As previously mentioned in Eq. (27) and Eq. (28) for **Model2**, we can calculate the natural frequency $\omega_n$=2.44×$10^4$ rad/sec and the damping ratio ζ= 1.12 of the buck converter model, from substitute these calculated two values in Eq. (29), we can calculate the model time constant which is equal to τ=36.5μsec and the sampling time is equal to 3.6μsec by depending on Shannon's theorem.

The specifications of smartphone applications for NoKia N95 that are taken from [12], can be demonstrated in **Table 4**, to show the equivalent resistance of each application represent as variable load at in buck converter output model.

**Table 4:** The specifications of smartphone applications for NoKia N95 [12].

| Application | TTL low Voltage (V) | Full load (mA) And Consumption Power (mW) | Equivalent Resistance (Ω) |
|---|---|---|---|
| CPU | 1.5 | 408mA, 612mW | 3.67 |
| Wi-Fi | 2.5 | 580mA, 1450mW | 4.31 |
| Blue Tooth (BT) | 2.5 | 172.8mA, 432mW | 14.46 |
| Display | 3.3 | 77.01mA, 254.16mW | 42.84 |
| 3G | 2.5 | 560mA, 1400mW | 4.46 |
| Mobile TV | 2.5 | 316mA, 790mW | 7.91 |

## 4. Conclusion

This work presented the non-ideal modeling of DC-DC buck converter elements specification and illustrated the effectiveness performance the dynamic behavior response of output voltage model as well as it analyzed and studied the stability of buck converter output voltage model by using MATLAB simulation package that based on Bode plot frequency response and Root Locus method when switching frequency changing, load resistance variation, and parasitic resistance changing for main inductor and capacitor.

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