International Journal of Science and Research (IJSR)
ISSN: 2319-7064
SJIF (2019): 7.583

Renovated 32 Bit ALU Using Hybrid Techniques

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Abstract: ***In this modern world to increasing the demand for enhancing the ability of processors, is a challenging one. The most preferred module of a CPU is ALU which executes the mathematical and digital transactions. This multi-roled ALU circuit can conditionally perform various functions depending on control inputs. In this project, by using Efficient Vedic mathematics and refurbished approximate adder to form a 32 bit Efficient ALU. The major target of this works is to get Efficient ALU by reducing the area, power, and delay. So here used unique and earliest techniques of Vedic mathematics and which is also modified and to form Efficient Vedic multiplier. This efficient Vedic multiplier eliminates the unwanted steps and remaining procedures used by CSA. It reduces the hardware complexity of speed and area, it leads to decreasing the propagation delay in the chip. Approximate carry look-head adder contributes better delay and power reduction compared to other approximate adders. Delay, power, area of this proposed method of paper calculated by using Xilinx 14.7***

Keywords: ALU-Arithmetic And Logic, CSA-Carry Select Adder, Vedic mathematics-Urdhva tiryakbhyam sutra

1. Introduction

Aarithmetic Logical Unit(ALU) is the prime element of the Central Processing Unit and digital system design. A computer processor one of the vital parts is ALU. it's also a fundamental part of the Central Processing Unit which deals with arithmetic and logic operations. Nowadays ALU is getting miniature and more composite, because of logic gates. By using the Logic gate circuit design of the existing ALU chip implementation relatively slower because normal Logic gates want more power, delay, and area[2].

ALU allows the arithmetic operation of the computer like addition, subtraction, division, and multiplication and also perform normal logical operations such as AND, OR, XOR, XNOR, NAND, and inverter, etc. So the entire computer demands to do these functions, that is why ALU is known as the heart of the CPU. ALU also works in a combinational logic circuit when it has more than one inputs and only one output. ALU's output depends only on inputs which are applied at that instant and not on past conditions[3]. In basic ALU includes two inputs for the operand data, one input is used for choosing the specified operation, and one output is used for the result according to the selected operations [3].

In this work adder in logical operation is replaced by a fast energy-efficient refurbished approximate carry look-ahead adder. The existing structure of Carry Look-Ahead adder in larger bits has more area and power efficiency. This major drawback is overcome by a little bit of rearrangement to the traditional Carry look-ahead adder (CLA). Then it forms to refurbished Carry Look-Ahead Adder, and the proposed adder provides better in delay and in power reductions compared to other exact CLA.

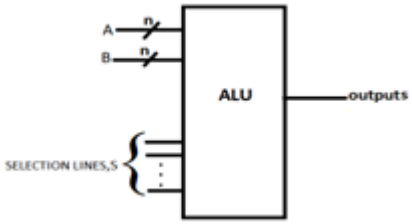

Figure 1: Basic ALU

The multiplier in the logical operation of this project was replaced by Vedic-multiplier based on Vedic mathematics. 16 sutras are included in Vedic-mathematics. In these, multiplication of any two numbers most commonly used Urdhva Tiryakbhyam(UT) and Nikhilam Navatashcaramam Dashatah (NND). This proposed project UT sutra. Urdhva tiryakbhyam sutra is a beneficial algorithm that can reduce the delay, power, and hardware requirements for the multiplication of numbers. So this Vedic based multiplier unit is faster than any other multiplier unit and also a reduction in power, delay, and area [1].

2. Design of Proposed ALU

Novel and Efficient 32-bit Arithmetic and Logic Unit using renovated Vedic mathematics and refurbished approximate adder contain Arithmetic and logic units. The arithmetic unit contains ADDITION, MULTIPLICATION, and SUBTRACTION. The logic unit contains AND GATE, OR GATE, NAND GATE, NOR GATE, XOR GATE, and XNOR GATE. The selection line will choose each operation in ALU

Table 1: ALU operations

Selection Line [S]	Operations
0000	RAP CLA ADDER
0001	SUBTRATOR
0010	VEDIC MULTIPLIER
0011	AND
0100	OR
0101	XOR
0110	NAND
0111	NOR
1000	XNOR

2.1. Refurbished Approximate Carry Look-Ahead Adder

This refurbished approximate carry look-ahead adder is based on the traditional carry look-ahead adder (CLA), it does not need any external correction unit. So these proposed adders delay and power consumption are considerably very less.

In the traditional CLA, the carry output of the *i*th stage is determined from equ.[1],

$$C\ i+1 = Gi + Gi-1Pi + \cdots + Go\prod_{j=1}^{i} Pj + Cin\prod_{j=0}^{i} Pj \quad [1]$$

Where *Cin* is the input carry and *Pi* and *Gi* are the propagate (*Ai^Bi*) and generate (*AiBi*) signals of the *i*th stage, respectively. In larger bits of CLA, the area usage, and power consumption of the carry generator units increase. So it will get a complex circuit. This problem overcome by this proposed method

So equation [1] rewritten as

$$Ci+1 = \sum_{m=0}^{i} Gm\left(\prod_{n=m+1}^{i-1} Pn\right) \quad [2]$$

2.2 Efficient Vedic Multiplier [1]

Vedic mathematics has its origin from ancient Indian scriptures "Vedas". Vedas itself means "knowledge" which can be used in algebraic mathematics and arithmetic mathematics. It reduces the complexity and delay of operation by pullout the unwanted steps during calculations.

Most commonly the multiplication of two numbers by using Urdhva Tiryakbhyam(UT) and Nikhilam Navatashcaramam Dashatah (NND). In the case of Urdhva Triyagbhyam Sutra, partial product generation is less and so it requires less hardware demand, hence increased speed and improved area so UT sutra is used in this project.

Urdhva Tiryakbhyam(UT) means "vertically and crosswise". So it is used for two numbers multiplication with any base. Let us consider the procedure for multiplying two 3-bit numbers A[2:0] and B[2:0] for example and C[3:0] indicate as carry, Y[2:0] indicate as the partial product output:-

step1: C0Y0=A0B0
step2: C1Y1={(A0B1)+(A1B0)}+C0
step3: C2Y2
={(A0B2)+(A1B1)+(A2B0)}+C1
step4: C3Y3={(A1B2)+(A2B1)}+C2
step5:C4Y4={(A2B2)}+C3
final product= C4Y4Y3Y2Y1

Normal Vedic multiplier[1] based on UT sutra is shown in fig.2

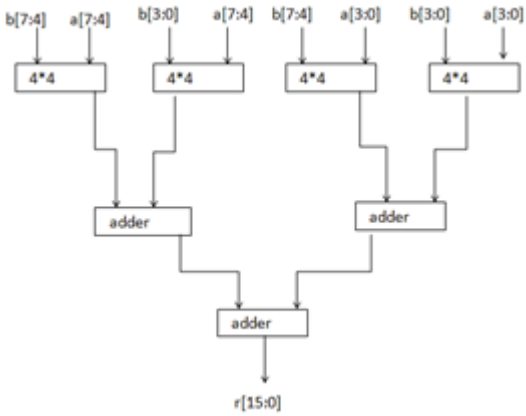

Figure 2: Normal Vedic Multiplier

Here 4, 4*4 Vedic multipliers are used for implementing an 8bit multiplier. Also, a 4-bit multiplier is implemented by a 2bit Vedic multiplier. Where 'A and B' are the inputs and 'r' are the outputs.

In this Efficient Vedic multiplier, instead of conventional adder replaced by the carry-save adder. So this will improve the delay & speed and reduce the hardware complexity. That modified version of the Vedic multiplier is shown fig.[3]

An efficient Vedic multiplier was designed by a 16-bit multiplier with a carry-save adder. In the design of a 32-bit Multiplier unit, designed by an efficient 16bit multiplier was used. It has been designed by efficient 8-bit multipliers. Similarly, an efficient 4bit-Multiplier was designed to operate for an efficient 2-bit Multiplier. An efficient Vedic multiplier design is shown in figure [3].

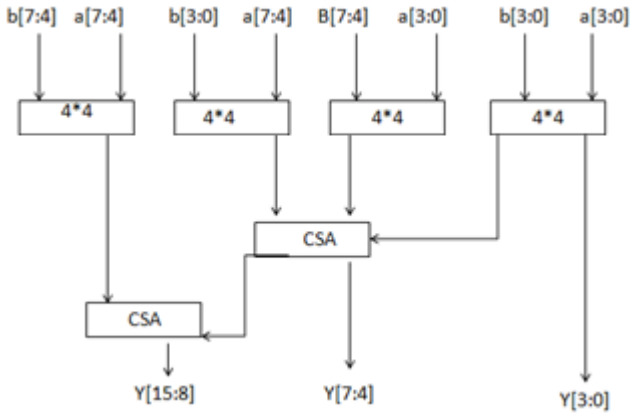

Figure 3: Renovated Vedic Multiplier

This fig.[3] Shows basic 8 bit of Efficient Vedic multiplier. Only conventional adders are used in normal Vedic multiplier, which is added to the output of each MUXs and finally gets resultant output. But here conventional adder replaced by Carry Save Adder [CSA]. 3 or more n-bit numbers can be used for computing the addition. It's done in two steps. When 3 inputs are given to CSA, the first step is the conversion into two outputs ie, sum and carry, and then the second step adds sum and carry vertically and then converting it into a single output. So it will provide better delay and reduction in power.

In this project, we implemented a 32-bit Efficient Vedic multiplier based on the redesigned 8-bit Vedic multiplier

shown in fig.[4]. Here 'a'&'b' are the inputs and 'y' is the output.

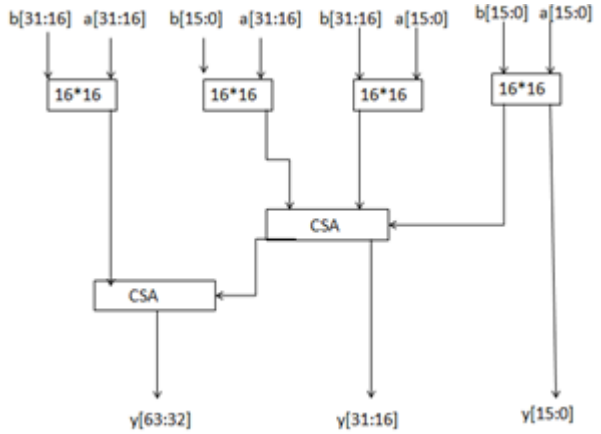

Figure 4: Renovated 32bit vedic multiplier

3. Simulation Results

In arithmetic circuits such as ADDER, SUBTRACTOR, MULTIPLIER, and logic functions such as AND, OR, XNOR, etc, .. in a single bit of ALU are separately verified at transistor and gate-level each of the modules is then integrated. We can determine its propagation delay and power consumption under the single-bit ALU circuit is simulated.

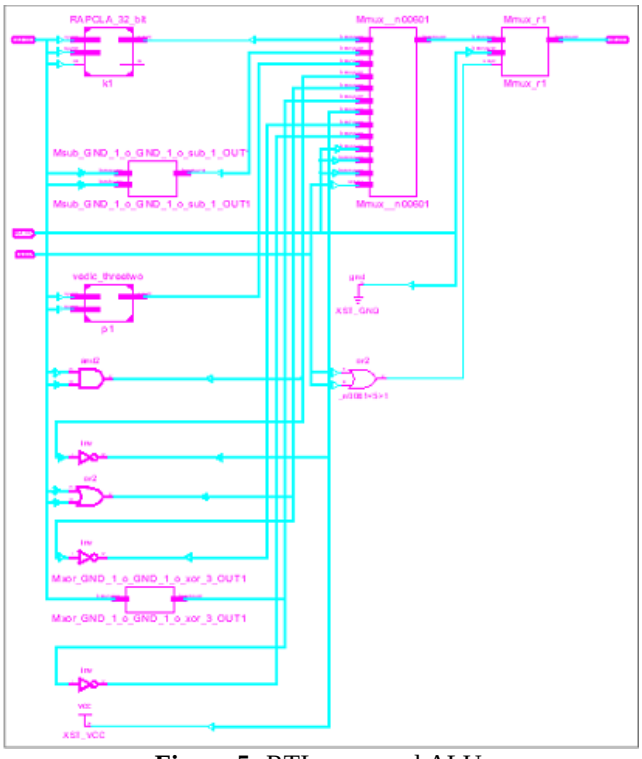

Figure 5: RTL proposed ALU

Verilog hardware modeling language is used for design and simulations of the circuits at the IC layout level up to 45nm process technology. Xilinx 14.7 is used here for the implication of the Verilog hardware modeling language.

The above fig.5.Shows the RTL of novel and efficient 32 bit ALU. RTL is Resister Transfer Level. Combinational logic is performed by transforming the data between the registers.

This proposed ALU design is consisting of 32-input-bits ie, 'A&B' and 5-bit selection line 'S' for selecting particular operations. If the selection line 'S=00000' then we get refurbished carry look-ahead adder output. It has 32-bit 'A' and 'B' inputs and 32-bit 'r' as the output shows in figure [6]

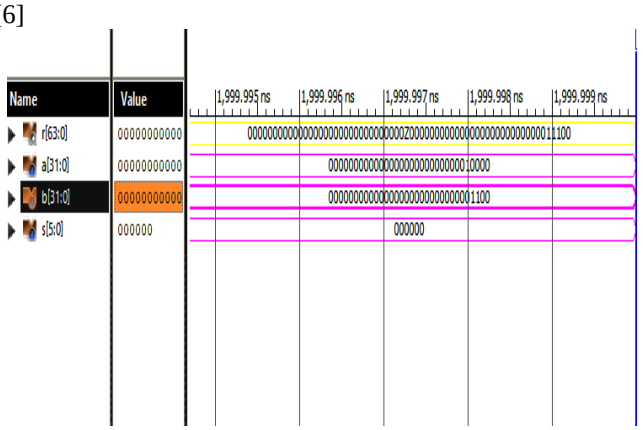

Figure 6: Output of adder

When selection line 'S=00001', then subtraction operation take place. Where 'A&B' are the 32-bit inputs and 'r' is the 32-bit outputs shows in figure[7]

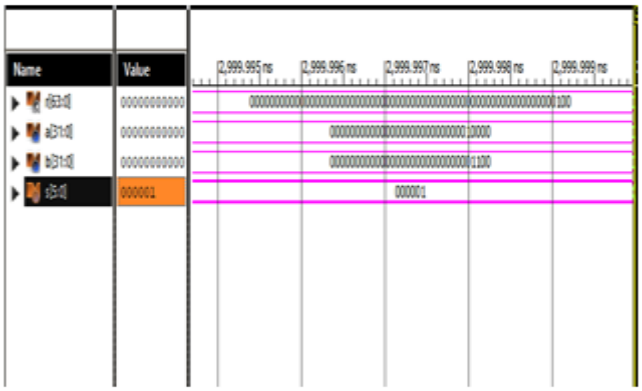

Figure 7: Output of subtraction

When the selection line 'S=00010', then multiplier operation takes place. Where 'A&B' is the 32-bit inputs and 'r' is the 64-bit outputs shown in figure[8]

Logic operations such as AND, OR, NOR, NAND, XNOR, and XOR are the same as the conventional operations.

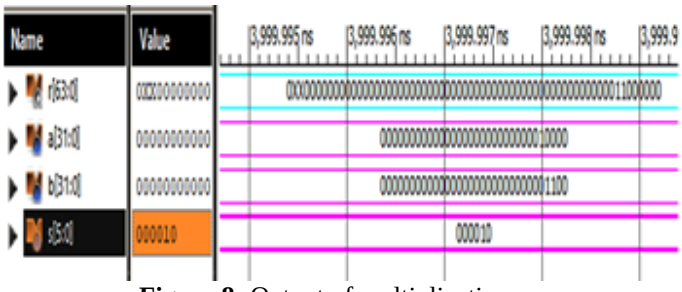

Figure 8: Output of multiplication

4. Comparision of Results

This proposed 32-bit ALU compare with other previous work to analyze that in table[2]

Table 2: Comparison with previous work

	Delay	Power
DREP ALU[6]	42.58ns	113mW
ALU chip with constraint of power consumption[1]	48.04ns	127mW
ALU chip using D3L logic And ancient mathematics[2]	120.6ns	54.48mW
Proposed ALU	34.32ns	45.61mW

This table [2] shows the delay and power is comparatively less with other previous work. Then the table [3] shows that bitwise ALU delay, power, and area. The result of the table [3] is delay and the area increases with the number of bits. Then the power of 8 bits is lesser than 4 bits that shown in table [3]

Table 3: Bitwise comparison

No.of bits	Delay	Power	Area[Utilisation percentage
4 bits	4.099ns	10.96mW	20[6%]
8 bits	9.532ns	7.92mW	36[15%]
32 bits	34.311ns	45.61mW	134[63%]

5. Advantages and Applications

Arithmetic and Logic Unit (ALU) is a very essential sub-block in the central processing unit and digital system design. Area, delay, and power these factors determine the performance of any circuit. So these factors are very relevant in VLSI design processor. Advantages of novel and Efficient ALU using renovated Vedic mathematics and refurbished carry look ahead-adder can reduce delay and power. Also, reduce the number of hardware requirements and areas of the chip. So this efficient ALU is faster than any other ALU chip.

This proposed adder used in many applications like cell phones, calculators, computers, and so on. Then it applicable in the central processing unit (CPU), microprocessor, nano-technology, optical computing, quantum compute and signal processing in satellite GPS-based systems.

6. Conclusion & Future Scope

Minimize the area and power is the more crucial task in the research field of very large scale integration (VLSI). So proposed Novel 32 Bit ALU Using Efficient Vedic Multiplier & Refurbished Approximate Mode Carry Look-ahead Adder is the improved version of the conventional ALU. In the renovated Vedic multiplier, which is a modified version of the UT sutra. It includes CSA. This reduces the power, delay, and area. Then refurbished carry look-ahead adder is used which will reduce the area and delay. This simulated code of 32 bit ALU design is implemented in Verilog HDL using Xilinx 14.7 and observed better performance in delay, power, and area compared to other ALU.

In the future, this proposed ALU extended to larger bits and can be used in CPU and signal processing.

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