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Development of QA Cell for PDK Validation and Automation using Cadence Skill

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Abstract: ***Process Design Kit is a unified foundry specific data used to design an integrated circuit.it can be logically thought similar to molecular DNA for the semiconductor industry. With the help of this PDK, an VLSI engineer can jump-start to design a chip and work seamlessly through the entire Design flow i.e Schematic Entry to Tapeout. This PDK is provided by the foundry which is technology specific,but can be tailored by the company according to their design style and markets. The Designer can use this PDK to design,simulate and verify the design before handling them to foundry for chip production. More accurate the PDK , More the chances of first pass successful silicon which in turn decreases the loss for the company. Cells are made with respect to the Design rules for various possible cases that an Designer may come across and then the DRC is made to run on the cells which gives us a check whether the DRC rules are properly coded or not to cover all the possible scenarios. if any discrepancies are found then they are fixed and same procedure is repeated. In the another section of the project an attempt is made to reduce the time required for drawing the QA cells with the help of automation using Cadence SKILL Language which in turn makes the process of validation faster.***

Keywords: QA Cell; Skill Automation; PDK.

1. Introduction

The integrated circuit are the basic building blocks of modern electronics. Integrated circuits are the self contained circuits which contains the transistor,resistor and capacitor etched on tiny silicon chip. Complementary metal oxide semiconductor (CMOS)forms the basis of every integrated circuit. Due to its zero static power dissipation, high density, high noise margin and ease of fabrication, it is widely used in semiconductor industry to develop random access memory (RAM) chips, digital signal processor (DSP)and application-specific integrated circuits (ASIC) chips.

A Process design kit is a unified set of data provided by the foundry, in a single environment, everything that is necessary to design and verify a cell/micro-cell/circuitry in a given CAD platform. PDKs can be considered as the logical equivalent of molecular DNA for the entire semiconductor industry. They are the basic building blocks of underlying integrated circuit design. They are the basic building blocks of underlying integrated circuit design. They include both physical and electrical models, constraints, rules, and all the things required by the EDA tools.

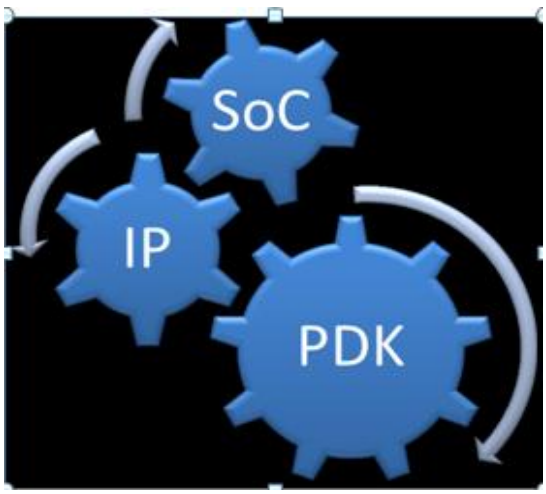

Figure 1: PDK Application

2. Formal Quality Assurance

After the product is being developed, next step consists of testing it which is QA. In this step the product is being tested as how the product will perform for different environment for various input conditions. Formal quality assurance is any systematic process used to check whether the product or service being developed is meeting specific requirement. A formal quality assurance system of the product increases the chance of first time success of the products which in turn increases the customer confidence and company's credibility. By improving work processes and efficiency, and enable a company to better compete with others. It emphasize on catching the defects before they get into the final chip/product. As far as PDK is concerned, FQA is drawing the design rules mentioned in the design rule manual in the layout viewer and verifying the functionality of devices in PDK library. Quality is ensured by developing the test cases for the rules which are mentioned in design rule manual of the specified technology for various possible cases. To minimize the risk and release higher quality PDK, FQA team create QA cell for each design rule mentioned in the DRM.

3. Methodology

DRC runset implementation is a task performed by the PDK (Process Design Kit) development team. DRC Deck coding for an advanced process is a long and complex task, and since the design rule descriptions are becoming complex day by day, implementation is based on the programmer subjective interpretation. Creating a correct and accurate check of a complex design rule is Highly impossible hence the probability of making errors is so high.[3] To minimize the risk and release higher quality run-sets, PDK teams create QA test cases for each design rule mentioned in DRM. These test cases are layout snippets that represents both violating (fail) and legal (pass) configurations.

A. Example of QA Cell

17-3: NPLUS Distance to N+ active other than NWELL strap -0.2

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Where 17-3 is the rule name drawn with the text layer NPLUS Distance to N+active other than NWELL strap is a rule description.

0.20 is the rule value

For particular DRC rule test cases are made accordingly. these test cases are drawn for various cases. Good and Bad test-cases are developed for all the possibilities of DRC rule in 2nd and 1st Quadrant respectively. Markers y5 and y8 are placed with their property changed according to the rule name .These markers are used by ARTE to identify the particular rule.

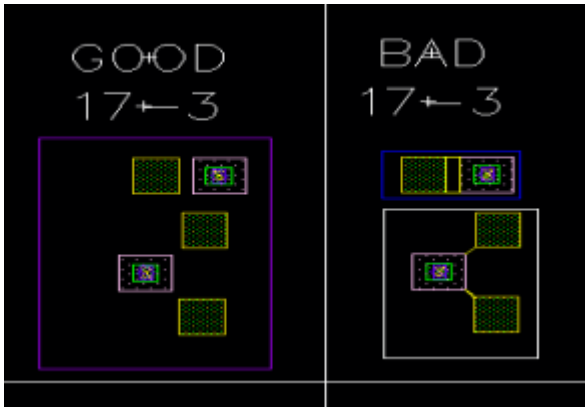

Figure 2: Sample QA Cell

Density Design Rule:
PO.DEN.1.1: Maximum physical PO density over local 150 µm x 150µm areas, stepping 75µm = 80 %
Calculation Total Chip Area = 150*150 = 22500µm2

1) PO;D, PO;Fill, PO;Filltr, PO;fillhv = 150*20*5 = 15000µm2
2) PO;mask, PO;nonprocessing = 150 * 10 *2 = 3000µm2
3) Total Area occupied by the Layers in 150*150 window = 18000µm2 satisfies according to rule
4) Area for Bad case 18000+0.25 (Area of any extra layer) = 18000.25µm2
5) Percentage = 18000.25/22500 = 80.00111% (Violation BAD Case)

B. Examples of Automation

As We all Know in the today's world of Semiconductor business, time to market is the important factor in deciding the success of product and growth of the company. Because of automation, productivity increases as man made errors are reduced. The time required will be less than half as compared to manual testing. This automation is done using Cadence proprietary language called as SKILL.
Area case
Rule name: NP.A.1

Rule Description NP area
Rule Value 0.129 (C)
SCRIPT
To make the QAcell for AREA
INPUT: value of area and width OUTPUT:Finding breadth

```
fqaMinArea( cv list("nplus" "drawing") 0.129 "NPLV.A.1")
fqaMinArea( cv "nplus" 0.129 "NPLV.A.1" ?Yref 10.0)
fqaMinArea( cv "nplus" 0.129 "NP.A.1" ?layerX "hvwell" ?Yref 15.0)
procedure(fqaMinArea(cv layer val rule @key layerX Yref)
;initial coordinates of good bad QAcell area
;rule for area of any layer
let( (xg yg xb yb x0 y0 x1 y1 qsp y5db y8b prp1 breadth
unless( YrefYref=0.0)
 ;initial coordinates
xg=-10.0 yg=Yref xb=5.0 yb=Yref
;unit space of Qacell
 qsp=5.0
 ;space for y5/y8 marker
 ysp=0.5
 dbCreateLabel(cv "text" 0.0:Yref rule
"centerCenter" "R0" "stick" 1.0)
breadth = round(val/(gr*qun))*gr ; To avoid offgridwhen( breadth ¡ val/qun
breadth = breadth + gr
;Add y5 and y8
when(layerX dbCreateRect(cv layerX list( xg:yg x0+breadth:y0+qun)))
y5db=dbCreateRect(cv list("y5" "drawing") list( xg-ysp:yg-ysp x0+breadth+ysp:y0+qun+ysp))
prp1=dbCreateProp(y5db "Rule Under Test" "string" rule)
when(layerX dbCreateRect(cv layerX list( xb:yb x1+breadth:y1+qun)))
y8db=dbCreateRect(cv list("y8" "drawing") list( xb-ysp:yb-ysp x1+breadth+ysp:y1+qun+ysp))
dbCopySingleProp(prp1 y8db) ;copy y5 property to y8
```

Figure 3: QA Cell for Area

4. Conclusion

As the node technology is decreasing day by day i.e. Beyond Moore's law,the DRC rules are becoming more complex.Rules in the DRM are increasing at the exponential rate. Hence good quality of PDK is essential for any Designer to ensure first time silicon success. At the same time ,In this cut throat competitive environment, time to market is the most essential thing for the growth of any company.PDK validation helps us to find errors before they can derail the chip and help to avoid huge loss for the company. before releasing the design kit it has to be fully validated with respect to DRC and LVS. Thus, QA Cell development is of high importance to the semiconductor industry.

References

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