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Simulation of Digital Current Sensorless Control for Dual-Boost Half-Bridge PFC Converter

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Abstract: ***To enhance the efficiency of the traditional enhance-kind power factor correction (PFC) converters with the diode bridge circuit, the PFC converters of bridgeless category are frequently used. Due to no series-related switches and no short-circuit dangers, the dual-boost half-bridge (DBHB) circuit is used because the PFC converter on this paper. This converter is able to working beneath variable PF. However, the focus of this paper is in reaching team spirit PF operation best. The efficiency of this circuit is excessive due to the fact there is simplest one series semiconductor on-state voltage drop at any on the spot. The presence of an imbalance within the voltages of the two DC-hyperlink capacitors, which changed into mentioned earlier than, is showed here. The purpose for the imbalance is analyzed the usage of suitable models, and a manage technique to take away it's far mentioned in element. In order to simplify the traditional -loop manipulate scheme and decrease the variety of sensors, the behaviours of DBHB PFC converter are studied and its equivalent unmarried-switch version is developed. Then, the current sensor less manipulate for DBHB PFC converter is proposed to achieve voltage law and yield sinusoidal enter contemporary in segment with the enter voltage without sensing any current. In addition, the proposed approach is capable of balance capacitor voltages certainly without including any voltage balancing control loop. An 800W DBHB PFC circuit is designed to assess the control performance and its simulation consequences are provided to illustrate the proposed present day sensor less control approach.***

1. Introduction

The extensive usage of dc power supplies inside most of electrical and electronic appliances lead to an increasing demand for power supplies that draw current with low harmonic content & also have power factor close to unity. Dc power supplies are extensively used inside most of appliances such as in computers, audio sets, televisions, and others. The presence of non-linear loads results in power system's low power factor operation. The basic block in most of power converters are uncontrolled diode bridge rectifiers with capacitive filter. Due to the non-linear nature of bridge rectifiers, non-sinusoidal current is drawn from the supply and harmonics are injected into the utility lines. The bridge rectifiers contribute to more THD, low PF, and low efficiency to the power system. These harmonic currents cause several problems such as voltage distortion, heating, noises etc. which reduces the efficiency of the power system. Therefore, there is a need for power supplies that draw current with low harmonic content & also have power factor close to unity.

The alternating mains utility supply ideally is supposed to be free from high voltage spikes and current harmonics. Discontinuous input current that exists on the AC mains as a result of non-linearity of the rectification process should be shaped to follow the sinusoidal form of the input voltage. Power factor correction techniques are of two types – passive and active. While, passive power factor correction techniques are the good choice for low power, cost sensitive applications, the active power factor correction techniques are used in majority of the applications due to their better performance.

1.1 Conventional Boost PFC Converter

The conventional input stage for single phase power supplies operates by converting the ac line voltage into dc and filtering with large electrolytic capacitors. By this process the input current waveform gets distored with large harmonic content. As a result, the power factor becomes very poor (around 0.6). The reduction of input current harmonics and operation at high power factor (close to unity) are important requirements for good power supplies. The conventional boost topology is the widely used topology for power factor correction applications. It consists of a front-end full-bridge rectifier followed by the boost converter. This diode bridge rectifier is used to rectify the AC input voltage to DC, which is then given to the boost section. This approach is good for a low to medium power applications. For higher power levels, the diode bridge becomes an important part of the application and it is necessary to deal with the problem of heat dissipation in surface area.

The continuous-conduction mode (CCM) conventional boost topology has been highly used as a PFC converter because of its simplicity and high power capability. Currently, in order to improve the efficiency of the front-end PFC rectifiers, many power supply manufacturers have started considering bridgeless power factor correction circuit topologies. Usually, the bridgeless PFC topologies which also known as dual boost PFC rectifiers, reduce the conduction loss by reducing the number of semiconductor components in the main line current path.

1.2 Cascaded Dual-Boost Converter

Recently, the cascade dual-boost converter had been widely used in some applications, such as the solar power conditioning systems and the intelligent universal transformer due to their high reliability and efficiency. From Fig. 1.1(d), each switch is connected with a diode which enables the cascade dual-boost converter to avoid the short-through problem without including dead-time settings. Moreover, no reverse recovery current flows through the body diode of each switch due to two diodes in the current flowing path. Therefore, the loss of reverse recovery current is obviously reduced. The distinguished features contribute

to the advantages of the high reliability and high efficiency for cascade dual-boost converter.

Many single-stage approaches have been suggested to get both power-factor correction and power conversion from the ac mains to a desired dc output. Since these topologies have a PFC cell integrated with a DC/DC conversion cell and both cells share an active switch and controller, the single-stage approach is a good choice from a cost point of view. Unfortunately, most of the proposed converters have some of the following drawbacks: large low-frequency output voltage ripple, low efficiency due to the switching and rectification loss, variable switching frequency and high-voltage stress on the switch.

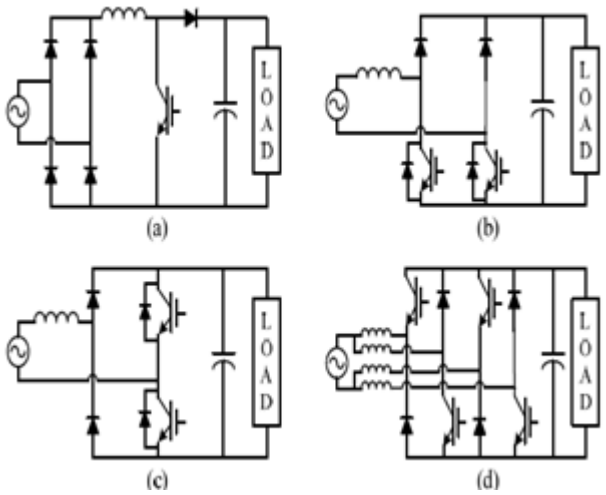

Figure 1: Boost-type converters: (a) conventional single-switch PFC converter (b) bridgeless PFC converter (c) bridgeless PFC converter (d) cascade dual-boost AC/DC converter

1.3 Half-Bridge PFC Converter

Compared with systems based on full bridge converters with a high frequency or commercial ac line frequency isolation transformer, the half-bridge topology offers several advantages including a simple power conversion circuit with possibly the lowest switching device count and no isolation transformer. Adding other desirable features such as sinusoidal ac line currents with unity power factor and load regulation with non-linear loads, the half bridge topology provides the potential for compact, low cost and high performance systems. Moreover, measurement of high frequency current is demanding, especially in cost-sensitive applications. The PFC converter proposed combines simple half-bridge topology and improved current sensorless-control algorithm that takes into account conduction losses. These losses influence volt-second balance in the input inductor and result in distorted grid current shape. The current sensorless control method proposed compensates this influence and allows achieving sinusoidal current shape.

1.4 Proposed Dual-Boost Half-Bridge Converter

The proposed PFC dual-boost half-bridge (DBHB) PFC converter with current sensorless control is shown below in Fig.2.

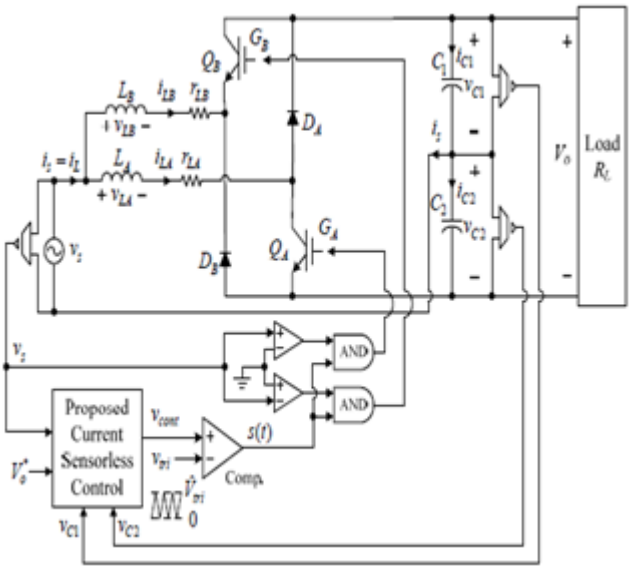

Figure 2: Dual-boost half-bridge (DBHB) PFC converter with current sensorless control

For PFC application, the conventional two-loop control with the inner current loop and the outer voltage loop can be used to control all the converters in Fig.2 where it needs to sense the DC-link voltage, the AC voltage and the inductor current. It is noted that the two-loop control can also be used in the half-bridge converters, but it needs to include third control loop to balance both capacitor voltages. Therefore, total four sensors (three voltage sensors and one current sensor) are needed to implement the half-bridge PFC converter. In digital PFC control, the current is conventionally feedback by the current sensor and Analog-to-Digital converter (ADC) with high resolution and high bandwidth. To reduce the cost, some control methods like current sensing methods using only comparators without real A/D converter were proposed. Furthermore, the control methods are proposed to rebuilt the current feedback signal from the sensed voltages. An adaptive inductor model and the adaptive nonlinear current observer were developed to estimate the current, individually. All the above methods can be classified into two-loop current sensorless control methods. The methods proposed can be seen as the single-loop current sensorless control methods where only voltage feedback loop is included and the switch duty ratio is synthesized from the controller output and the circuit parameters.

From literatures, no control method had been developed for half-bridge converter due to the requirement of voltage balancing loop. In this paper, the DBHB behaviors have been studied and its single-switch model is developed. Then, the first current sensorless control method for DBHB PFC converter has been proposed. Without including any voltage balancing loop, both capacitor voltages can be balanced naturally by the proposed method.

1.3 Modeling of Dual-Boost Half-Bridge Converter

From the Fig.2, the switch QA always turns off when the input voltage is in negative half-cycle Vs < 0. The switch QB always turns off in the positive half-cycle Vs > 0. All the switching states are tabulated below where the corresponding circuits are plotted below in Fig.3.

Summary of Switching States

Input Voltage	States	s(t)	Bridge A		Bridge B		C_1	C_2
			G_A	D_A	G_B	D_B		
$v_s > 0$	State 1	High	ON	OFF	OFF		$i_{C1} < 0$	$i_{C2} < 0$
	State 2	Low	OFF	ON			$i_{C1} > 0$	
$v_s < 0$	State 3	High	OFF		ON	OFF	$i_{C1} < 0$	$i_{C2} < 0$
	State 4	Low			OFF	ON		$i_{C2} > 0$

According to the control block diagram as shown in the Fig.2, the switching signal s(t) is generated from the comparison between the control signal Vcont and the triangle signal Vtri .

When the input voltage is positive Vs > 0, the gate signal GA is equal to the switching signal GA = s(t) and the other gate signal GB is off. Both capacitor currents are negative iC1 < 0 and iC2 < 0 (i.e. both capacitors C1 and C2 discharge) in state 1.

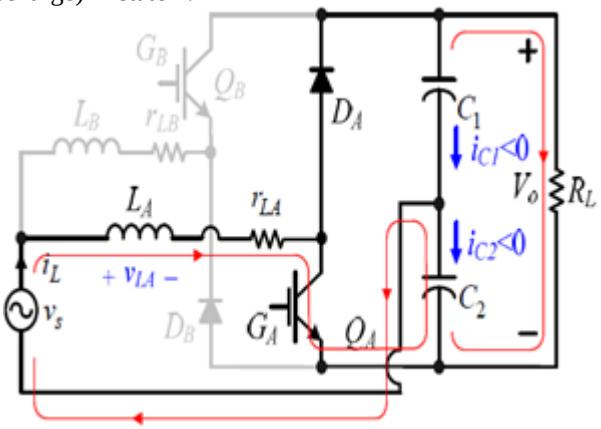

Figure 3 (a): Switching State 1 of dual-boost half-bridge PFC converter

In Fig.3(b), the switch QA turns off but the inductor current flows through the diode DA, and the capacitor current iC1turns to be positive. That is, the capacitor C1 becomes charged iC1 > 0, and the other capacitor C2 keeps discharged iC2 < 0 in state 2.

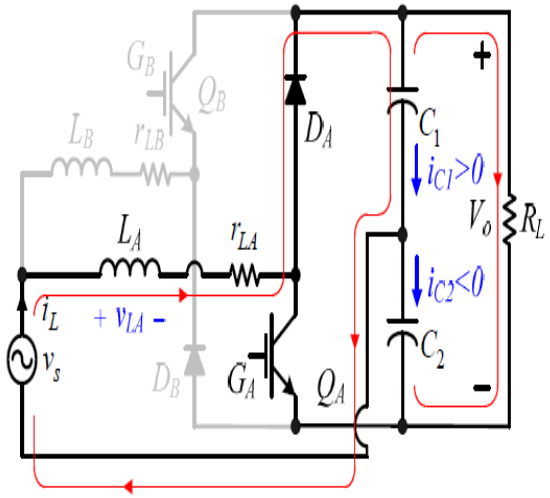

Figure 3 (b): Switching State 2 of dual-boost half-bridge PFC converter

In the negative half-cycle Vs < 0, the gate signal GB is equal to the switching signal GA = s(t) and the other gate signal GA is off. In state 3, both capacitor currents are negative iC1 < 0 and iC2 < 0 , and both capacitors C1 and C2 discharge as drawn in Fig. 3(c).

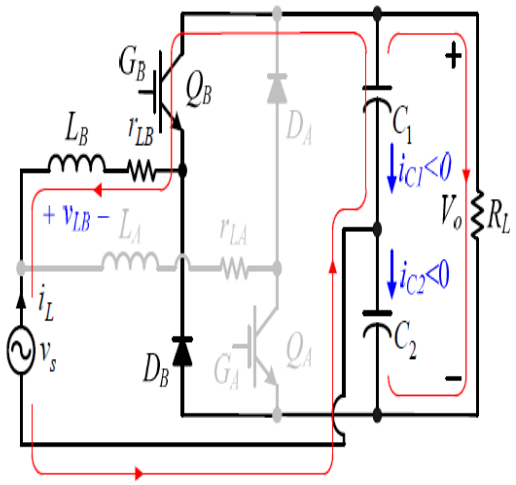

Figure 3 (c): Switching State 3 of dual-boost half-bridge PFC converter

Fig. 3(d) shows that the switch QB turns off but the inductor current flows through the diode DB. It follows that the capacitor current iC1 remains negative but the current iC2 becomes positive in state 4.

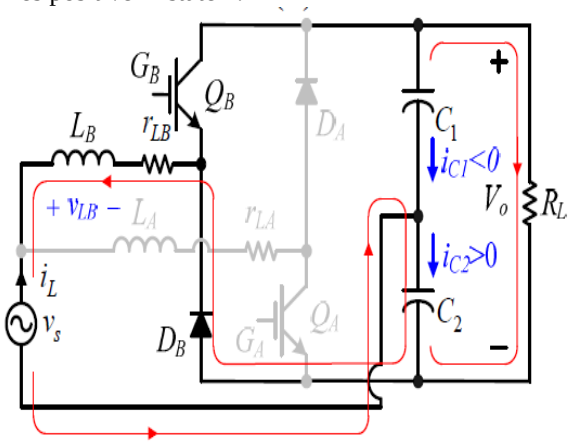

Figure 3 (d): Switching State 4 of dual-boost half-bridge PFC converter

1.4 Sensorless Current Control Method

Multiple current control techniques are known from the literature: peak current control, hysteresis, delta modulation, boundary switching, which relate to current measurement and all are relevant in some specific applications. On the other hand, input inductor current sensing in high frequency switched mode power supplies (SMPS) is the most challenging task, which will increases the cost and size of control system as it was mentioned in various articles, while the importance of the fast current loop has been discussed. The current sensorless control techniques are then proposed. They eliminate instantaneous current measurement, but use other approaches for estimation of input current. It is proposed to use a slower load current measurement to estimate current of input inductor. It is advised to use an average inductor current sensor that is suitable for digital

control systems. In the single-loop current sensorless control is being proposed, which is based on digital current rebuilding approach and uses input and output voltage values as well as predefined circuit parameters (inductor and capacitor precise values) to estimate instantaneous inductor current value. The fixed and variable switching frequencies are used in the above mentioned articles, however, according the constant frequency reduces switching losses in comparison with variable frequency control, as well as reduces high-frequency components.

In order to reduce the current sensor, the single-loop current sensorless control is proposed. The proposed current sensorless control is able to regulate the output voltage Vo and shape the input current is in phase with the input voltage Vs.

The proposed current sensorless control scheme is shown in the following Fig.4.

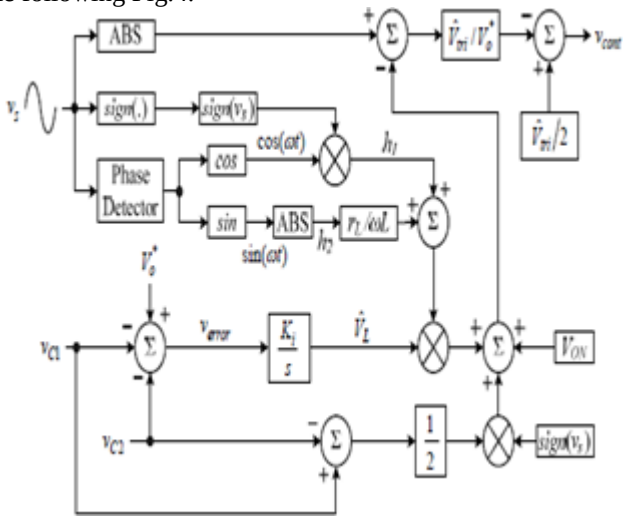

Figure 4: Proposed current sensorless control scheme

1.5 Natural Capacitor Voltage Balancing

From Fig.4, the amplitude of voltage signal VˆL is determined from the difference between the output voltage Vo and the voltage command *Vo through an integrator controller. the voltage error v_{error} in the imbalanced condition can be approximated as

$$v_{error} = Verror - a\cos(wt).$$

where Verror is the dc voltage error and the line-frequency component is dominant ripple.

When an extra resistor is connected to the capacitor C1, the capacitor voltages turn to be imbalanced. The feedback voltage error v_{error} is near to acos(wt) with a < 0 . Then, the ripple - (a /w)sin(wt) observed in the controller output VˆL would be in phase with the input voltage Vˆs sin(wt). Thus, the yielded current in positive half-cycle would be larger than that in negative half-cycle as shown in Fig. 5(a), which contributes to more charges stored in the capacitor C1 than C2 , and the balance between two capacitor voltages.

On the other hand, when an extra resistor is connected to the capacitor C2, the observed ripple in the controller output VˆL would be near -(a /w)sin(wt) where a > 0 . Thus, the yielded current in negative half-cycle is larger than that in positive half-cycle as shown in Fig 5(b), which brings more charges to capacitor C2 than C1, and balances the capacitor voltages.

Consequently, the proposed current sensorless control is able to balance the capacitor voltages without introducing the additional voltage balancing loop.

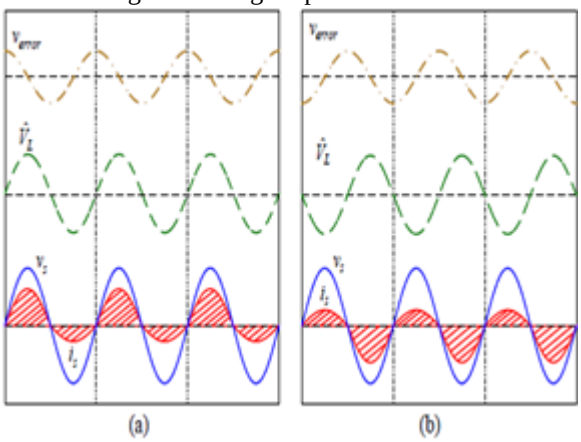

Figure 5: Illustration of natural capacitor voltage balancing: (a) transient response after an extra resistor is connected to *C*1; (b) transient response after an extra resistor is connected to *C*2.

To evaluate the natural voltage balancing performance, an extra 100Ω resistor is suddenly connected across the capacitor C1 and C2 , respectively, and then removed. Unlike the change of load resistor, the capacitor voltages have different changing direction, and thus the significant line-frequency ripple can be found in the output voltage Vo and the controller output VˆL until the connected resistor is removed.

When an additional resistor 100Ω is suddenly connected across capacitor C1 and then removed. The capacitor voltage vC1drops to 156V and the voltage vC2 rises to 244V within 0.3seconds. From the zoomed waveforms the controller output VˆL in positive half-cycle is higher than that in negative half-cycle due to its ripple.

The resulting current magnitude of input current is during positive half-cycle is higher than that during negative half-cycle, which brings more charges to the capacitor C1 than the capacitor C2 . Thus, the proposed current sensorless control is able to balance the capacitor voltage after the resistor is connected across capacitor C1 .

With consideration of the other condition, an extra 100Ω resistor is suddenly connected across the capacitor C2 and then removed. The capacitor voltage vC1 rises to 243V and vC2 drops to 157V. From the zoomed waveforms, the significant line-frequency ripple can be found in the output voltage Vo and the controller output VˆL . Fortunately, the controller output VˆL is higher during the negative half-cycle than that during the positive half-cycle. It follows that the magnitude of input current is during negative half-cycle is higher than that during the positive half-cycle. The larger current amplitude contributes to more charges stored to the capacitor C2 than C1. Eventually, both capacitor voltages vC1 and vC2 are balanced at 200V.

The proposed current sensorless control method is able to meet the PFC function not only in the steady-state condition, but also in the transient condition. At the same time, the voltage ripples in the output voltage Vo and the controller output V^L benefit the voltage balance. Thus, the proposed method is also to naturally balance the capacitor voltages without introducing any voltage balancing loop.

1.6 Current Sensorless DBHB PFC Converter Simulink Model

Here, the simulation results of the proposed current sensorless control for dual-boost half-bridge PFC converter are provided. The simulation parameters and some nominal values are listed in Table.

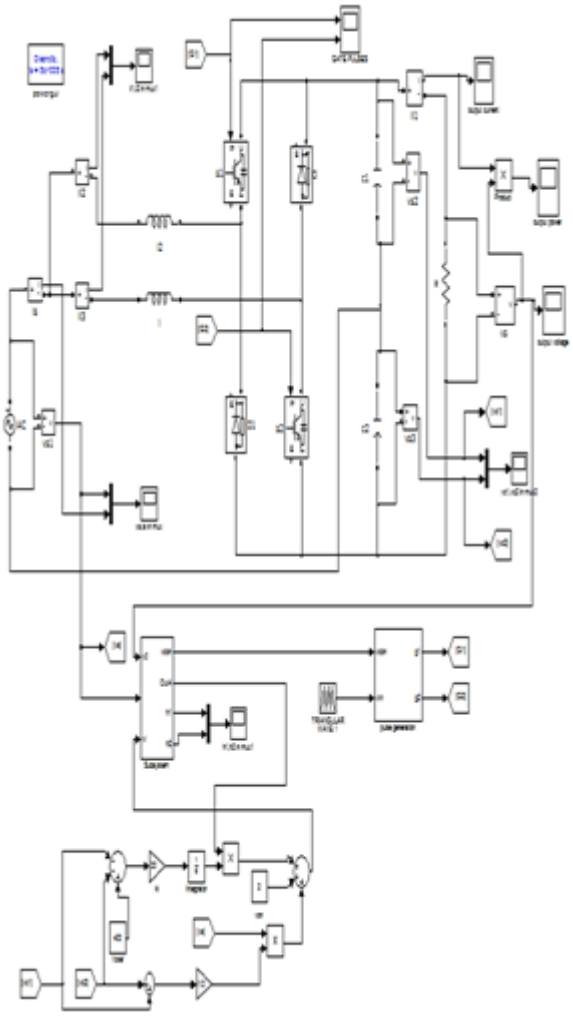

Figure 6: Simulink model of proposed DBHB PFC converter

Simulation Parameters

Specifications	*Values*
Input AC voltage (rms)	Vs = 110V
Output DC voltage	Vo = 400V
Line frequency	50Hz
Switching frequency	45KHz
Inductances	$L_A = L_B = 2.23$mH
Inductor resistances	$r_{LA} = r_{LB} = 0.4\Omega$
Capacitances	$C_1 = C_2 = 1170\ \mu$F
Conduction voltage	$V_{ON} = 2$V
Integrator gain	$K_i = 30$

The input current and voltage waveform corresponding to the above Simulink model is shown in Fig.6.2, Results shows that input current has harmonics which represent power factor will be low and it has to be corrected. The root-mean square value of input voltage is 110V and the line frequency f is 60Hz. The input current measured is 2A.

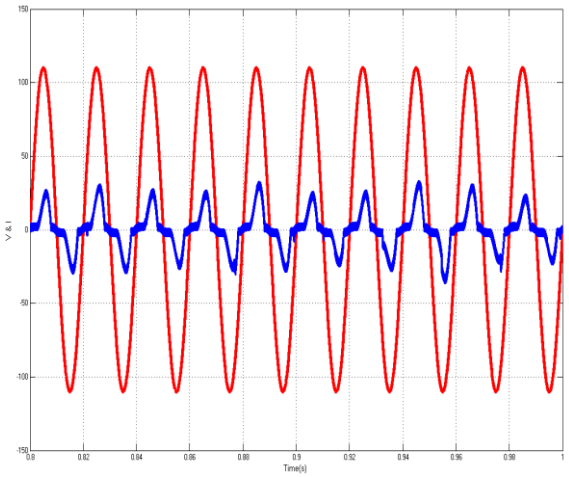

Figure 7: Input current and voltage waveform

The switching pulses for dual boost half bridge PFC converter is shown in Fig.8, consists of switching frequency 45 kHz given by flip flop after the sampling of control variable to obtain the steady state output. This gate signals are provided to the Switching devices Q_A and Q_B.

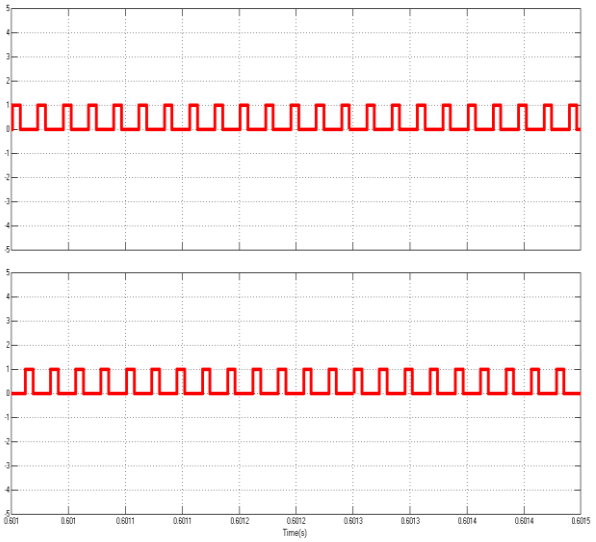

Figure 8: Switching Pulse waveform

The voltage across the DC link capacitor C1and C2 which are used for the filtering purpose are shown below. The measured voltage across the capacitor is 200V each since both the capacitor is naturally balancing in this circuit. Thus the capacitor voltages are VC1 = 200V & VC2 = 200V.

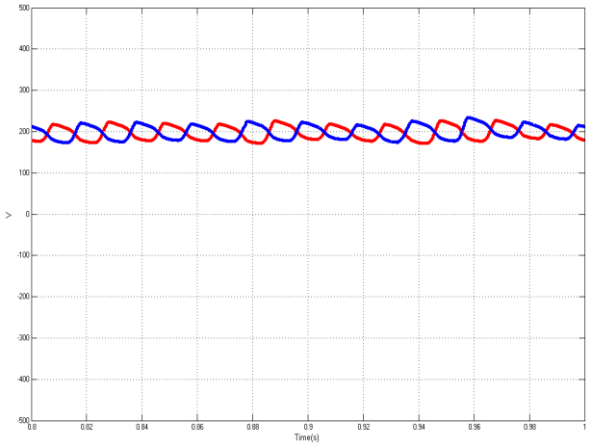

Figure 9: Voltage across the capacitors

The Steady state output voltage Vo waveform of the proposed dual-boost half-bridge PFC converter is shown below. The boosted output of the proposed system is measured as Vo = 400V.

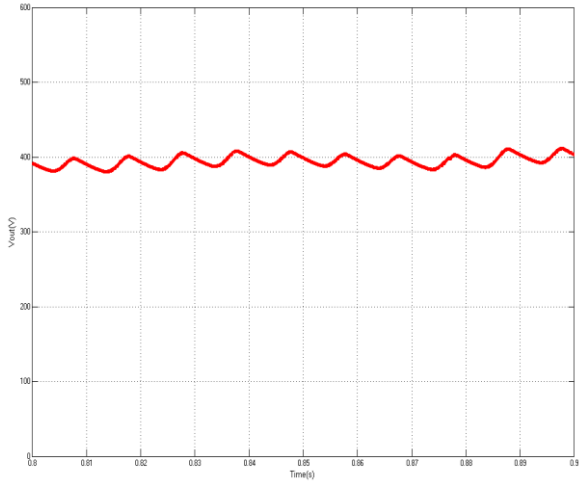

Figure 10: Output voltage waveform

The Steady state output current Io waveform of the proposed dual-boost half-bridge PFC converter is shown below. The output current of the proposed system is measured as Io = 2A.

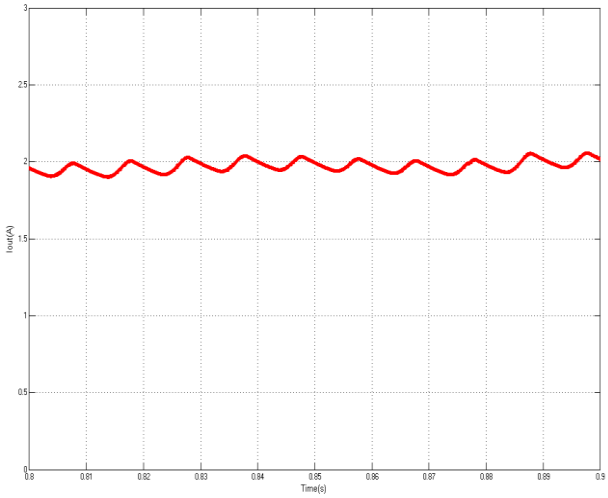

Figure 11: Output current waveform

The Steady state output power waveform of the proposed dual-boost half bridge PFC converter is shown below. The output power of the proposed system is measured as 800W. This power is measured for the load of 200Ω.

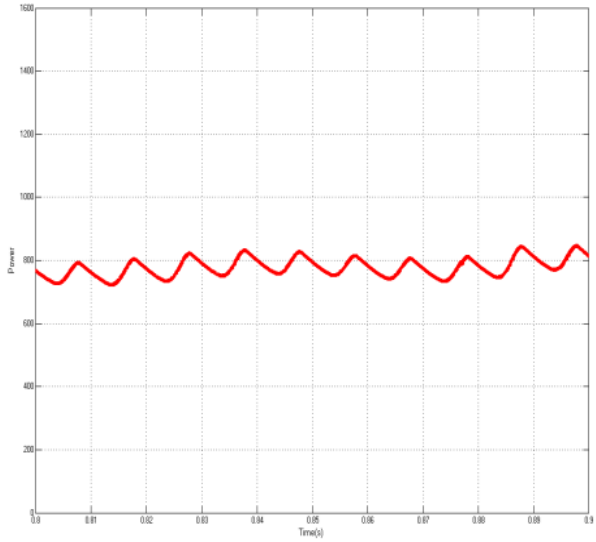

Figure 12: Output power waveform

2. Conclusion

The single-switch model for DBHB PFC converter has been developed. The current sensorless control method for DBHB PFC converter has been proposed and implemented in this paper. The integrator-type voltage controller is able to regulate the output voltage and balance the capacitor voltages. The proposed control strategy effectively achieves PFC function in steady-state condition and transient condition. Moreover, the capacitor voltages can be naturally balanced by the proposed control method.

From the simulation results, the proposed current sensorless control method is able to meet the PFC function not only in the steady-state condition, but also in the transient condition. At the same time, the voltage ripples in the output voltage *Vo* and the controller output *V˜L* benefit the voltage balance. Thus, the proposed control method is also to naturally balance the capacitor voltages without introducing any voltage balancing loop.

And also from the results of 800W proposed DBHB current sensorless control method, it is able to achieve PFC function even when the input voltage is distorted. Thus this control method can be used to the half-bridge PFC converter due to the same single-switch model. To evaluate the proposed current sensorless control, an 800W prototype converter is to be implemented in future.

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