

A Fast Calculation Method of QFP Packaging PIN Conductor Inductance

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Abstract: In this paper, a simplified method for calculating inductance of multiple microstrip lines (PIN conductors) is proposed. Taking the simplified calculation method of QFP packaging PIN conductors inductance as an example, with establishing the equivalent model and calculating their inductances by dividing the smallest units in parallel, and then it compared with the equivalent model inductance extracted by the professional electromagnetic simulation software HFSS, which proves that the simplified method is effective. By comparing the errors between the inductance calculated by the algorithm and the inductance of the equivalent model, the accuracy of the inductance parameters extracted by the method is verified from the engineering point of view. This method is easy to extract the inductance of PIN conductor encapsulated in QFP, and has great practical value.

Keywords: QFP Packaging; PIN; calculation

1. Introduction

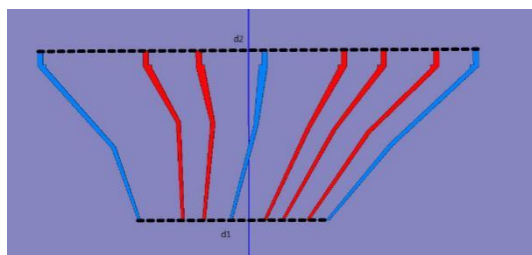


Figure 1: QFP Packaging Pin Model

QFP package is one of square pin flat package and surface mount package. The distance between pins of CPU chip in QFP package is very small and pins are very thin. Usually large scale or ultra large scale integrated circuits adopt this kind of package, and the number of pins is more than 100. As shown in the example in Figure 1 above, the PIN part represents the power supply with red conductor, and the blue conductor represents the ground. Generally, the metal is copper strip conductor. In general, in order to save location, the number of land is generally less than that of power supply.

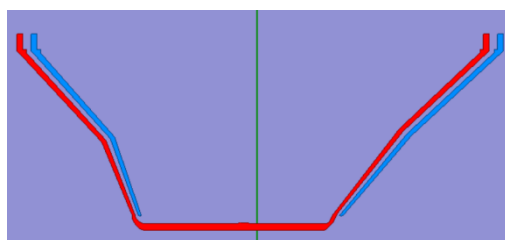


Figure 2: PowerBar Model in QFP Packaging Pin

In the actual QFP package, the Pin part may also have different forms. In order to save Pin's position, two pins are connected to replace many pins, that is, PowerBar structure. The specific model is shown in Figure 2. For this structure, the power bonding wires are typically on the power PowerBar, and the bonding wires of the ground property are typically on the Pin or on the power Bar.

2. Establishment of Equivalent Model

For the actual structure of Pin as shown in Figure 3, we simplify the model, because the Pin part is not regular, the front-end lead is a square with an edge length of about 0.08mm, and the back-end lead is a square with an edge length of about 0.16mm. In order to facilitate calculation, this paper will simplify it into a regular rectangular strip structure. The specific flow chart is as follows:

- 1) Firstly, the maximum length and the minimum length of the Pin part are determined, and then the equivalent length Len is chosen as the mean of the maximum length and the minimum length of the Pin in the given structure, as follows:

$$Len = \frac{l_{max} + l_{min}}{2}$$

- 2) Then determine the distribution length of the front end and the end of Pin part, and then homogenize according to the number of power sources. As shown in the figure 3, the distance d between two lines is equivalent to:

$$d = \frac{d1 + d2}{2(p_num + g_num - 1)}$$

- 3) Determine the average length and width of cross section and the height of PCB (replaced by PEC conductor). Draw the equivalent model as shown in Figure3 below.

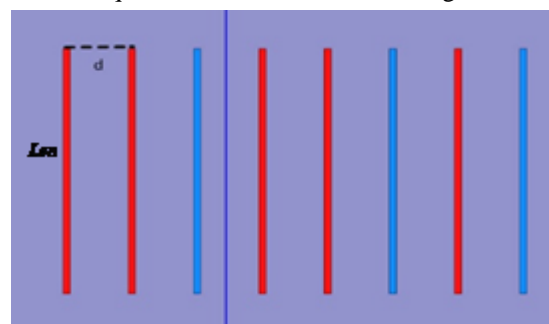


Figure 3: Pin Equivalent Model for QFP Packaging

The QFP encapsulated Pin equivalent circuit model, like its bonding line, can be equivalent by lumped model T-type network structure or type network structure, which is not described here.

3. A method of Calculating Pin Inductance Parameters

Fig. 4 (a) - (d) is the basic component of the smallest unit. It is the smallest unit 1p1g, 2p1g, 3p1g and pg_more (the remaining power lines except the smallest unit). Among them, the inductance formula is fitted by the minimum unit 1-3, and the inductance matrix of the minimum unit 4 can be formed by the fitting of self-inductance and mutual

inductance. Then the inductance of the minimum unit 4 can be calculated by the empirical formula. Then the inductance of each minimum unit can be calculated in parallel, so that the total inductance can be estimated and the mutual inductance between the minimum units can be neglected. The first three minimum units may have some errors because of the layout of power supply ground. The errors are closely related to the distance and the height of PEC. If you want to calculate very accurately, you can fit the formula for each arrangement. For engineering purposes, the errors that have been verified are less than 20%. The layout of power supply ground can be neglected. This will not be repeated here.

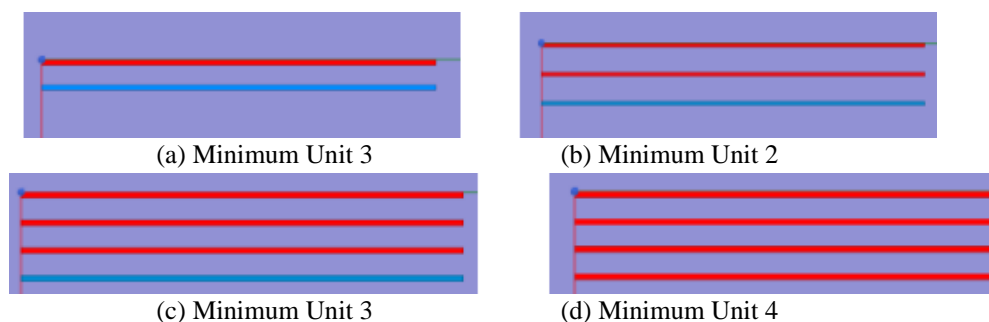


Figure 4: Pin partition unit

Because of the linear relationship between inductance and length, this section uses double fixed-point method to determine the linear fitting formula of inductance with respect to length. The specific process is as follows: Fitting formula first determines the range of variables, and then fits through curve-fitting tool in MATLAB software (polynomial fitting). Based on the engineering point of view, thickness and width on the one hand do not change much in primary flow sheet, and on the other hand, it changes little in primary flow sheet. On the one hand, this factor has little influence on inductance. The thickness h_t of Pin coplanar was determined to be 0.12-0.2 mm (the fitting formula was based on the length of 0.16 mm), and the width range was determined by the same fitting method. The fitting variables are:

- 1) The range of PEC and H is 0.5-2.1 mm.
- 2) Determine the distance d between two adjacent roots as follows: $> 0.2\text{mm}$; (Mutual inductance is neglected when the distance is greater than 6mm).
- 3) The range of length Len is 2 MM-16 mm.

Because the distance d and height h are determined, and the length Len is approximately linear, we use the method of fitting the linear coefficients a and B according to the variables d and h , and then calculate the inductance of a certain length Len according to the linear formula of $L=a*Len+b$. Specific ways are as follows: because the length span is from 2mm to 16mm, in order to ensure the accuracy of fitting formula, we select 2mm, 14mm polynomial fitting formula a_{1p1g} , b_{1p1g} , and then estimate the inductance formula of about 2mm-16mm length.

$$a_{1p1g} = 0.2183 + 0.5551 \times d - 0.08948 \times h - 0.4919 \times d^2 + 0.5451 \times d \times h + 0.02413 \times h^2 + 0.1749 \times d^3 - 0.1757 \times d^2 \times h - 0.1241 \times d \times h^2 - 0.02704 \times d^4 + 0.02012 \times d^3 \times h + 0.04074 \times d^2 \times h^2 + 0.001517 \times d^5 - 0.0005822 \times d^4 \times h - 0.003788 \times d^3 \times h^2;$$

$$b_{1p1g} = -0.003764 + 0.1959 \times d + 0.0697 \times h - 0.1423 \times d^2 + 0.0885 \times d \times h - 0.0294 \times h^2 + 0.04355 \times d^3 - 0.02128 \times d^2 \times h - 3.537 \times 10^{-5} \times d \times h^2 - 0.006105 \times d^4 + 0.002561 \times d^3 \times h - 0.001544 \times d^2 \times h^2 + 0.000324 \times d^5 - 0.0001448 \times d^4 \times h + 0.0002349 \times d^3 \times h^2;$$

$$L_{1p1g} = a_{1p1g} \times Len + b_{1p1g};$$

For the Minimum Unit 4 without ground wire, we calculate self-inductance by fitting the formula of single microstrip PIN and mutual inductance by two microstrip PIN. The inductance matrix is composed of the above two parts, and the total inductance of Minimum Unit 4 is calculated by the formula.

$$L_t = \frac{1}{\sum_{i=1}^{m+n-1} L_{m+n-1,i}^{-1}}$$

After fitting the formula, the total inductance is calculated according to the relationship between the smallest element and the non-smallest element in parallel according to the following formula:

$$L = \frac{1}{\frac{num_1p1g}{L_{1p1g}} + \frac{num_2p1g}{L_{2p1g}} + \frac{num_3p1g}{L_{3p1g}} + \frac{num_more}{L_{more}}}$$

4. Result Verification

According to the calculation method of capacitance and inductance in Pin part of QFP package, we select the

specific distribution of the given actual model. According to the extraction of parasitic parameters by HFSS, Q3D and other electromagnetic software, parasitic parameters are calculated by the calculation method discussed by myself. Then the parasitic parameters are compared. The parasitic parameters of Pin part of QFP package are explained in the form of error percentage and the model comparison chart of impedance in the next section. The extraction approximation is accurate and reasonable.

- 1) Model 1 is VSS_DOWN model: the edge profile is rectangular, its edge length is 0.12mm, that is, its width is 0.13mm, and its height is 0.12mm. The number of power pin is 5; the number of ground pin is 3; the arrangement of power ground is PPGPPG (where P stands for power pin and G stands for power pin), the length is 6.06mm, and the distance between each two is 1.35 mm.
- 2) Model 2 is VSS_DOWN2 model: the edge profile is rectangular, its edge length is 0.12mm, that is, its width is 0.13mm, and its height is 0.12mm. The number of power pin is 8; the number of ground pin is 0; the arrangement of power ground is PPPPPP (where P stands for power pin and G stands for power pin), the length is 6.06mm, and the distance between each two is 1.35 mm.
- 3) Model 3 is VSS_DOWN_TO_LEAD model: the edge profile is square, its edge length is 0.12mm, that is, its width is 0.12mm, and its height is 0.12mm. The number of power pin is 7; the number of ground pin is 2; the arrangement of power ground is PPGPPGPPP (where P stands for power pin and G stands for power pin), the length is 7.84 mm, and the distance between each two is 1.1 mm.
- 4) The fourth model is VSS_DOWN_TO_LEAD2 model: the edge profile is square, its edge length is 0.12mm, that is, its width is 0.12mm, and its height is 0.12mm. The number of power pin is 5; the number of ground pin is 4; the arrangement of power ground is PGPGPGP (where P stands for power pin and G stands for power pin), the length is 7.84 mm, and the distance between each two is 1.1 mm.

As shown in the table below, the error of the numerical solution of extracting pin parasitic inductance by this method is less than 15%.

Table 1: Comparison of Calculated Inductance by Pin and
Extracted Inductance by HFSS

	$L_{\text{计算}}$	$L_{\text{提取}}$	误差 ε %
模型一	1.27 nH	1.36 nH	6.7
模型二	1.47 nH	1.42 nH	3.5
模型三	0.94 nH	0.91 nH	3.3
模型四	1.07 nH	0.95 nH	12.6

5. Conclusion

In this paper, from the engineering point of view, a fast calculation method of PIN conductor inductance in QFP packaging is proposed. Through the validation of equivalent model and algorithm, this method is simple, practical, fast and accurate. It can quickly and approximately calculate

PIN conductor inductance in QFP packaging, and can provide some guidance for researchers and developers.

References

- [1] Ji Y and Hubing T H. On the modeling of a gapped power-bus structure using a hybrid FEM/MOM approach. IEEE Transactions on Electromagnetic Compatibility. 2002, Nov., 44(4). pp. 566–569.
- [2] Elfadel I M, Huang H M, Ruehli A E, et al. A comparative study of two transient analysis algorithms for lossy transmission lines with frequency-dependent data. IEEE Transactions on Advanced Packaging. 2002, May, 25(2). pp. 143–153.
- [3] Branin F H. Transient analysis of lossless transmission lines. Processing of the IEEE. 1967, Nov., 55, pp. 2012–2013.
- [4] Nakhla N M, Dounavis A, Achar R, et al. DEPACT: delay extraction-based passive compact transmission-line macromodeling algorithm. IEEE Transactions on Advanced Packaging. 2005, Feb., 28(1). pp. 13–23.
- [5] Lu J M, Li Y S and Zhang M S. An Efficient Spice-Compatible Model for Striplines Including Cavity Resonant Effect. IEEE Transactions on Electromagnetic Compatibility. in press.