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Utilizing VHDL for Teaching CPU Design in Engineering Education: An Approach to Build Students' Capacities to Understand and Develop Complex Projects by Applying FPGA, PBL, and ML Technologies

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Abstract: ***This studywas conducted to help students understand and develop complex projects applying the Field Programmable Gate Arrays (FPGA) technology, Project Based Learning (PBL) and Micro-learning (ML), which enable students to successfully accomplish complex projects in short time.The central processing unit (CPU) design is based onVHSIC (Very high-speed integrated circuit), which is used for VHDL (VHSIC Hardware Description Language) that helps accomplishingcomplex projects by applying both PBL and MLmethods. The mentioned PBL and ML methodsfacilitate students to solve problemspertaining topractical projects, specifically the problems, which cannot betheoretically solved. In addition, these methods develop students' skills to address and solve complex design problems, help them achievetheir desired results, and assure flexible design that can be modified.They are ideal approaches to solveengineering problems and encourage students to get"self-directed independent learning". Moreover, the proposed curriculum project is based on the development of practical/real-world projects.The project presented in the current study was designed to excite, attract, and challenge students when they deal with complex project designs. This paper presents a new educational approach to computer engineering education for university students. The instructional design addresses some complex and open research projects using project-based learning; however, a new teaching method has been created by combining PBL and ML.***

Keywords: CPU, FPGA, VHDL, Digital Design. Electronic, Engineering Education, Micro Learning, Project Based Learning

1. Introduction

The intention of this study isapplyingthe combination of Project-Based Learning and Micro Learning (PBL and ML) as a novel teaching method in order to help students achieve the desired results, and this approach is needed because traditional education no longer fulfills students' learning needs and their requirements to handle complex projects.

There is growing demand for teaching the CPU function through effective learning methodology; however, it is a complicated process. This is possible byusing FPGA technology and some new teaching methods, which are part of Project Based Learning and Micro-Learning. These approaches are mainly chosen to help students learn better. Consequently, it makes the learning process more attractive and useful(Kiray, Demir et al. 2013).Engineering education should be oriented with modern educational techniques specifically in the institutions, which impart higher education because advanced methods and devices enhance students' understanding and performance (Flochová, Hollý et al. 2011).

Many universities are using FPGAin their electronics and computer engineering departmentsbecause itincreases students' understandingof the subject and economizes the time consumption(Koch and Golze 1993).Accordingly, there is a need for finding new ways to guide students and help them solve problems, which they might face in the laboratory (Bradley-Levine and Mosier 2014).In addition, there is growing need to educate students and develop engineering skills to improve theirdesigns. This is essential because of multidisciplinary nature of these systems that makes it harder forstudents to exercise all of its aspects (Kumar, Fernando et al. 2013).Students must develop and design the existing complex electronic circuits and they need to continue improving them even when the circuits' complexity is increased (Machado, Borromeo et al. 2009). Moreover, it is demanded of students to useproject-based learning approach for disseminating robotics education in the context of control engineering that uses integrated robotic platform (Mysorewala and Cheded 2013).

Keeping in view the above-mentioned realities, this study aims atsolvingmajor problems, which students are facing in the traditional education systems; for example, students are insufficient to understand when the syllabus is completed in a short time. For that reason, the Project-Based Learning and Micro-Learning can beusedas novel teaching methods in order to deal with the problems of the traditional methods. Later, we compared the results of the PBL-ML method with the results of the traditional engineering education process.

Another aim of this study is to improve the simulator-based approach by including the hardware design in the teaching method to enable students get hands-on hardware and software training during the computer architecture course. In addition, the target is implementing CPUdesign via

VHDL (Very high-speed integrated circuit Hardware Description Language) design by introducing FPGA technology througha couple of teaching methods: Project-based Learning and Micro-Learning.

2. Methodology

We applied quantitative research methodology for collecting datathrough distributing survey questionnaires. This study has revealed the importance of Project-Based Learning and Micro-Learning methods for engineering education. Besides, we also compared the combination ofPBL and ML methodologies with the traditional learning procedure. This study was accomplished at the TurgutÖzal University and the Kastamonu University, Turkey. Two groups of students were chosen as the population of this study. The first group had 46 students whereas the other group had 34 students. First, we identified the students' problems in traditional education. This identification wasbased on the students' opinions. Then, we formulated a comprehensive plan to solve the reported problems using a new technique based on FPGA, PBL and ML in two separate semesters. In the first semester, education was imparted through traditional processes; i.e.without using FPGA, PBL, or ML. In the second semester, FPGA technology and the PBL-ML combination were applied. The assessment process was accomplished through analyzing questionnaires, homework, mid-term and final exam results.

Practical implementation of the study was performed through the following procedure:

a) A complex project was designed and divided into useful and attractive examples. After that, the PBL and ML methods were applied to all the contents of the subject. These activities are summarized as follows:
   - Developing a project combining various types of hardware and software
   - Designing CPU by VHDL Technology
   - Applying FPGA Technology.
   - Using PBL and ML as methods ofeducation

b) The problems pertaining to the traditional educational methods can be grouped under five main topics:
   - Difficult to understand
   - Inappropriate for complex project design
   - Time Consuming
   - No possibility to limit educational time consumption
   - Use of breadboard in lab

The organizational plan of the second non-traditional approach is evident in Figure 1.

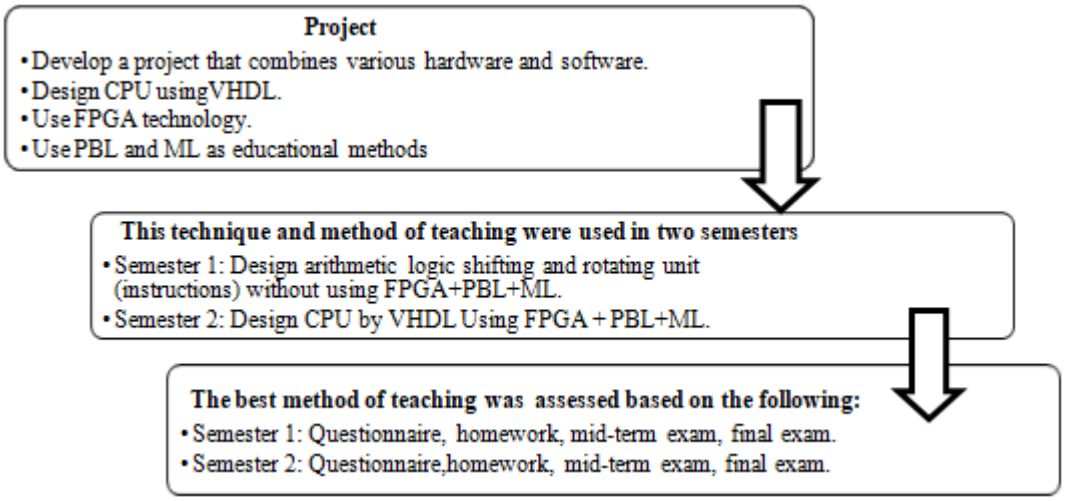


Figure 1: Plan to collect data for both education methods

2.1. Field-Programmable Gate Array (FPGA)

FPGA has become a significant technology for modern electronic design. Besides, it has been currently consideredas the most important implementation technology for digital systems when the design cycle requires a specific time period,and besides, it can be easily adapted to design the teaching curriculum. Moreover,it has the ability to update many applications.

2.2. Project Based Learning (PBL)

PBL is another educational method that requires students to learn a set of skills and topics while they are in the process of accomplishingtheir own projects. Those projects are real-world projects. Using this method of teaching helps students develop their communication skills and teamwork. In addition, students are encouraged to take responsibility for their learning experience, and transform their passive learning patterns into active patterns.

2.3. Micro learning (ML)

Micro-Learning is a way of teaching and delivering content to the students in small and very specific parts.Micro-learning emerged from micro-content. Micro-Learning involves learning in smaller steps and it goes hand-in-hand with the traditional e-learning process.Through micro-learning, the students learn how to deal with the sub-block components, how to create modules for each part, and how to make productive modules in educational sense(Said and Çavuş).

To produce a good project in the course, the FPGA technology, Project Based Learning and Micro-Learning methods should be combined; consequently, students can

develop their abilities to solve complex design problems, as depicted inFigure 2.

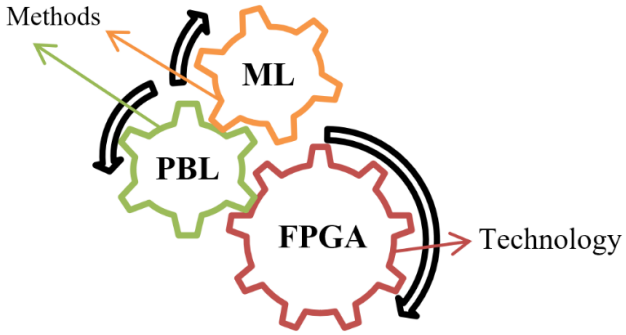


Figure 2: Interacting the three ideas to produce a good project in the course

While starting the CPU design, the first step is dividing the project into many parts to deal with the complexity of the project. This is possible by using the ML method, which helps students understand and accomplish their final project design, as shown in Figure 3.

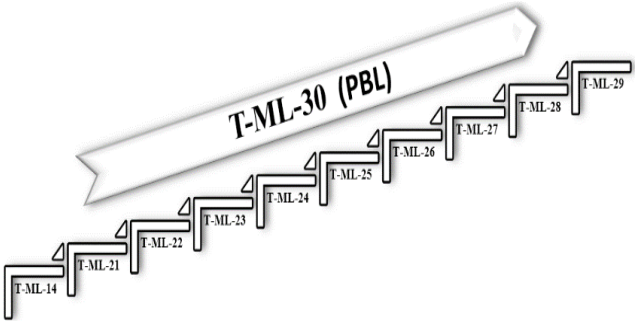


Figure 3: CPU design with sequential steps using ML and PBL; **T**: Theoretical, **P**: Practical

In order for students to understand this method and to befaster and more efficient at the beginning of the course, students are given the following steps to follow:

- A detailed tableand splitting lectures were providedinto three different levels of complexity, from easy to complex. The following table shows the project setup in three versions with three levels of complexity. Three levels were identified in each lecture, as shown in Table 1.

Table 1: Types of lecture levels

Code	Code Name	Code Type
V1	Version one	Homework I, the same subject was taught during the lecture.
V2	Version two	Homework II, between Version one and Version three, and the mid-term project.
V3	Version three	Homework III, complex project.

- A presentation was prepared that showed the use of new technology (FPGA) and teaching methods (PBL and ML) for this course during three-hour time span.
- A review of the digital CPU design is needed within two hours of the first week.
- A complete image of the experimental design is displayed and explained before the lecture begins.

2.4. The CPU Design Experiment

This experiment has beendivided into two levels; the firstlevel depends on MLwhile the second leveldepends on project-based learning, as shown in Figure 4.

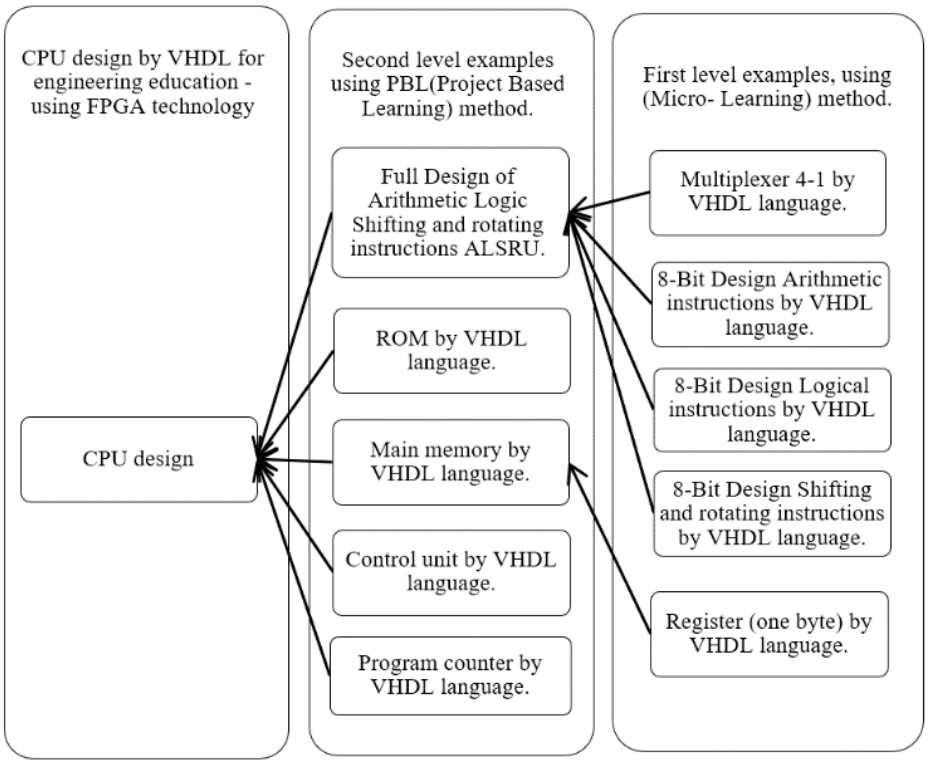


Figure 4: CPU Design by VHDL using FPGA technology and two educational methods PBL and ML

This project has been divided into smaller sub-projects from simple to complex steps, i.e. from micro-learning to project-based learning. Topic selection is needed in the process of designing the project, which has been shown in Figure5.

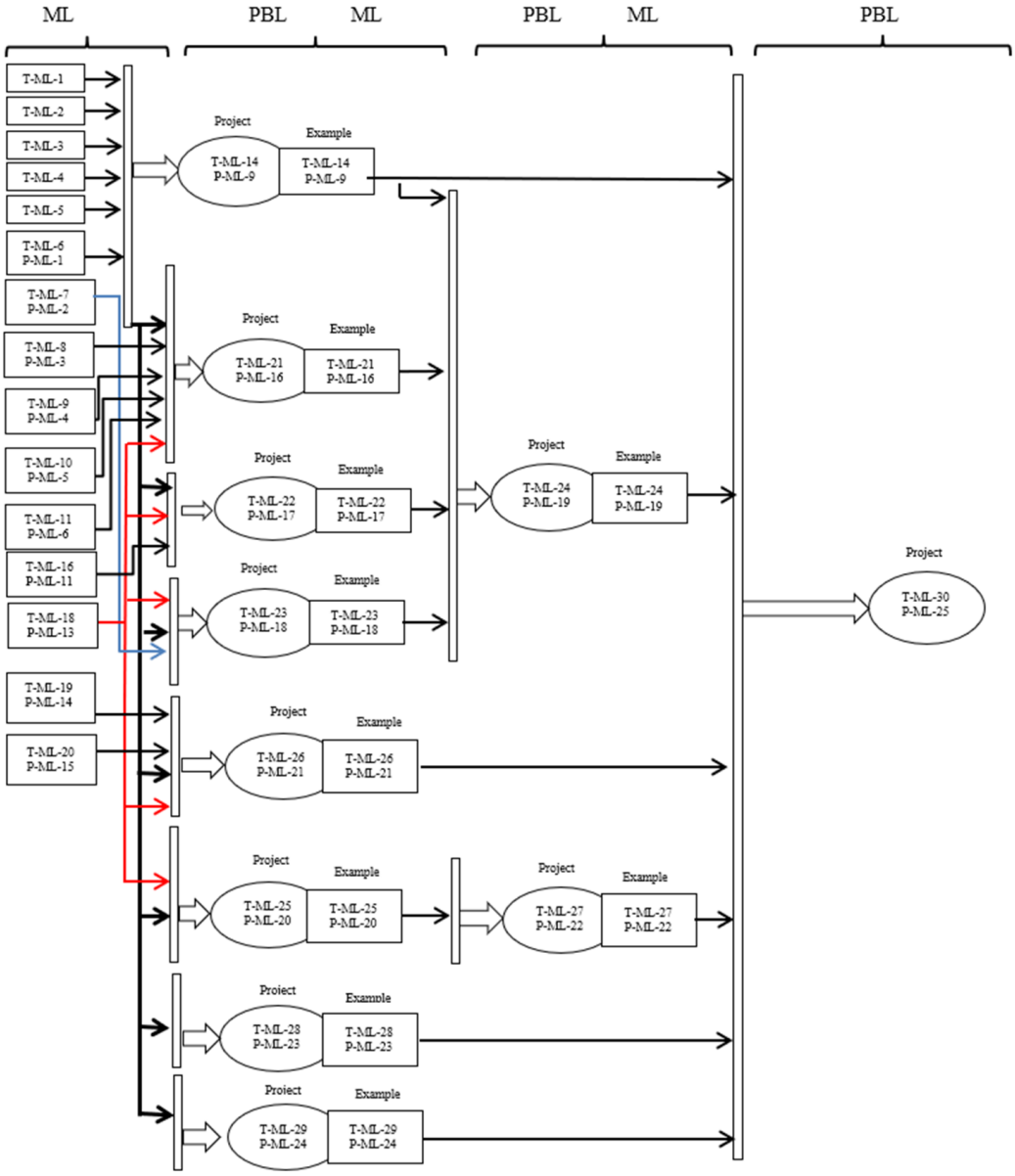


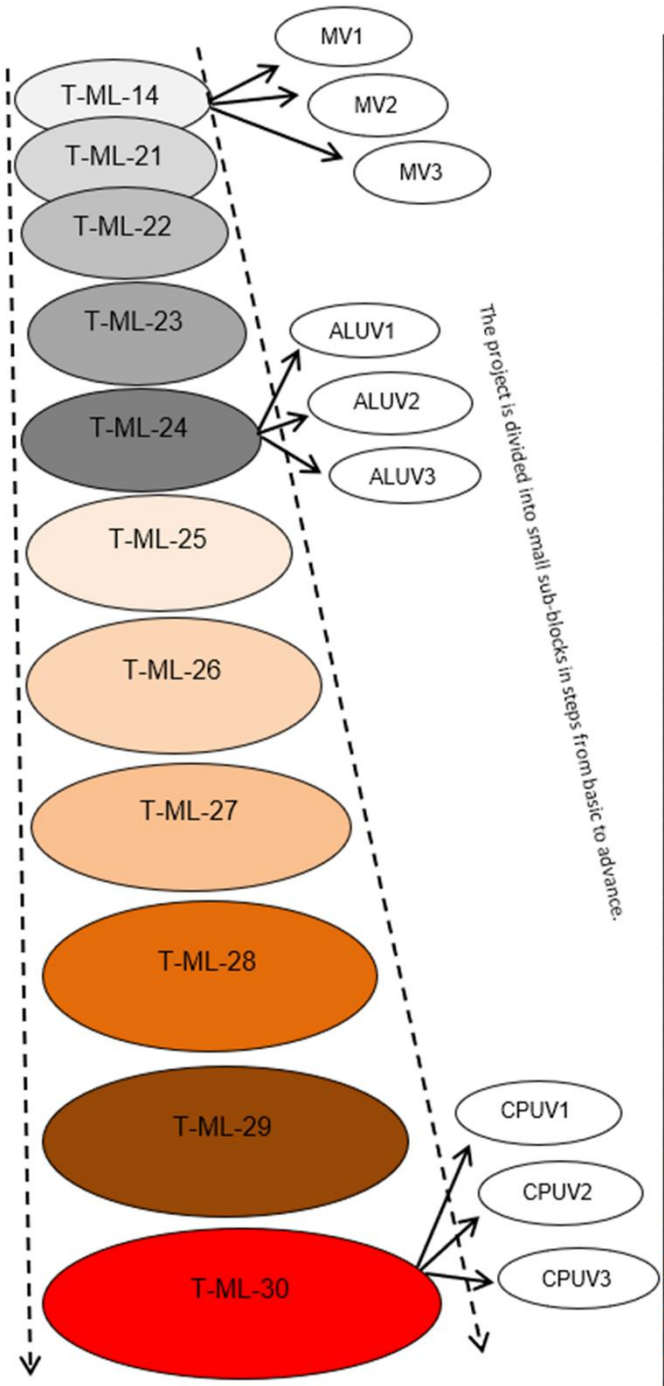
Figure 5: Project steps in small sub-blocks from simple to complexsteps

It is possible to create a project using a set of examples, and this project may serve as an example to the designers of other more complex projects.

According to the obtained test results, using ML-PBL combination gives better results than using PBL only. Everytopic in each lecture was divided into three levels from simple to hard. While designing a project based on curriculum, the design can be divided into small sub-blocks in steps from simple to complex, as illustrated in Figure 6.Also, the codes used in the course are given in Table 2.

Table 2: Codes used in the course

Code	Title Name
MV1	Multiplexer 4-1 by VHDL language.
MV2	Multiplexer 8-1 by VHDL language.
MV3	Multiplexer 16-1 by VHDL language.
⋮	⋮
ALUV1	Design 4-bit arithmetic logic shifting and rotating instructions by VHDL language.
ALUV2	Design 8-bit arithmetic logic shifting and rotating instructions by VHDL language.
ALUV3	Design 16-bit arithmetic logic shifting and rotating instructions by VHDL languageusing new operational design.
⋮	⋮
CPUV1	Design 4-bit CPU by VHDL language.
CPUV2	Design 8-bit CPU by VHDL language.
CPUV3	Design 16-bit CPU by VHDL language.



The code	Example name
T-ML-1	Number systems
T-ML-2	Electronic signals and switches
T-ML-3	Arithmetic operations and circuits
T-ML-4	Boolean Algebra And reduction techniques
T-ML-5	Karnough map
T-ML-6	Logic gates
P-ML-1	Logic gates
T-ML-7	shift Registers
P-ML-2	shift Registers
T-ML-8	Half adder
P-ML-3	Half adder
T-ML-9	Full adder
P-ML-4	Full adder
T-ML-10	Half subtract
P-ML-5	Half subtract
T-ML-11	Full subtract
P-ML-6	Full subtract
T-ML-12	Encoder
P-ML-7	Encoder
T-ML-13	Decoder
P-ML-8	Decoder
T-ML-14	Multiplexer
P-ML-9	Multiplexer
T-ML-15	DE multiplexers
P-ML-10	DE multiplexers
T-ML-16	Comparator
P-ML-11	Comparator
T-ML-17	flip-flop
P-ML-12	flip-flop
T-ML-18	Registers
P-ML-13	Registers
T-ML-19	Counters
P-ML-14	Counters
T-ML-20	SM
P-ML-15	SM
T-ML-21	Arithmetic unit
P-ML-16	Arithmetic unit
T-ML-22	Logic unit
P-ML-17	Logic unit
T-ML-23	Shifting and rotating unit
P-ML-18	Shifting and rotating unit
T-ML-24	Arithmetic Logic Shifting and rotating unit
P-ML-19	Arithmetic Logic Shifting and rotating unit
T-ML-25	Register (one byte)
P-ML-20	Register (one byte)
T-ML-26	Program counter
P-ML-21	Program counter
T-ML-27	Main memory-RAM
P-ML-22	Main memory-RAM
T-ML-28	ROM
P-ML-23	ROM
T-ML-29	control unit
P-ML-24	control unit
T-ML-30	CPU
P-ML-25	CPU

Figure 6: CPU project divided into small sub-blocks from easy to complex steps, and symbols

2.5. Training groups

In this project, we used quantitative research methodology (experimental approach). Also, in this project, there are two groups of students, as shown in Figure7.The first group learned the computer architecture course without applying FPGA technologies, project-based learning and micro learning method, shown in Fig 7a.The second group was taught by applying FPGA technologies, project-based learning and micro learning method (using attractive and instructive examples), which has been shown in Fig 7b.

(a) **(b)**

Figure 7: Groups of the study.

The two methods were tested to understand which method is better for teaching. After the end of each semester, it became clear which method has shown better performance.

The performances of both the methods have been assessed throughquestionnaires, homework, mid-term exam, final exam, and tests of the first and fourth groups.This project has been implemented in two semesters, as shown in Figure 8.

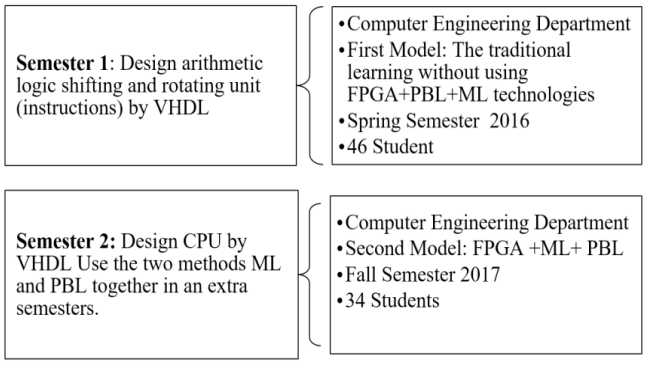


Figure 8: Content of two semesters

Semester 1: In this semester,arithmetic design, logic shifting and rotating instructions were given by VHDL in the Computer Engineering Department by traditional learning without using FPGA+ PBL + ML technologies. In Spring Semester 2016, the number of students, who attended this class, was 46, as Figure 8 shows.

Semester 2: In this semester, CPU design was taught by VHDL using project-based learning and micro-learning methods in the Computer Engineering Department using FPGA + PBL + ML technologies in Fall Semester2017. The number of students who attended this class was 34, as Figure 8 indicates.

2.6. CPU design by VHDL for engineering education and simulation

The CPU design used in the project and its simulation are given in Figures 9a and 9b, respectively.

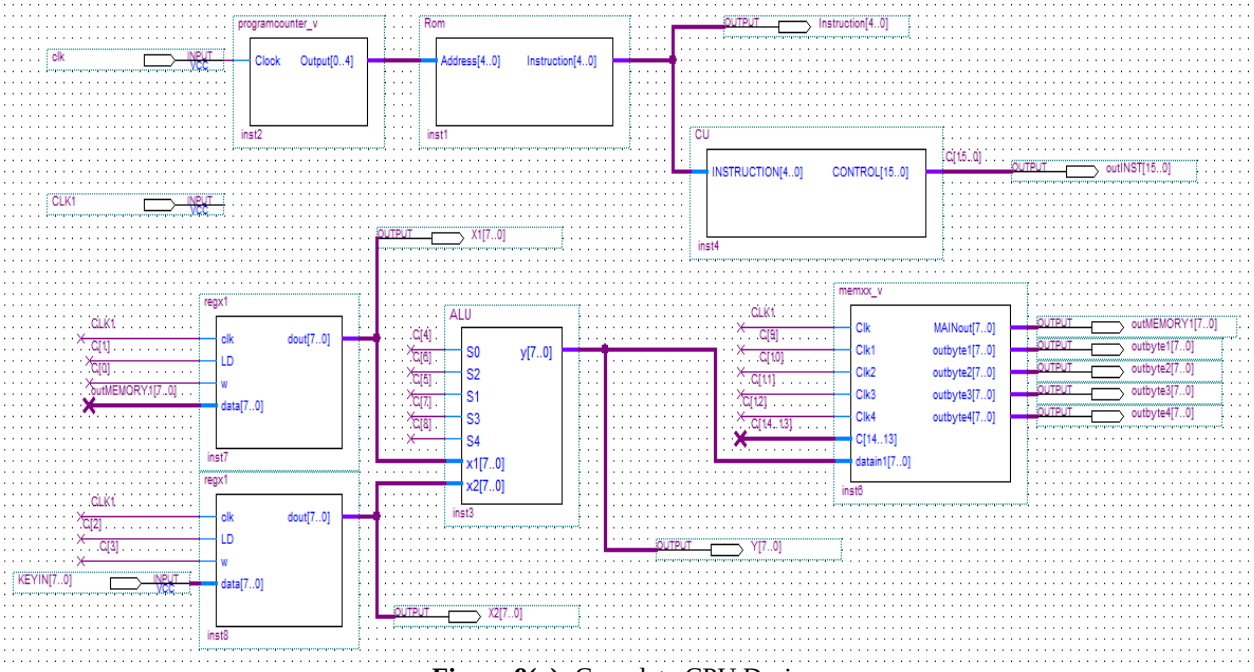


Figure 9(a): Complete CPU Design

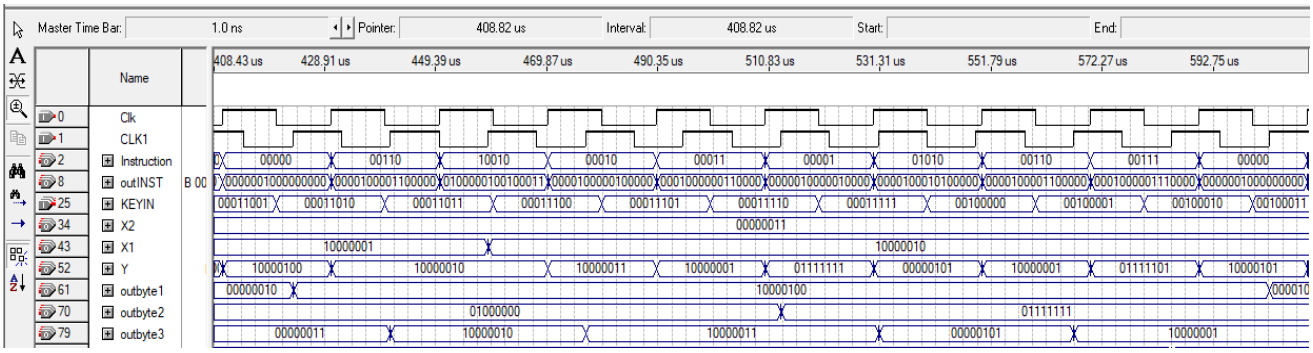


Figure 9 (b): Simulation for CPU

2.6.1 Control Unit

The control unit is a component of a computer's central processing unit (CPU) which directs operations of the processor. It controls communication and co-ordination between the input and output devices. It reads and interprets instructions and determines the sequence for data processing.VHDL codes for Control Unit (CU) is given Figure 10.

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY CU IS
    PORT (
            INSTRUCTION : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
            CONTROL : OUT STD_LOGIC_VECTOR (15 DOWNTO 0));
END  CU;

architecture beh of CU is
begin
process (INSTRUCTION)
 begin
CASE INSTRUCTION IS
   WHEN  "00000" =>
     CONTROL<="0000001000000000";--ADD
   WHEN  "00001" =>
     CONTROL<="0000010000010000";--SUB
   WHEN  "00010" =>
     CONTROL<="0000100000100000";--INC
   WHEN  "00011" =>
     CONTROL<="0001000000110000";--DEC
   WHEN  "00100" =>
     CONTROL<="0000001001000000";--AND
   WHEN  "00101" =>
     CONTROL<="0000010001010000";--OR
   WHEN  "00110" =>
     CONTROL<="0000100001100000";--XOR
   WHEN  "00111" =>
     CONTROL<="0001000001110000";--NOT
   WHEN  "01000" =>
```

Figure 10: VHDL codes for Control Unit (CU)

1) Number 1, when C4=C5=C6=C7=C8=0, it means that the operation is ADD, the value in the recorder X1 is combined with the value in the recorder X2 and stored in the recorder Y.
2) Number 2, when C4=1 and C5=C6=C7=C8=0, it means that the operation is SUB, the value in the recorder X1 is subtracted from the value in the recorder X2 and stored in the recorder Y.
3) Number 6, when C4=C6=1 and C5=C7=C8=0, it means that the operation is OR, the value in the recorder X1 is compared with the value in the recorder X2 and stored in the recorder Y.
4) Number 9, when C7=1 and C4=C5=C6=C8=0, it means that the operation is SL, The value in the X1 recorder is removed to one left bit and the results are stored in the recorder Y.
5) Number 13, when C8=1 and C4=C5=C6=C7=0, it means that the operation is M[0]→X1,and the value in the memory of the first location is transferred to the registrar X1.
6) Number 14, when C8=C4=1 and C5=C6=C7=0, it means that the operation is M[1]→X1. The value in the memory of the second location is transferred to the registrar X1.
7) Number 15, when C8=C5=1 and C4=C6=C7=0, it means that the operation is M[2]→X1. The value in the memory of the third location is transferred to the registrar X1.
8) Number 16, when C8=C5=C4=1 and C6=C7=0, it means that the operation is M[3]→X1. The value in the memory of the fourth location is transferred to the registrar X1.
9) Number 17, when C8=C7=C4=1 and C6=C5=0, it means that the operation is KEY→X2. The reading is done through the keyboard, and the results are stored in the recorder X1.

Control Unit Simulation is given in Figure 11.

Figure 11: Control unit simulation.

Control signal of the control unit is given Table 4.

Table 4: Control signal of the control unit

NO.	control signal				M[4]	M[3]	M[2]	M[1]	instruction					X2		X1	
		C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
1	ADD	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
2	SUB	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
3	INC	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
4	DEC	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
5	AND	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0
6	OR	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0
7	XOR	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0
8	NOT	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0
9	SL	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
10	SR	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0
11	RL	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0
12	RR	0	0	0	1	0	0	0	0	1	0	1	1	0	0	0	0
13	M[0]→X1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1
14	M[1]→X1	0	0	1	0	0	0	0	1	0	0	0	1	0	0	1	1
15	M[2]→X1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	1
16	M[3]→X1	0	1	1	0	0	0	0	1	0	0	1	1	0	0	1	1
17	KEY→X2	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0

2.6.2 Read-only memory (ROM)

It means Read-only memory as it saves all the instruction codes tomake the CPU implement them according to their priority. ROM design by VHDL is given Figure 12.

```
1  LIBRARY ieee ;
2  USE ieee.std_logic_1164.all ;
3  --USE ieee.std_logic_unsigned.all ;
4
5  ENTITY Rom IS
6      PORT (  Instruction : out bit_VECTOR (4 DOWNTO 0);
7              Address : INTEGER range 0 to 31 );
8  END  Rom;
9
10 architecture beh of Rom is
11     type arr is array (0 to 31, 0 to 4) of BIT ;
12     constant ROM : arr := (
13     ("11001"),("00000"),("10000"),("00101"),("01000"),("00001"),("00010"),("00010"),
14     ("00101"),("10001"),("00000"),("00100"),("00110"),("00111"),("01011"),("00000"),
15     ("01011"),("10011"),("01001"),("01010"),("01000"),("00000"),("00110"),("10010"),
16     ("00010"),("00011"),("00001"),("01010"),("00110"),("00111"),("00000"),("00110")
17     );
18 begin
19 process (Address)
20  begin
21  Instruction(0)<=ROM(Address,4);
22  Instruction(1)<=ROM(Address,3);
23  Instruction(2)<=ROM(Address,2);
24  Instruction(3)<=ROM(Address,1) ;
25  Instruction(4)<=ROM(Address,0) ;
26  END PROCESS ;
27  end beh;
```

Figure 12: ROM Design by VHDL

A simulation for ROM is given in Figure 13.

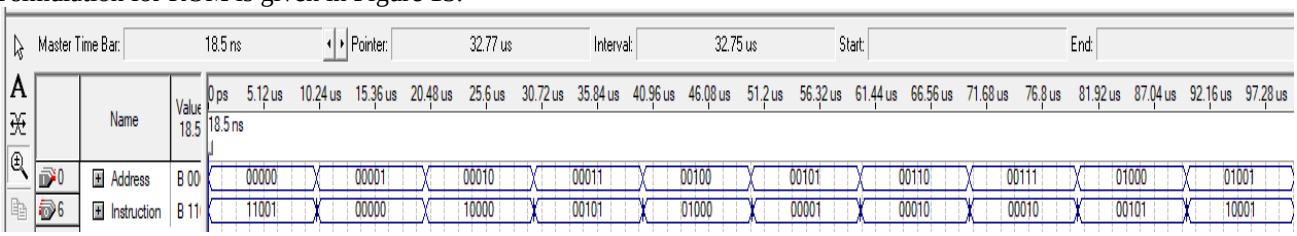


Figure 13: Simulation for ROM

Addressing instructions and commands are given in Table 5.

Table 5: Addressing instructions

Addressing instruction	Details of the instruction
11001	Read from keyboard and after that, store in register X2.
00000	ADD addition of registers X1 and X2, after that, store the result in the memory(byte one).
10000	Load data from memory (byte one) into register X1.
00101	OR logical operation is applied on bits of registers X1 and X2, and after that, store the result in the memory (byte two).
01000	SL (Shifting left) instruction shifts the content of register X1 towards one bit on the left (byte one).
00001	SUB subtraction of registers X1 and X2, and after that, store the result in the memory(byte two).
00010	INC increases the value of register X1 by one, and after that, stores the result in the memory(byte three).
01001	SR (shift to the right) instruction shifts the content of register X1 by one bit towards right (byte two).
⋮	⋮

3. Results and Discussion

The results of the tests were obtained through questionnaires, homework, mid-term exam, and final exam.From this test, the difference between the two learning methods, i.e. the traditional learning method without FPGA + PBL + ML, and the second method that uses FPGA + PBL + ML, we found substantial difference. According to our finding, the second method is better than the first method.

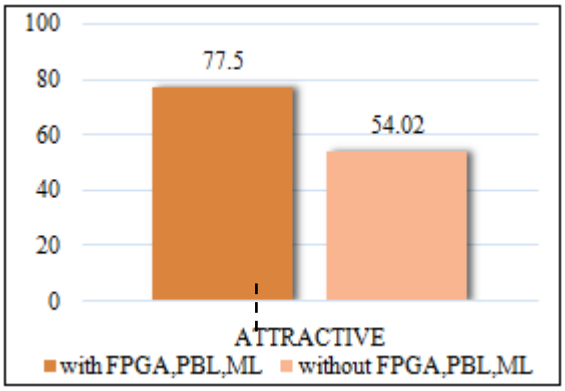


Figure 14: Comparison between instructive factor values

The data analysis of instructive factor for the method (FPGA +PBL + ML) showed clear difference in terms of instructive factor values according to the findings of our study, and the results proved that learning by using FPGA technology, project-basedlearning and micro-learning methods has substantially higher instructive effectiveness as compared to traditional learning method, as Figure 14 indicates.

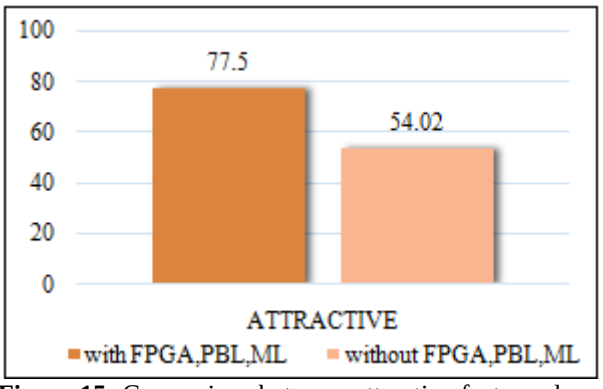


Figure 15: Comparison between attractive factor values.

The data analysis of attractive factor model shows that using the new method (learning through FPGA + PBL + ML) showed a clear difference in the values of the attractive factor in the study, and the results show that using combination of FPGA technology, project-basedlearning and micro-learning methods is better in terms of attractive factor as compared to the traditional learning method, as Figure 15 clearly indicates.

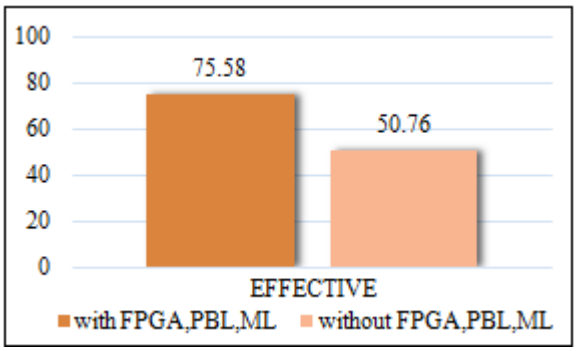


Figure 16: Comparison between effective factor values.

The data analysis in terms of effective factor shows that the new method (using combination of FPGA + PBL + ML) showed clear difference in the effective factor values for studied population of students; therefore, learning by using FPGA technology, project-based learning and micro-learning methods is more effective as compared to the traditional learning method, as Figure 16 indicates.

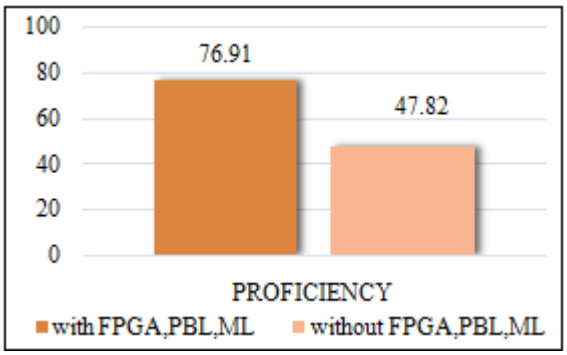


Figure 17: Comparison between proficiency factor values

The comparison between the proficiency factor values show that the new method (FPGA + PBL + ML) showed a significantly higher proficiency factor value, and the results of this method are significantly higher as compared to the traditional learning method, which means that this method results in higher proficiency, as Figure 17 indicates.

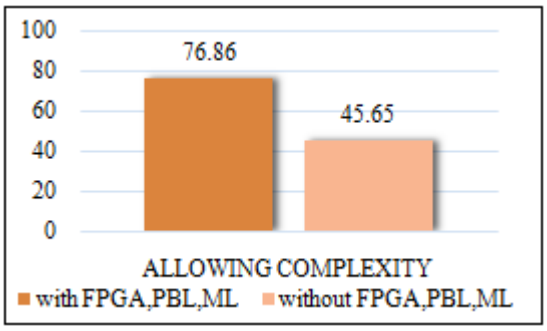


Figure 18: Comparison betweenallowing complexity factor values

The data analysis shows that allowing complexity factor for the new method (FPGA + PBL + ML) showed a clear difference in the values of the allowing complexity factor in the study, and the results show that learning by using FPGA technology, project-based learning and micro-learning methods allows more complexity as compared to the traditional learning method, as Figure 18 depicts.

Table 6: Results of the comparison of engineering education methods with respect to factors

Factors	Traditional learning without FPGA+ML	with FPGA+ML
Instructive	52.39	76.17
Attractive	54.02	77.5
Effective	50.76	75.58
Proficiency	47.82	76.91
Allowing complexity	45.65	76.86

The data analysis shows clear difference in terms of the values of all the factors analyzed in the study (Instructive, Attractive, Effective, Proficiency and Allowing complexity); therefore, the students, who were taught using FPGA technology, project-based learning and micro-learning methods, showed better results as compared to those students, who were taught using the traditional method, as Table 6 shows.

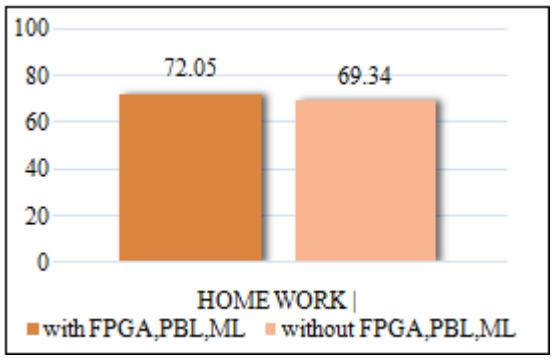


Figure 19: Comparison between Learning Methods for Homework I

The data clearly shows that the difference between the two learning methodscan be simply described by the fact thatthe homework is the same lecture and not difficult for students, as Figure 19 indicates.

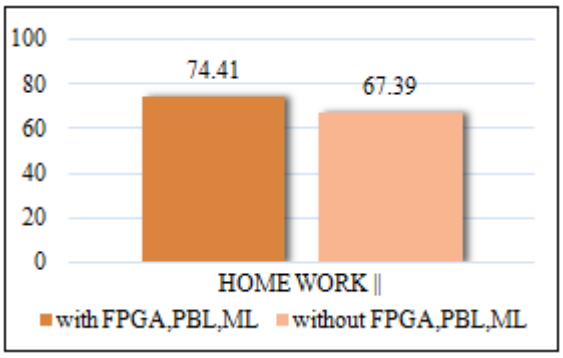


Figure 20: Comparison between Learning Methods for Homework II

The data analysis clearly shows that the second homework, in which the difference increased, was more difficult than the first homework, as Figure 20 shows.

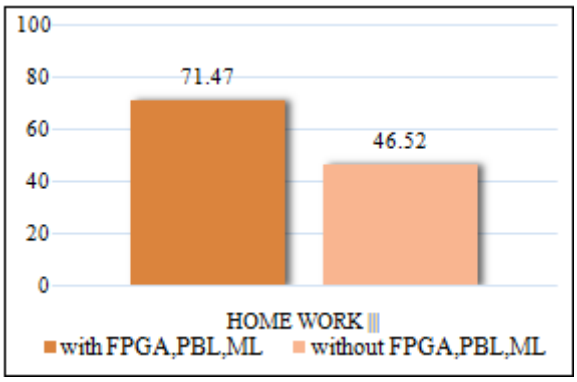


Figure 21: Comparison between learning methods based on Homework III.

The data analysis clearly indicates that the statistics of the third homework assignment showsubstantial difference because this homework was more complex as compared to the first and the second homework,as indicated inFigure 21.The data analysis clearly depicts that the FPGA + PBL + ML method substantially allows students to understand and do complex assignments because these methods arouses interest among students, speeds up their learning process, and helps them deal with the design complexity, as Table 7 indicates.

Table 7: Results of the comparison of educationalmethods by homework assignments

Homework	Traditional learning without FPGA+ML	Learning with FPGA+ML
Homework I	69.34	72.05
Homework II	67.39	74.41
Homework III	46.52	71.47

The second homework assignment can be solved after understanding and performing the first homework assignment.The third home assignment can be accomplished after understanding and solving the second homework assignment; therefore, the third home assignment is the most complex of all.Based on the obtained values, using project-based learning and micro-learning is advisable to deal with assignment complexity.

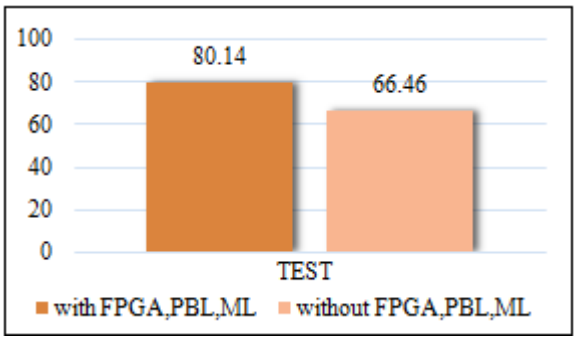


Figure 22: Results of mid-term test.

The results of the mid-term test show that the students who were taught using the new method (FPGA + PBL + ML) scored better in the mid-term exam. The results also show that FPGA learning, project-based learning, and micro-learning methods help students perform much better in their tests as compared to traditional learning method, as Figure 22 indicates.

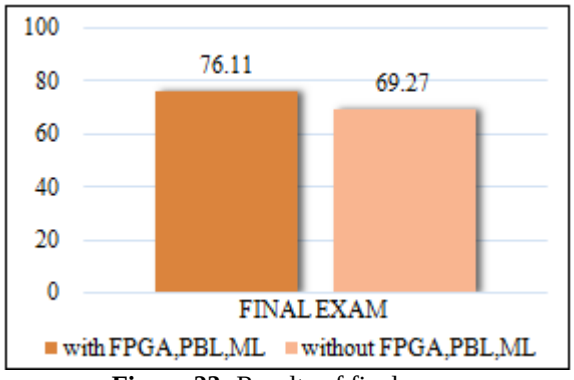


Figure 23: Results of final exam

The results of the final exam show that the students, who were taught using the new method (FPGA + PBL + ML) clearly scored better than the students who were taught using conventional method. The results obtained through FPGA learning, project-based learning, and micro-learning methods are much better as compared to traditional learning method, as shown in Figure 23.

Table 8: Comparison between educational methods in the mid-term test and final exam

Type of test	Traditional learning without FPGA+ML	with FPGA+ML
Mid-term Test	66.46	80.14
Final Exam	69.27	76.11

In the mid-termtest and final exam, the ratioswere not so different but still, it has been proven that project-based learning and micro-learning methods result in better exam performance of the students as compared to the traditional learning method as Table 8 indicates.

4. Conclusion

In this study, a new approach has been introduced for conducting engineering education programs in order to make students understand, use and design computer architecture. CPU design was used to improve the students' abilities to understand the subject in short time.As a result, employing theFPGA, PBL, and MLmethodswere proved as much better and more useful methods as compared tothe traditional learning method.

In addition, the study is aimed at extending and applying ML with PBL in a systematic course pertaining to the curriculum of computer architecture.Moreover, students' performances improved when FPGA, ML, and PBL methods were used, and besides, students' responses were faster than the traditional learning methods. This result was observed in students' responses to the questionnaire, particularly in the contexts of efficiency factor, allowing complexity factor, and ability to perform their home tasks. Furthermore, we concluded that FPGA learning is important for both engineers and students because it develops their abilities to gain knowledge and effectively use their time.

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