International Journal of Science and Research (IJSR)
ISSN: 2319-7064
Impact Factor (2018): 7.426

Modelled Approach of Avionics LRUs for System Health Management

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Abstract: ***In this research paper, a complete investigation has been performed regarding the maturity of avionics systems from different phases of the development. Here, the interaction between the various Line Replaceable Units (LRUs) and the Remote Data Concatenator (RDC) through ARINC-429 protocol using SIMULINK is modelled and simulated. The various signals from all the LRUs are combined systematically and arranged by a scheduler, effectively combining them into a single signal through a single channel to the RDC. Further it effectively simulates various situations in which the failure of the system or certain parts of the system occurs. Each condition has been modelled based on the typical reasons for failures and the same is simulated. Hence few LRUs are modelled and ARINC 429 protocol is also designed, and the model is simulated by transmitting data in ARINC format and the receiving the data at remote data concatenator and storing them. Various levels of failures are also modelled and simulated. This helps in better understanding of how the systems work. The simulations are carried out for three LRUs namely: RADALT, AFCS and ADF. Each LRUs at transmitter side are simulated for each parameter, parameters transmitted at various instants, periodicity of all the parameters are also verified. At the receiver, parameters of all the LRUs received at correct instants have been simulated.***

Keywords: ARINC 429, LRU, Time-Scheduler, RDC, Label Congruency

1. Introduction

Inter-system communication and signaling in avionics have been pivotal factors ever since electronics was applied to aircrafts and spacecrafts. To construe the challenges faced by the wide use of general computing methods in commercial avionics, standards such as ARINC 419 and revised ARINC 429 were formed by group of aviation industries. Since its use in industries, ARINC 429 has been modified very less. It was first designed during the late 70s. ARINC 429 has some limitations in meeting the current trend of flexible system design and increase in system complexity. Avionics Full Duplex has emerged as a proven solution with modern Ethernet technology, safety and functional availability that can handle current demands.

Avionics and aircraft engine manufacturers exploited the advantage of commercially available data bus technology that had a proven advantage of reduced weight and manufacturing time which in turn increased the airborne system performance. This wish persuaded producers on believe in the lines about restoring unidirectional buses. Furthermore, point-to-point wiring information Buses for example, such that ARINC 429 for swift and light-weight bi-directional data Buses [2].

Data buses transfer information between line replaceable units (LRUs) installed in an aircraft.

Aircraft and avionics manufacturers proposed to use different types of data buses on aircraft. Application engineers have substantial freedom during the process of designing a data bus as there are many logical configurations, physical layers in airborne systems, which includes message traffic, data transfer protocols, formation of data packets etc., allowing avionics manufacturers, data bus vendors, and system integrators more laxity when configuring data buses. Multidisciplinary designs of controls among many fabricators, vendors, and integrators, are in fact the critical steps for this flexibility to validate the engine design or the aircraft design as the whole, that helps in determination of compliance to the regulations, and to maintain continued airworthiness

Aircraft Data Networks have been rapidly growing since the evolution of aviation electronics that started during the 18th century. Electrical aviation started with a few discrete analog systems like - radar, cockpit displays and navigation & communication equipment. The intricacy involved in aircraft design became quantum with the evolution of digital electronics industry; as many standalone systems were designed and manufactured. This initiated the necessity to interconnect these systems and to connect via computer which in turn helps the pilot to visualize all factors responsible for the successful flight [4].

This led to the invention of data buses, with that emerged a standard for transmission and reception of data that would help in efficient data transfer. One of the earliest protocols was designed by Aeronautical Radio Inc and is widely known in civil aviation field, by the name ARINC. ARINC 419 was its first release with standards for analog electronic equipments. Later its digital counterpart was released under the name ARINC 429.

Presently, the electronics industry and the aviation industry have advanced enormously. Each has its own advantages and limitations such as power consumption, increase in number of cables which in turn increases the weight and has an influence on aircrafts 'efficiency in terms of number of passengers, cargo, etc. Crucial aspect is safety and reliability of data. ARINC 429 cannot cope with modern systems. Thus, the birth of new protocol, Avionics Full Duplex Network popularly known as AFDX network, which works on Ethernet.

2. Architecture

The block diagram of the architecture of an avionics health management system is shown in Fig 1. It consists of a CNS system, different types of displays, radar systems and remote processors which are connected through the data buses. The avionic system architecture refers to the avionics instruments layout in the cockpit which is a typical location for avionic equipment, including control, monitoring, communication, navigation, weather, and anti-collision systems.

There has been an achievement towards centralized control of the multiple complex systems fitted on to the aircraft that includes engine monitoring and management. Health and Usage Monitoring System are integrated with aircraft management computers to give the pilot an early warning of LRUs' failure that will need restoration. The combined modular avionics concept proposes an integrated architecture with application software compact beyond a cluster of common hardware module. The fourth-generation jet fighters and the latest generation of airliners use it [9].

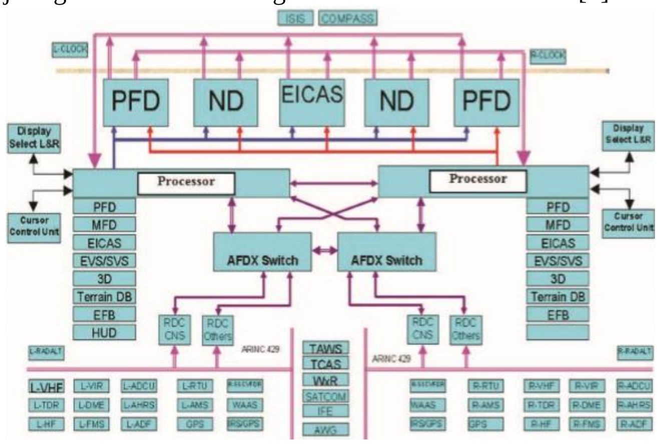

Figure 1: Architecture of avionics System

3. Objective

This experimental study aims at converging the ARINC 429 data buses and make it feasible to use it with AFDX (ARINC 664) so as to successfully upgrade to integrated modular avionics by using the existing buses which in turns will have economic benefits. It mainly focuses on modelling and simulating LRUs' transmitter and receivers and combining data at RDC, furthermore simulating various failures associated with the architecture [5].

This involves the simulation and analysis of interaction between the various LRUs (Line Replaceable Units) and the RDC through ARINC-429 protocol using SIMULINK. Line Replaceable Units are components that are in charge of the data arriving from various measuring devices incorporated into the aircraft. They receive their respective inputs, convert the data into 32-bit sequences which is in turn sent periodically as the output. The various signals from all the LRUs are combined systematically and arranged by a scheduler, effectively combining them into a single signal through a single channel to the RDC. The purpose of this simulation is to effectively simulate various situations in which the failure of the system or certain parts of the system can be modelled and studied, and to observe the output for various conditions [1].

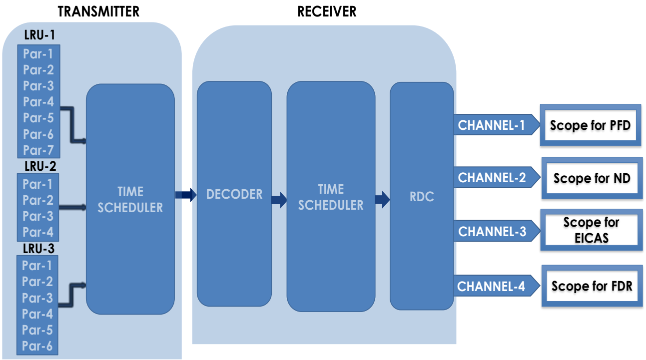

Figure 2: Flow Diagram indicating the data transmission from LRU to RDC

4. Methodology

This paper aims at designing a computational model of some of the communication and navigation modules (LRUs) each having defined parameters to determine their functionality and associated time rate defining how often the data has to be update depending on how frequently it changes. These data are saved at the RDC for further processing. Failure at each level will be modelled that helps in deciding the possible cause for the failure. The framework is as described below

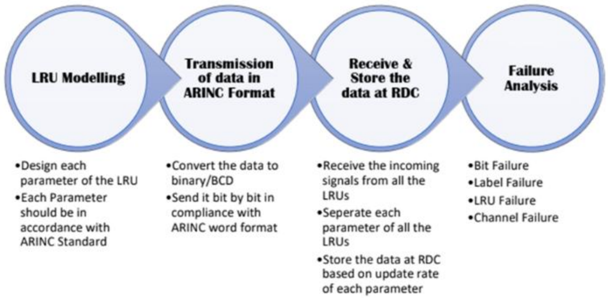

Figure 3: Overall Framework

5. Modelling and Simulation

A computational model is designed using Simulink. The fundamental objective of modelling and simulation is: the results are either correct or incorrect or correct but irrelevant. This helps in the realization of possible outcomes of the model. In the present work models can be classified under three main headings: LRU, Scheduler modelling which forms a part of Transmitter and RDC modelling which forms a part of receiver [3].

a) LRU Parameter Modelling

All the parameters of each LRU forms the SIMULINK input block. Each parameter will have their own input block Standard inputs from each parameter are LABEL, SDI (Source Destination Indicator), DATA and SSM (Sign status Matrix). The DATA parameter is first designed in accordance with its resolution. In this review only, left unit is used as source. Hence, the value of SDI remains 1. All the data is transmitted with respect to the specified update rate. LABEL is an octal number, DATA and SSM are decimal numbers. All the incoming data are converted to binary digits. Signal generator blocks generates the parity automatically by taking into the account all input bits. The fig 3 below shows the typical block for one parameter. In the same way blocks are designed for all the parameters. Each LRU may vary in the number of parameters.

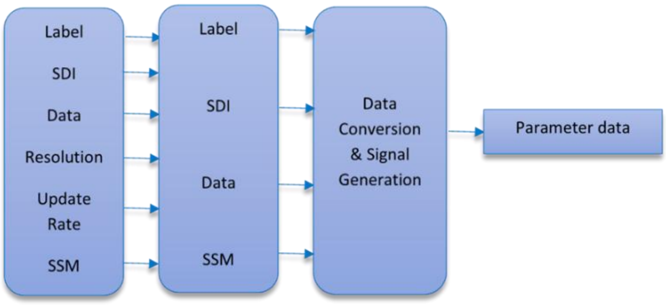

Figure 4: Parameter Model

b) Scheduler Modelling

Next step after the parameter modelling is the scheduler modelling. It mainly consists of a Look up Table (LUT), ARINC clock generator and a multiport switch. The greatest common factor (GCF or LCM) and highest common factor are computed using update rates as the inputs. Both GCF and HCF forms the dimensions of the LUT and the table data is computed by considering the parameter with respect to its update rate. GCF and HCF combination gives the information regarding the time frames of the scheduler. The table data indicates what parameters have to be sent at the given time.

ARINC clock generates the time rate which in turn indicates the speed of ARINC bus. Most of the LRUs require low speed bus i.e.,12.5kbps. In this review both high speed (100kbps) and low speed are designed, high speed simulation results are referred for further analysis. Multiport switch passes the input signals corresponding to the truncated value of the first input. The inputs are numbered top to bottom (or left to right). The first input port is the control port. The other input ports are data ports. First input to the multiport switch is the output of the LUT, that acts as the control port. The other data inputs are the outputs from each Parameter Model block.

The output of the multiport switch and ARINC clock generator are fed as the input to ARINC signal generator. Output of this is a signal in ARINC high level and low-level formats. This data consists of 32 bits.

c) ARINC Receiver

The data transmitted from the Scheduler is received by the RDC and stored for further transmitting the data to upper levels. The data from RDC goes to the AFDX switch which follows ARINC 664 protocol. Hence, it is crucial to retrieve the data in proper order. The ARINC 429 transmits the data in reverse order, expect for the Label.

Signals from all the LRUs are combined at the Scheduler, which consists of a LUT, multiport switch and ARINC clock generator. Table dimensions are provided by the computed GCD and HCF by considering the update rates of each parameter from all the LRUs.

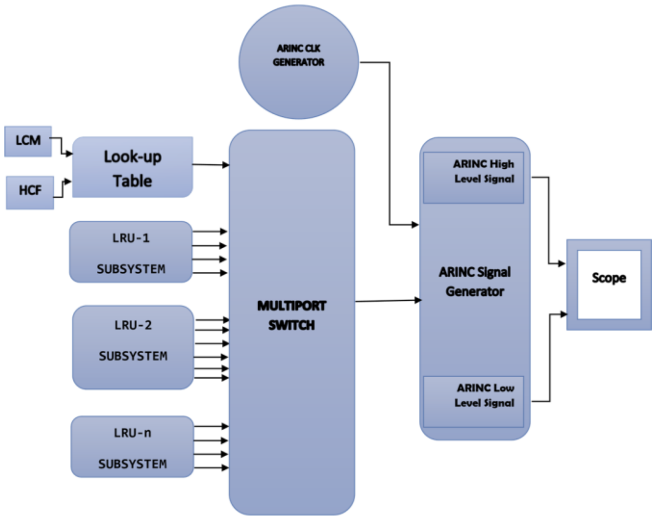

Figure 5: Scheduler Model

The received data consists of high level and low-level signals. Hence positive edge and negative edge detectors are designed to identify the signals and both signals are correlated to get a single signal. Each LRU has its corresponding receivers. Each parameter is decoded by using Label as the unique identifier. All bits are reversed except for the label and added to make it single binary signal.

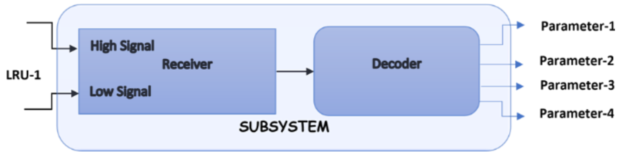

Figure 6: Receiver and Decoder

Table data is imported from the excel sheet which has the information regarding the parameter and their respective update rate. A post load function code is written so as to automatically update the table data by simply importing the excel sheet before running the simulation. LUT output is fed as the control input to the multiport switch. Each parameter of all the LRUs are given as data inputs to of the multiport switch.

Output of the multiport switch and the clock generator are fed to the ARINC signal generator which generates the ARINC signal pairs of high and low level. The whole system forms Remote data concatenator.

d) Sample Design of Scheduler at RDC

The following example helps in the better understanding of the Scheduler design. Two LRUs namely RADALT (Radio Altimeter) and ADF (Automatic Direction Finder) are considered. Critical part of the scheduler design is update rate and unique identifier for each parameter is the Label. Hence only these two are taken and a table is made as shown below:

Aim of the scheduler is send parameters according to their update rates. At zeroth time instant all the data parameters are sent. Next scheduling occurs at 0.05s wherein the parameters with update rate 0.05 are only sent. At 0.1s again parameters having update rate of 0.05s is sent.

Table 1: Typical Parameters of two LRU

RADALT	
LABEL	UPDATE RATE(s)
164	0.05
165	0.05
270	0.2
350	0.25

ADF	
LABEL	UPDATE RATE(s)
32	0.05
162	0.2
350	0.2
371	0.2

Same is repeated at 0.15s. At 0.2s parameters containing update rates of 0.05s and 0.2s are sent. At 0.25s parameters with update rate of 0.05s and 0.25s are sent. The following figure depicts the same.

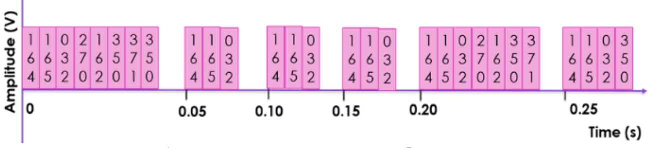

Figure 7: Data Received at RDC

6. Failure Modelling And Analysis

Failure analysis just minimizes the imperfections. Hence, it is the responsibility of the designer to think about all the possible ways the system might fail and take necessary safety precautions in handling the failure. System has to be produced in such a manner that it is fault tolerant. These analyses will help to produce a sturdy system. Also, failure analysis is an essential part of any simulation. Here in this project, 4 cases of failure analysis will be carried out.

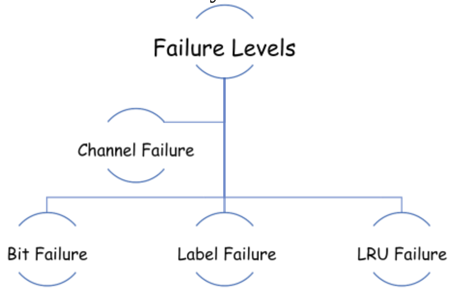

Figure 8: Levels of Failure

A) Bit Failure

Bit failure is defined as the failure in which a particular bit is transmitted incorrectly. This occurs mainly when the computed data in the ADC is flawed. In this model, this failure is simulated using bit operations on the data parameter. Manually data bit is interpreted wrong by using a switch. This failure is shown in figure 13.

B) Label Failure

Label failure occurs when a particular parameters' label is mismatched. In this case the incoming data will not be validated as Label being the unique identifier fails. In this review Label is manually forced to fail by using a switch. Here two's complement method is used. When the Label connected to the designed two's complement block; the Label is interpreted wrongly. This failure is automatically indicated by SSM. For normal operation SSM is either 00 or 11 depending on the datatype of the parameter. It switches to 11 or 00 which indicates failure warning. This is shown in Figure 12.

C) Channel Failure

Channel failure occurs when there is no data in a particular channel due to breakage of cable or channel power off, etc. One of the channels is stopped from getting data by using switches at RDC and turning them off by connecting it to zero. Figure 10 depicts this failure

D) LRU Failure

LRU failure occurs when there is a power failure or LRU is faulty. There will be no data from the LRU which has failed. In this analysis LRUs are connected to the switches and a particular LRU is made to power off by connecting the switches to zeros. There should be no data from that LRU. Figure 11 depicts the failure.

7. Simulation Outputs and Waveforms

a) ARINC 429 Transmitting and Receiving formats

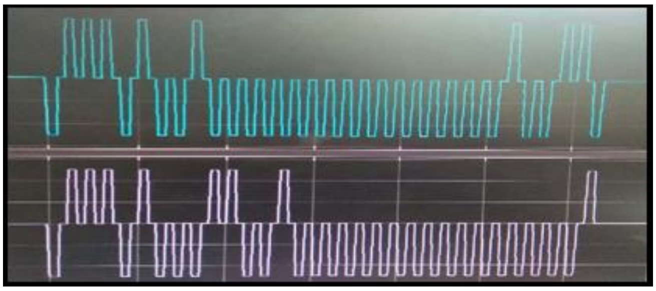

Figure 9: ARINC Transmitter and Receiver

From the above figure it can be seen that the transmission(green) is in ARINC word format and when it is received at the RDC it is received (pink) in the suitable format

b) Channel Failure

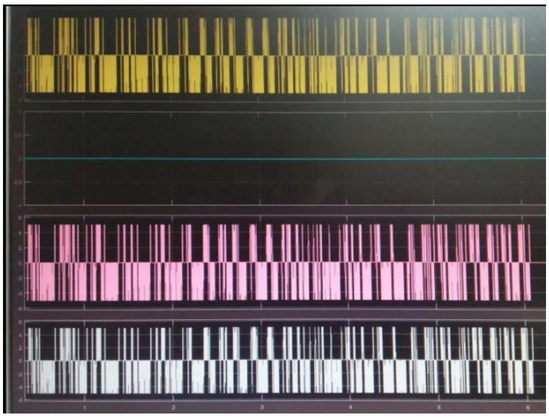

Figure 10: Channel Failure

It can be seen from the above figure that there is no data received in channel 2

c) LRU Failure

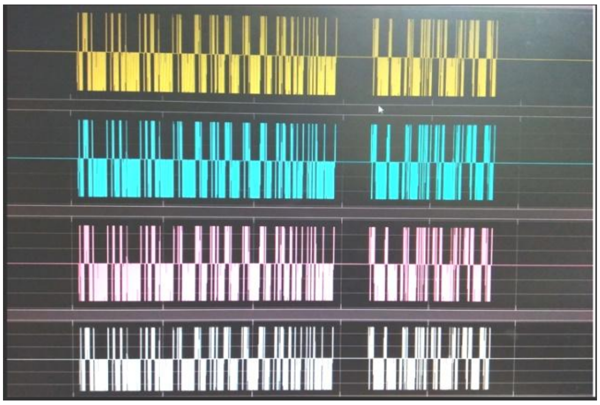

Figure 11: LRU Failure

It is evident from the figure 11, that there are some parameters missing which belongs to a particuar LRU (RADALT). This depicts the LRU failure.

d) Label Failure

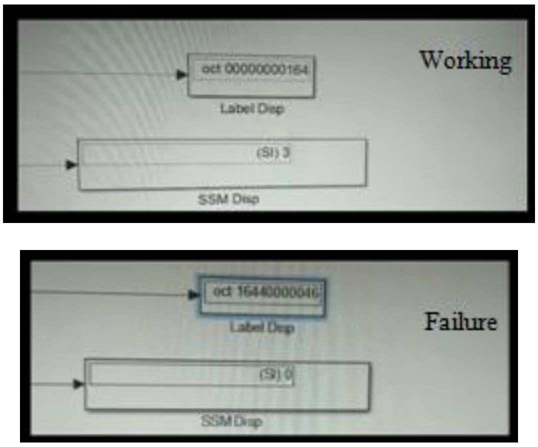

Figure 12: Label Failure

It can be seen from the figure that there is a label mismatch and so is the SSM indication

e) Bit Failure

From figure 13 and figure 14 the bit failure is indicated clearly

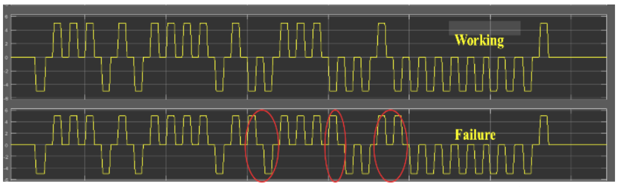

Figure 13: Bit Failure represented in waveform

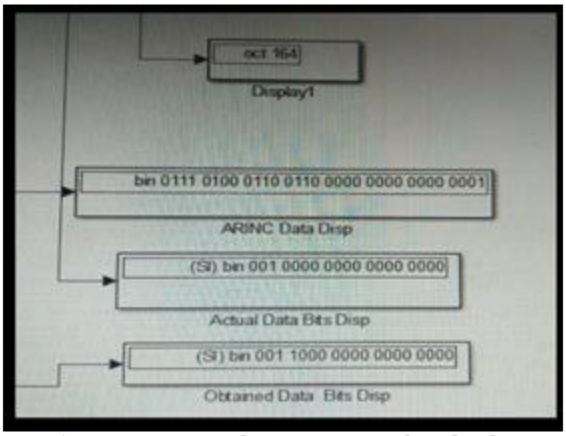

Figure 14: Bit Failure represented in display

8. Conclusion

Practitioners believe that simulation modelling and analysis is one of the operation methods used in research techniques. It gives the better understanding of the system by observation of the systems' behavior over long periods of time. It is also possible to test the feasibility, helps in identifying the bottlenecks in the functional flow. Additionally, it leads to a systematic approach to problem solving and helps in developing robust systems in a transient time.

Hence with this approach, real time symbolic Health Monitoring for Avionic LRUs are comprehended in ARINC 429 domain and transmitted which is also received at a suitable format at the RDC.

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