International Journal of Science and Research (IJSR)
ISSN: 2319-7064
ResearchGate Impact Factor (2018): 0.28 | SJIF (2018): 7.426

Low Power and Area Efficient Carry Select Adder Using D-Flip Flop

S. Muminthaj[1], S. Kayalvizhi[2], K. Sangeetha[3]

[1]PG Scholar, Government College of Technology, Electronics and Communication Engineering Department
muminthaj5930[at]gmail.com

[2]PG Scholar, Government College of Technology, Electronics and Communication Engineering Department
kayalgctcbe[at]gmail.com

[3]PG Scholar, Government College of Technology, Electronics and Communication Engineering Department
sangeethaa180596[at]gmail.com

Abstract: ***Area, Power Consumption and Delay are the constituent factors in VLSI design that limits the performance of any circuit. This work presents a simple approach to reduce the area, power consumption and delay of CSLA architecture. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. Carry Select Adder is efficient for low power application, produces the partial sum and carry by independently generating multiple carries. The proposed design has reduced area, low power consumption when compared to other adders in VLSI. The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.***

Keywords: CSLA Adder, RCA, BEC-1, D-FF, Multiplexer

1. Introduction

Area and power reduction in data path with reduced delay logic systems are the main area of research in VLSI system design. High speed addition and multiplication has always been a fundamental requirement of high performance processors and systems.

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structure becomes a very critical hardware unit. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The carry select adder is used in many computational systems to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

2. Regular Carry Select Adder

A Carry Select Adder (CSLA) is a particular way to implement an adder, which is a logic element that computes the (n+1)-bit sum of two n-bit numbers. A carry-select adder comes under the category of high speed adders to compute sum and carry. A carry- select adder is simple, but rather faster than other adders. That is generally called as "Regular CSLA".

The Regular CSLA consists of two Ripple Carry Adders (RCA's) and a Multiplexer. Adding two n-bit numbers with a carry select adder is done with two adders (therefore two RCA's). In order to perform the calculation twice, one time with the assumption of the carry being zero and other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. Carry select adder is in between delay of ripple carry adder and Area of the carry look ahead adders circuits. CSA reduces the cost and improves the performances.

Our proposed work shows the Carry Select Adder using D-Flipflop, Provides the great advantage in terms of reduced area and less power consumption when compared with Carry Select Adder using Ripple carry adders and the Carry Select Adder using Binary to Excess-1 Converter with the help of multiplexers.

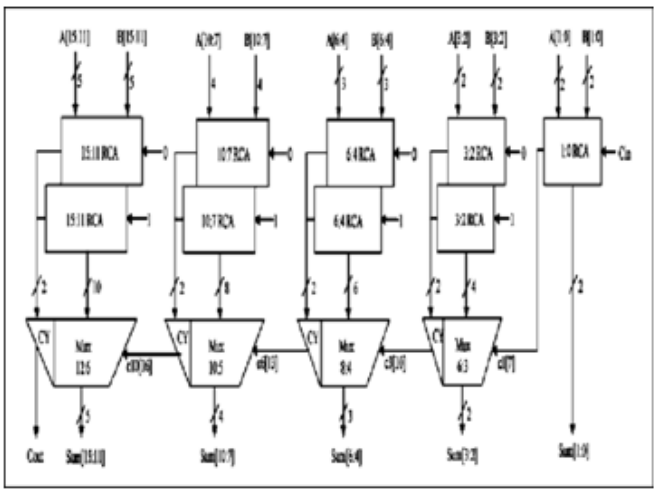

Figure 1: Regular CSLA

A 16-Bit Regular Carry Select Adder is divided into two ripple carry adder sectors (RCA's) and multiplexers. Each of which, except for the least significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one within the sector, there are two 4-bit ripples carry adders receiving the same data inputs but different Cin. The upper RCA adder has a carry in of zero, the lower RCA adder a carry- in of one. The actual Cin from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carry-out of the upper adder are selected.

If the carry-in is one, the sum and carry-out of the lower adder are selected. Logically, the result is not different if a single ripple carry adder were used. First the coding for full adder and different multiplexers of 6:3, 8:4, 10:5 and 12:6 was done. Then 2, 3, 4, 5-bit ripple carry adder was done by calling the full adder. The Regular 16-Bit CSLA was created by calling the ripple carry adders and all multiplexers based on circuit. It has five groups of different size RCA. The delay and area of each group has to be evaluated. To do this, we first need to evaluate the delay and area of each of the basic adder blocks used in the structure of the CSLA. The source code is written for all the above sadder blocks like xor gate, half adder, full adder, 2*1 multiplexer, ripple carry adder with different sizes and finally the Regular 16-Bit carry select adder is done using Verilog HDL. Simulation will be done to verify the functionality and synthesis will be done to get the NETLIST using Xilinx ISE 14.2.

2.1 Ripple carry adder (RCA)

Arithmetic operation like addition, subtraction, multiplication and division are basic operation to be implemented digital computers using basic gates among all arithmetic operations. If we can implement addition then it is easy to perform multiplication (repeated addition). Half adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple adders to N-bit binary numbers. Each full adder inputs carry which is the output of the previous adder; this kind of adder is a ripple carry adder, since each carry bits "ripples" to the next full adder. The first full adder may be replaced by the half adder, because the initial carry-in of the first full adder is zero (ie.Cin=0), so here we are replacing the full adder by the half adder.

3. Modified Carry Select Adder with bec-1

The Regular CSLA is not area efficient because it uses to pairs of Ripple Carry Adders (RCA's) to generate sum and carry by considering carry input Cin=0 and Cin=1 and then the final sum and carry are selected by the multiplexers (mux). The delay and the power consumption also higher in regular CSLA.

To overcome the above problem, the Regular CSLA is modified by using N-bit Binary to Excess-1 code converters (BEC) to improve the speed of the addition. The logic can be implemented with any type of adder to further improve the speed. We use the binary to excess-1 code converters (BEC) instead of RCA with Cin=1 in the Regular 16-Bit CSLA to achieve lower area, lower delay and lower power consumption. Hence it is known as Modified 16-Bit CSLA with BEC.

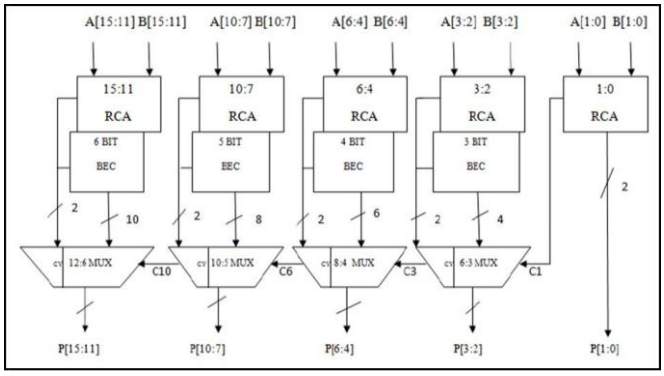

Figure 2: Modified CSLA with bec-1

3.1 Binary to Excess-1 Code Converter

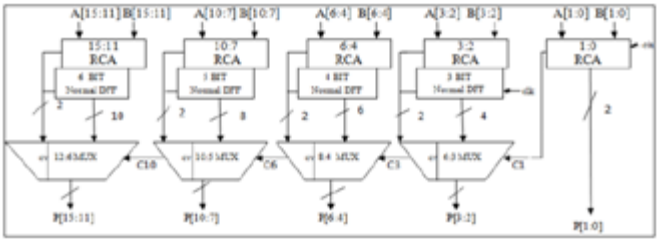

Figure 3: 5-Bit BEC

Binary to Excess-1 Converter is a digital circuit that excesses the value of the input to 1 means the value of input gets increased by 1 with the help of BEC-1. It is a digital circuit that uses 1 NOT gate, 2 AND gates and to 3 XOR gates to perform the operation. Since Regular Carry Select Adder uses multiple RCA's to perform the addition operation of input bits individually for Cin=0 and Cin=1, then BEC-1 is used to perform the addition of input bits Cin=1. So the operation of BEC-1 is same as that of the RCA with Cin=1. For Replacing N-bit RCA, N+1 bit BEC is required.

3.2 Use of Binary to Excess-1 in CSLA

The basic idea of the modified work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the Regular CSLA to achieve lower area, lower delay and lower power consumption. Practically the circuit BEC-1 is comes from the lesser number of logic gates than the n-bit full adder structure. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin.

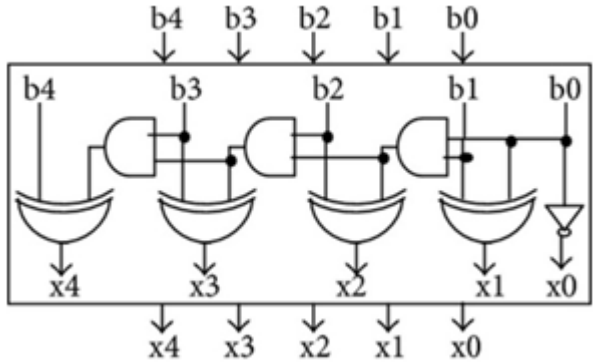

Figure 4: 4-Bit bec-1 with 8:4 Mux

If BEC input is x then Output is "X+1".

The importance of the BEC logic is from the large silicon area reduction when the CSLA with large number of bits are designed. The modified 16-bit CSLA using BEC-1 was created by calling the ripple carry adders, BEC and all multiplexers based upon the circuit. Here again the simulation and synthesis is performed using Xilinx ISE Design Suite 14.2 and the results are compared with the Regular CSLA.

4. Proposed Carry Select Adder Using D-Flipflop

When the modified CSLA using BEC-1 is simulated and synthesized, the area, delay and power consumption is less in the modified CSLA using BEC-1. So here there is a chance to reduce the power consumption further, so we can improve the above structure in terms of higher speed by replacing the BEC with a D-Flip-flop. Thus an improved Carry Select Adder with D-Flip-flop is shown below.

Here, The Binary to Excess-1 converter is replaced with a D-Flip-flop. Initially when Clk=1, the output of the RCA is fed as input to the D-Flip-flop and the output of the D- Flip-flop follows the input and given as an input to the multiplexer. When Clk=0, the last state of the D input is trapped and held in the flipflop and therefore the output from the RCA is directly given as an input to the mux without any delay. Now the mux selects the sum bit according to the input carry which is the selection bit and the inputs of the mux are the outputs obtained when Clk=1 and 0.

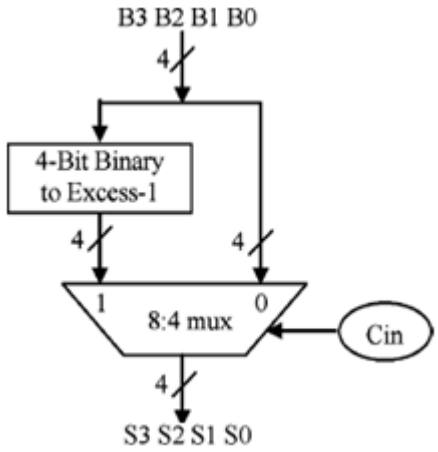

Figure 5: Carry Select Adder using D-Flipflop

4.1. D-flipflop

D-Flip-flop is an electronic device that can be used to store one bit of information. The d-flip-flop is used to capture, or "latch" the logic level which is present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the input, D is trapped and held in the flip-flop. Table: 10 show the function of D-Flip-flop Fig: 16 shows Symbol of D-Flip-flop Fig: 17 shows the logic diagram of D-Flip-flop and Fig: 18 shows the timing diagram of D-Flip-flop.

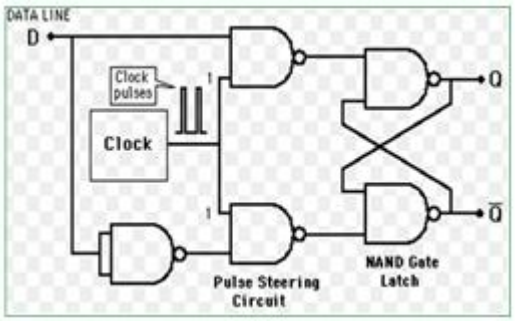

Figure 6: D-Flipflop Circuit Diagram

Here initially when Clk=1, the output of the RCA is fed as input to the D-Flip-flop and the output of the D-Flipflop follows the input and given as an input to the multiplexer. When Clk=0, the last state of the D input is trapped and held in the latch and therefore the output from the RCA is directly given as an input to the mux without any delay. Now the mux selects the sum bit according to the input carry which is the selection bit and the inputs of the mux are the outputs obtained when Clk=1and 0. Thus the improved CSLA using D-Flip-flop is implemented by writing the source code using Verilog and then performs simulation and synthesis using Xilinx ISE Design Suite 14.2 and compares the results of delay and power with Regular CSLA and Modified CSLA using BEC-1.

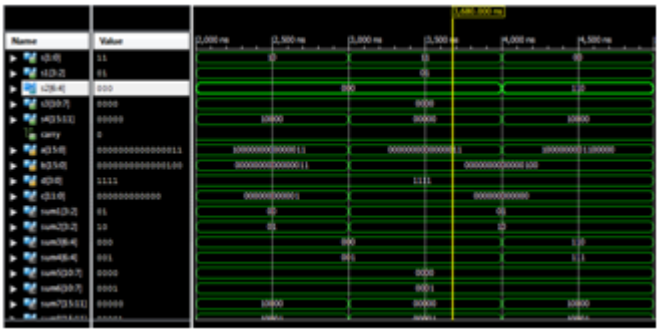

Figure 7: Waveform of Regular CSLA

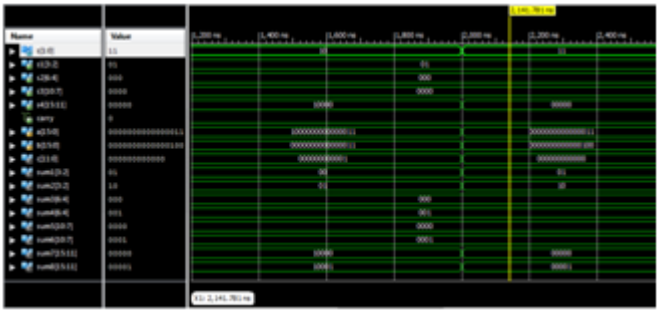

Figure 8: Waveform of Modified CSLA with BEC-1

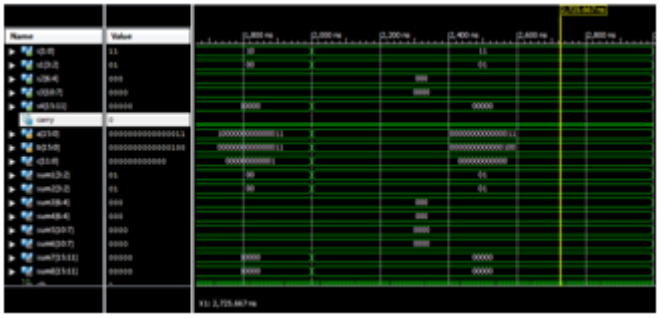

Figure 9: Waveform of Our Proposed CSLA with DFF

According to the requirement of the adder the designer has to consider all these parameter. While choosing a structure for adders what makes this decision even harder is that usually most of these parameter are not independent from each other tradeoff between desired parameter make this decision a multi- dimensional optimization problem for a non-linear system that usually has hundreds of variables, is unfortunately impossible to solve within the limited design time.

Our Proposed work shows the reduced area and less power consumption with slight increase in delay while using the Carry Select Adder using D-Flipflop when compared with other adder architecture in VLSI technology.

Table 1: Comparison Chart

ADDER	CELL AREA	POWER (nw)	DELAY (ps)
Regular CSLA	675.15	6870.66	243.40
Modified CSLA using BEC-1	554.05	6846.61	104.90
Proposed CSLA using D-FF	685.75	4920.97	147.90

5. Conclusion

In VLSI Design Technology, The power consumption, delay and area are the main factors to determine the overall performance of the circuit. The regular adder circuits consume more power compared to proposed design. This proposed work presents a simple approach to reduce the area, power consumption and delay of CSLA architecture. The conventional Carry Select Adder has the disadvantage of more power consumption and occupying more chip area and also the delay is high. All the three models of CSLA are designed and are implemented in Verilog using Xilinx ISE Design Suite 14.2 tool and the results are compared in terms of Area, Delay and Power consumption. The Improved CSLA using D-Flip-flop proves to be the High Speed and Low Power CSLA when compared to conventional CSLA.

References

[1] B. Ramkumar and H.M. Kittur, **"Low-Power and Area –Efficient Carry Select Adder,"** IEEE Trans. On VLSI Systems, Vol. No 2, pp.371-375, Feb 2012.

[2] K. Sangeetha and S. Kayalvizhi, **"Area and power Efficiency of Carry Select Adder using Gate Diffusion Input(GDI) Logic"**, Iconic Research and Engineering Journals, Volume 3, Issue 1, July 2019.

[3] O. J. Bedrij, **"Carry Select Adder,"** IRE Transactions on Electric Computers, Volume: EC-11, Issue: 3.

[4] Laxman Shanigarapu and Bhavana P. Shrivastava, **"Low-Power and high speed carry select adder,"** International Journal of Scientific and research Publications, Vol. 3, Issue 8, August 2013.

[5] D. Prasanna Kumari, R. Surya Prakash Rao, B. Vijaya Bhaskar A **" Future Technology For Enhanced Operation In Flip-Flop Oriented Circuits"** International Journal of Engineering Research and Applications, Vol. 2, Issue 4, July-August 2012, pp.2177-2180.

[6] Anitha Ponnusamy and Ramanathan Palaniappan, **"Area-Efficient Carry Select Adder Using Negative Edge Triggered D-Flip flop,"** Applied Mechanics and Materials, Vol. 573(2014) pp 187-193, June 2014.

[7] Rishikesh V.Tambat, Sonal A. Lokhatiya, **"Design of Flip-Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology",** International of current engineering and Technology, Vol.4, No.2 (April 2014).

[8] T. Y. Ceiang and M. J. Hsiao, **"Carry-select adder using single ripple carry adder,"** Electron. Lett., vol. 34, no. 22, pp. 2101–2103, Oct. 1998.

[9] Y. Kim and L.-S. Kim, **"64-bit carry-select adder with reduced area,"** Electron. Lett., vol. 37, no. 10, pp. 614–615, May 2001.

[10] Y. He, C. H. Chang, and J. Gu, **"An area efficient 64-bit square root carry-select adder for low power applications,"** in Proc. IEEE Int. Symp. Circuits Syst., 2005, vol. 4, pp. 4082–4085