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Design of Low Power 10T SRAM Cell with MTCMOS Technique

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Abstract: ***Now-a-days Power consumption (or) power dissipation has becomes the most important criteria for implementing anyone of the circuit. While calculating the efficient value of the output of that particular circuit, we may use the concept of scaling. But, while increasing the scaling process there may be a loss of leakage current. Due to the leakage current the usage of power (power dissipation) is increased. For removing these kinds of leakage currents we are going to use "power gating techniques". By using the power gating technique we can provide better power efficiency also. In this paper we are going to analyze the circuits using "MTCMOS" of power gated circuits with the help of low power VLSI design technique compare with other power gating techniques. The entire procedure may implement and simulated using Micro-wind Layout Editor & D. Sch (Digital Schematic).***

Keywords: Power gating circuits, 10T SRAM, sleep methods

1. Introduction

Static random-access memory (static RAM or SRAM) is a type of semiconductor that uses bistable latching circuitry (flip-flop) to storeeach bit. SRAM exhibits remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The SRAM from DRAM (dynamic random-access memory) which must be periodically refreshed. SRAM is faster and more expensive than DRAM; it is typically used for CPU cache while DRAM is used for a computer's main memory.
SRAM is semiconductor memory cell. It stores one bit of information. It is faster and consumes very less power as compared to other memory cells.Due to its robustness and stability, researchers are interested in further improvement of SRAM cell. SRAM is vital component in a chip or microprocessor IC. Designing a SRAM cell in Nano scale regime has become a challenging task because of reduction in noise margins and increased sensitivity to threshold voltage variation. Due to its robustness and stability, researchers are interested in further improvement of SRAM cell. SRAM is vital component in a chip or microprocessor IC. Designing a SRAM cell in Nano scale regime has become a challenging task becauseof reduction in noise margins and increased sensitivity to threshold voltage variation.

2. Related Work

Memory cell operations

Read operation:
Considering the case of reading Q=0; before reading a value from the storage nodes, the bit line BL is pre-charged to VDD. The read word line RL is then asserted to VDD. The storage node Q' that stores a 1 is statically connected to the gate of MRA (Read Access Transistor) and will drain the charges on the bit line through MRD to GND as the RL is 1, which means that the bit line has just read a 0. On the contrary, when Q=1, Q' will be 0 and MRA will be in cutoff and the bit line BL would not be able to discharge through MRD to Gnd, and it would read a 1.

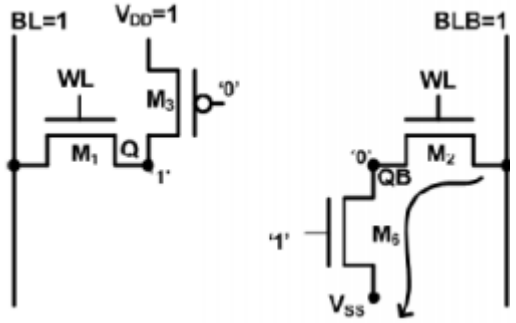

Figure 1: Memory read and write equivalent circuit

Bit lines are pre charged to supply voltage before read operation. The read operation is initiated by enabling the word-line (WL) and thereby connecting the internal nodes of the SRAM bit cell to bit-lines. The bit line voltage is pulled down by the nMOS transistor at the '0' storage node and the difference between two bit line voltages will be detected by sense amplifier. When the word line (WL) is high, one of the bit line voltages is pulled down through transistors M2 and M6 or M1 and M4. The transistors M2 and M6 forms a voltage divider, because of current flowing through M2, the potential at node QB is no longer at '0'V. Also it should not go beyond switching threshold of inverter (INV1) to avoid destructive read. The rising of potential depends on sizing of access transistor and pull down transistor which is defined as a bit cell ratio.

Write operation
The word-line WL is charged to VDD as in 6TStandard SRAM. Since NMOS is a stronger driver than PMOS, no problem is incurred while writing a 0 into the cell. The absence of the pull down NMOS for memory node Q allows writing a 1 into the cell easily. Writing a 1 is done by pre-charging bit-line BL to VDD. While writing 0, the bit-line BL is discharged and then word-line WL is charged to VDD as in 6T Standard SRAM. The write operation begins by forcing a differential voltage (VDD, and 0) at the bit line pairs (BLB and BL). This differential voltage corresponds to the data to be written at the storage nodes (Q and QB) and it is controlled by the write drivers. The WL is then

activated to store the data from the bit-line pairs to corresponding storage nodes. Assume, the nodes Q and QB store values '1' and '0' severally. Once the WL is declared the access semiconductor unit (M1) connected to BL (at '0') is turned on, a current flows from VDD to BL through M3 and money supply. This current flow lowers the potential at Q. The potential at the node Q needs to go below the trip purpose of the electrical converter (INV2) for a roaring write operation and this relies on the magnitude relation of pull-up {transistor junction semiconductor unit electronic transistor semiconductor device semiconductor unit semiconductor} (M3) and therefore the access transistor (M1). This magnitude relation is observed because the pull up- magnitude relation.

6TSRAM

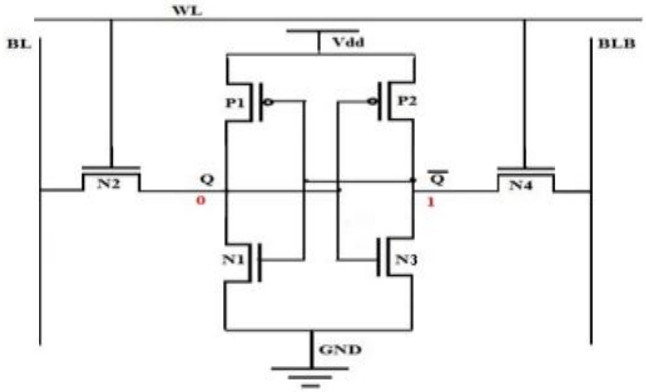

Figure 2: Schematic of the 6T SRAM

Conventional 6T SRAM cell consists of six transistors. Fig.2 shows the traditional 6T SRAM cell. Transistors N2 and N3 square measure access semiconductor unit, whereas remaining four transistors: N1, N2, P1 and P2 kind 2 inverters. These 2 inverters square measure accustomed latch information. The info enters into latching electrical converter through access semiconductor unit. The method of introducing a knowledge is thought as write operation and retrieving a knowledge is thought as scan operation. Word line (WL) selects a row of SRAM cell. Bit line (BL) and bit line bar (BLB) square measure accustomed choose a column of SRAM cell. Once each WL and BL square measure ON, a specific SRAM cell is chosen. A 10T SRAM cell may be designed by employing a typical 6T SRAM cell and a further scan electronic equipment 6T SRAM cell

DESIGN OF A 10T SRAM CELL

Schematic and Normal Operation Analysis

For the 10T memory cell, Fig.3 describes its basic schematic structure. each NMOS transistors N4 and N3 area unit outlined because the access transistors, and their gates area unit connected with thence, once this WL is in high mode (WL = 1), 2 access transistors area unit turned ON. At the instant, write/read operation are often enforced. The keep nodes area unit nodes Q, QN, S1, and S0 within which these four nodes area unit chargeable for keeping the keep price properly. So as to quickly transmit the digital signal to the output port throughout a scan operation, a differential sense electronic equipment must be used and connected with 2 bit.

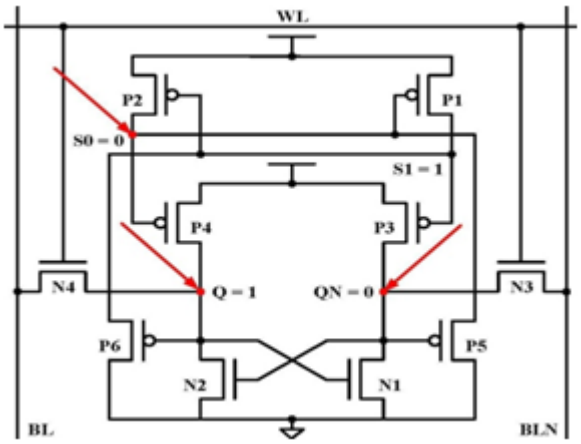

Figure 3: Schematic of the 10T SRAM

Assuming that the keep price of the 10T memory cell is 1 in digital logic, i.e., Q = 1, QN = 0, S1 = 1, and S0 = 0, as shown in Fig.3. It's simply terminated that the 10T memory cell is steady maintaining the keep price once WL is driven by an occasional voltage (WL = 0). Before traditional scan operation, because of precharge electronic equipment, the voltages of the bit lines BL and BLN are going to be raised to one in digital logic. In scan operation, WL is in high mode (WL = 1), so 2 access transistors N3 and N4 area unit turned ON right away. Nodes Q, QN, S1, and S0 area unit keeping the keep price, and therefore the voltage of bit line BL is additionally unchanged. However, the voltage of bit line BLN is attenuated because of the discharge operation through ON transistors N1 and N3. Once the voltage distinction of bit lines may be a constant price that has been confirmed within the differential sense electronic equipment connecting with 2 bit lines, the keep digital signal in memory cell are going to be output as shortly as doable. The aim of write operation is to alter the keep logical price properly. Therefore, before write operation, because of the write electronic equipment, the voltages of bit line BL are going to be zero in digital logic. Contrary to the voltage of bit line BL, the voltage of bit line BLN are going to be one. Once the voltage of WL is offer voltage VDD (WL = 1), write operation is dead. Transistors N2, P2, P3, and P6 area unit turned ON. At the instant, the states of transistors N1, P1, P4, and P5 are going to be OFF, in order that the logical price of this memory cell is justly modified to zero. Therefore, write operation can even be completed with success.

3. Proposed System

Power Gating is effective for reducing discharge power. Power gating is that the technique whereby circuit blocks that don't seem to be in use briefly turned off to cut back the discharge power of the chip. This temporary closure time can even decision as "low power mode" or "inactive mode". Once circuit blocks are needed for operation yet again they're activated to "active mode".

Power gating could be a technique employed in computer circuit style to cut back power consumption, by movement off the present to blocks of the circuit that don't seem to be in use. Additionally to reducing stand-by or discharge power, power gating has the advantage of facultative Iddq testing.

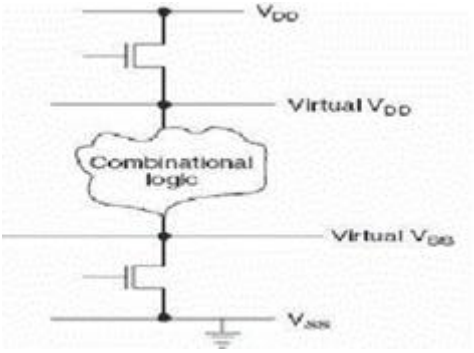

Figure 4: Power Gated Circuits

Power Gating Techniques:

The Sleepy Stack Technique (Fig.4.1) combines the Stack & Sleep techniques. The prevailing transistors divided into 2 0.5 size transistors within the Sleepy Stack technique like as Stack technique. Between the divide semiconductors one among sleep transistor are going to be extra in parallel. Stacked transistors suppress discharge current whereas saving state & Sleep transistors are turned off throughout sleep mode. In active mode it reduces delay & resistance of the trail as a result of sleep semiconductor, sleep semiconductor is placed in parallel to the one among the stacked transistors.

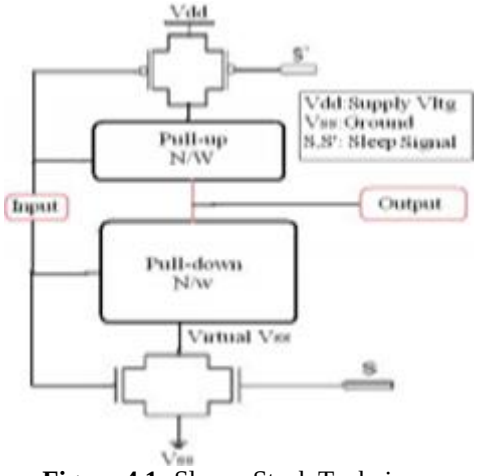

Figure 4.1: Sleepy Stack Technique

However, space demand is most for this system since each semiconductor is replaced by 3 transistors. Dual sleep Technique is (Fig.4.2) uses the advantage of exploitation the 2 further pull- up & pull-down transistors in sleep mode either in OFF/ON state.

To any or all logic electronic equipment the twin sleep portion is meant as common. For a particular logic circuit less variety of transistors are enough to use.

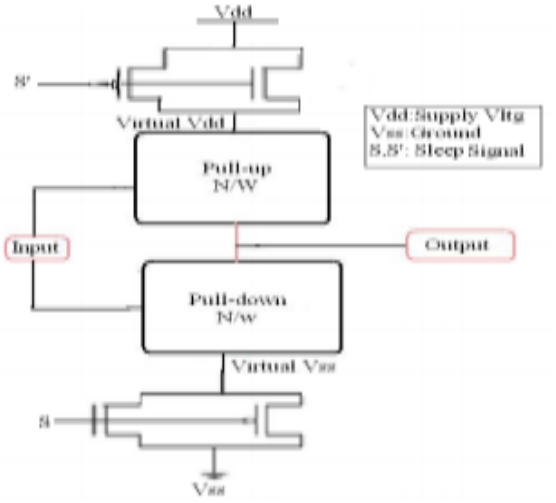

Figure 4.2: Dual Sleep Technique

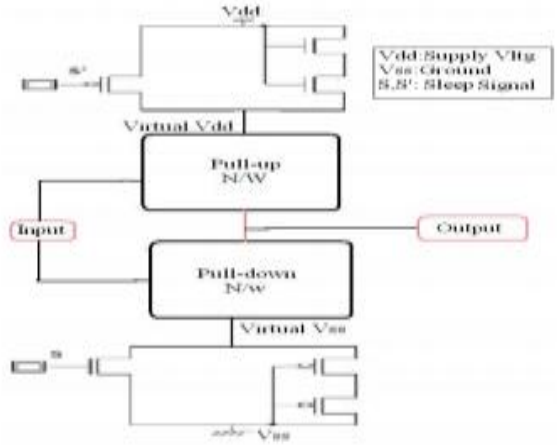

Figure 4.3: Dual stack Technique

The method is twin stack approach, in sleep mode, the sleep transistors are off, i.e. semiconductor N1 andP1 are off. We tend to do therefore by creating S=0 and thus S'=1. Currently we tend to see that the opposite four transistors P2, P3 and N2, N3 connect the most circuit with power rail. Here we tend to use a pair of PMOS within the pull down network and a couple of NMOS within the pull-up network. The advantage is that NMOS degrades the high logic level whereas PMOS degrades the low logic level. Thanks to the body result, they more decrease the voltage level. So, the pass transistors decreases the voltage applied across the most circuit. As we all know that static power is proportional to the voltage applied, with the reduced voltage the facility decreases however we tend to get the advantage of state retention. Another advantage is got throughout off mode if we tend to increase the brink voltage of N2, N3 and P2, P3. The transistors are control in reverse body bias. As a result their threshold is high. High threshold voltage causes low discharge current and thus low discharge power. If we tend to use minimum size transistors, i.e. ratio of one, we tend to once more get low discharge power thanks to low discharge current. As a results of stacking, P2 and N2 have less drain voltage. So, the DIBL result is a smaller amount for them and that they cause high barrier for discharge current. Whereas in active mode i.e. S=1 and S'=0, each the sleep transistors (N1 and P1) and also the parallel transistors (N2, N3 and

P2, P3) are on. They work as transmission gate and also the power affiliation is once more established in uncorrupted method. More they decrease the dynamic power.

4. Proposed Method

MTCMOS Operation

In the projected methodology there square measure 3 modes of operations. In Active mode (AM)

1) In Standby mode (SM)
2) Sleep to Active mode transition (SAM)

In AM, each the N2 & P2 sleep semiconductor devices stay ON & the sleep Signal (S) of the transistor is command at logic'1' (high). During this case virtual Vss node potential is force all the way down to the bottom potential, creating the logic distinction between the logic electronic equipment or so capable the Vdd (supply voltage) & each transistors supply terribly low resistance. To combining stacked sleep transistors, the magnitude of power offer fluctuations are going to be reduced as a result of these transitions square measure gradual throughout sleep mode transitions, a stacked sleep structures can do minimum escape the with a traditional threshold device, whereas typical power gating uses a sleep semiconductor device that may be a high- threshold device to reduce escape. In SM, each the T3 & T4 sleep semiconductor devices stay ON & the sleep Signal of the transistor is command at logic'1' (high) & management transistors P2 & N2 is OFF by giving logic'0, during this case virtual Vss node potential is force all the way down to the bottom potential, creating the logic distinction between the logic electronic equipment or so capable the Vdd (supply voltage) & each transistors supply terribly low resistance By exploitation of the stacking impact we are able to reduces the escape current, turning each sleep transistors OFF(T3 & T4) and vice-versa for the header switch. In SAM, the analyzed style provides major contribution in terms of peak of SM compared to stacking PG. once Sleep mode occurred, the circuit goes from sleep to active or active to sleep. In initial stage, by turning on the management {transistor junction semiconductor device electronic transistor semiconductor device semiconductor unit semiconductor} M1 (which is connected across the drain AND circuit of the T3) then the sleep transistor (T3) is functioning as a diode. Thanks to this Ids of the sleep semiconductor device T3 drops in a very quadratic manner. This reduces the circuit wake-up time, voltage fluctuation on the ability web & ground. So in SAM, at first when tiny period of your time we tend to square measure turning ON semiconductor device T3, to scale back the bottom Bounce Noise T4 are going to be turned ON. In next stage management {transistor junction semiconductor device electronic transistor semiconductor device semiconductor unit semiconductor} is off that sleep transistor works commonly. Throughout sleep to active mode transition, semiconductor device T3 & T4 (after tiny low period of time) is turned ON. The logic circuit isolated from the bottom for a brief period because the semiconductor device T4 is turned OFF. Throughout this period, the semiconductor device T4 is operated in thermionic tube region, by dominant the intermediate node voltage we are able to cut back the bottom Bounce Noise & Inserting correct quantity of delay (delay < discharging time of the T3transistor). By turning each T3 andT4 sleep transistors OFF, the escape current is reduced by the stacking impact. Thanks to tiny Id (drain current) it raises the intermediate node voltage VGND2 to +ve values.

5. Results

The Below Figure shows the Schematic of 10TSRAM.

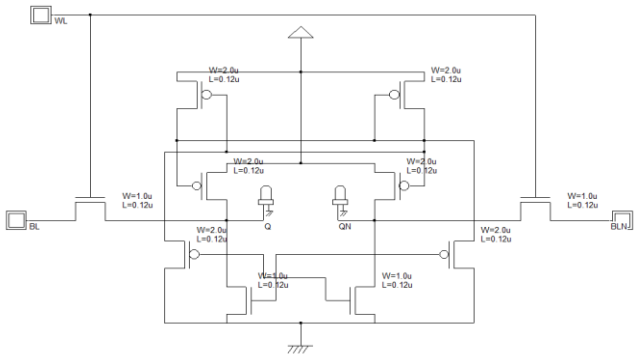

Figure 5.1: Schematic of 10TSRAM

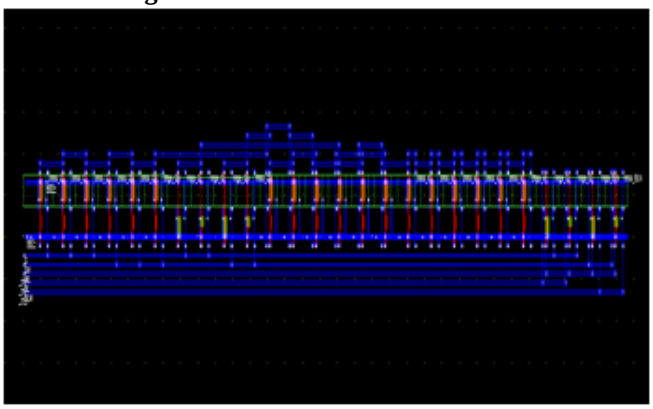

Figure 5.2: Layout of 10TSRAM

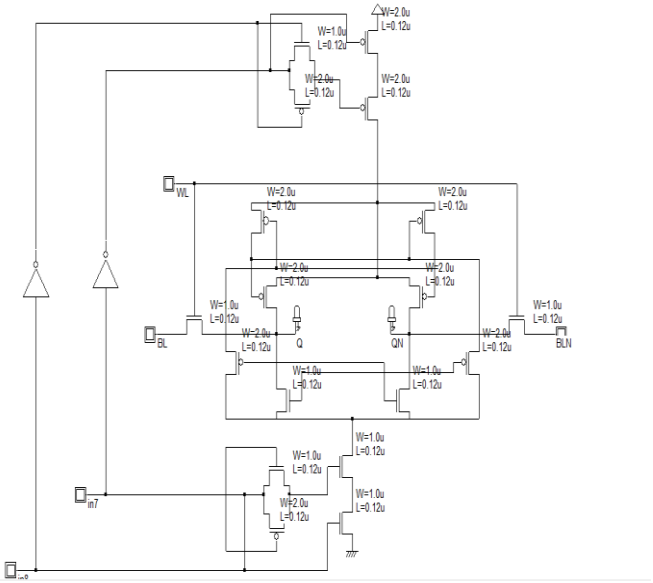

Figure 5.3: Schematic of MTCMOS

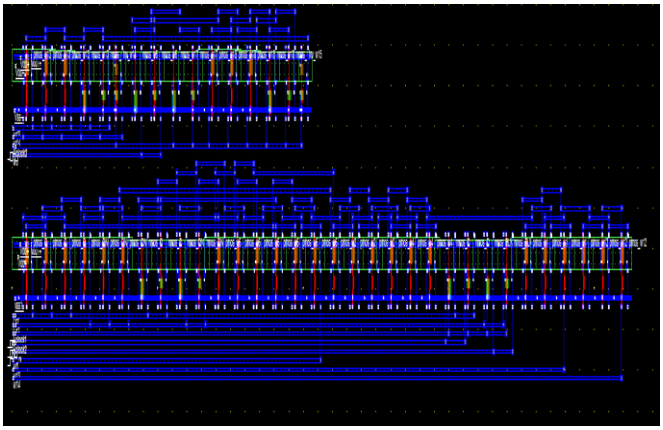

Figure 5.4: Layout of MTCMOS

Table 1: Comparison with Existing /Proposed System

Parameters	Existing System		Proposed System	
	10T SRAM		MTCMOS	
	PMOS	NMOS	PMOS	NMOS
No.of Transistors	6	4	9	8
Capacitance(fF)	1.75	1.86	0.1	0.05
Metal Capacitance(fF)	1.69	0.46	0.08	0.04
Inductance	0.02nH	0.04nH	0nH	0nH
Time Parameters				
tpHL(ps)	2007		4000	
tpLH(ps)	2006		2000	
Delay time(ps)	2006.5		2500	
Geometrical Parameters				
Width(um)	13.7um		53.3um	
Height(um)	3.5um		11.5um	
Surface Area(um^2)	47.8um2		609.7um2	
Technology				
Nanometer	45nm		45nm	
Metal Usage	8 Metal		8 Metal	

6. Conclusion

In nanometer scale CMOS 45nm technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named "MTCMOS" as a new remedy for designer in terms of static power and dynamic powers. The MTCMOS approach shows the least speed power product. If we implement this power gating technique to other reaming circuits, we may identify the drastic decrease in power consumption. It may be the great advantage of power gating technique.

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