International Journal of Science and Research (IJSR)
ISSN: 2319-7064
Index Copernicus Value (2016): 79.57 | Impact Factor (2017): 7.296

Regulated Power Gating Technique for PVT Variation-Tolerant SRAM in Data Retention Mode

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Abstract: ***Power gating technique is one of the most popular leakage power reduction solutions in sub-micrometer SRAM design in data retention mode. As technology scales down more, the stored data has suffered from process, voltage, temperature (PVT) variations more seriously in guaranteeing a reliable data without data loss. In this paper, PVT variation aware noise mitigation circuit is proposed to keep SRAM supply voltage stable to vulnerable noise during retention mode. Regulated power gating technique proved the ability of variation tolerant SRAM compared to the Conventional Diode Clamp Power Gating and the Dual Diode Clamp Power Gating which have often used to save SRAM power consumption in retention mode. The regulated power gating technique shows SRAM cell bias fluctuation is very little change, just 12.4 mV compared to 351.1 mV and 379.4mV in two other schemes. Simulation results are analyzed in impact of voltage, temperature and process variation as well as process corners in 45nm Predictive Transistor Model. Leakage power consumption is also considered in this comparison. The overhead area of the regulator is not considerable compared to the SRAM area.***

Keywords: Power Gating, SRAM Cell, retention mode, cell bias, variation, Diode Clamp Power Gating..

1. Introduction

Low power SRAM has become a critical issue of chip design together with reliable data storage. Especially, microprocessors including on-chip cache memory often require to be increased in size at each generation in terms of speed of processor and main memory. Here, total power of system on chip is dominated by SRAM cells. It is because more than 60% of Strong ARM and 30% of Alpha 2126 are devoted to cache and memory structure [1]. This is reason that power dissipation has become an important concern, including both higher SRAM cell density and explosive growth of battery operated appliances. In the development of technology, microprocessor designs occupy a large area portion of memory structure such as multiple levels of instruction, data caches, translation look-aside buffer, prediction table, lookup tables. Caches are a dominant component of leakage energy dissipation in the recent designs. Leakage energy accounts for 30% of L1 cache energy and up to 80% of L2 cache energy [1-2]. Thus, conserving energy has raised considerable concerns in SRAM design. Reducing operating voltage is often used to reduce SRAM power consumption. By applying a small voltage difference among two rails, power consumption will be decreased significantly. Here, power consumption generally includes dynamic and static power consumptions caused by switching activities and leakage current, respectively. The dynamic and static power consumptions are respectively characterized by quadratic and exponential dependency on the supply voltage. However, yield is degraded which is highly vulnerable to process variation under a low operating voltage. Thus, many different leakage reduction techniques have been proposed at both circuit and process technology level. At the circuit level, various leakage reduction techniques have been published such as transistor stacking, reverse body biasing, dual threshold CMOS and power gating [3]. Among above techniques, power gating is the most popular leakage reduction technique. Power gating uses sleep transistors by inserting them between power supply rail and ground rail. When the circuit is in sleep mode, the sleep transistors are turned off, cutting pull-up and pull down network off from one or both power rails [3]. Thus, leakage current is suppressed. When the circuit is in active mode, sleep transistors are turned on, reconnecting the pull up and pull down networks to power rails. The similar power gating techniques consist of multi-threshold CMOS, booted-gate CMOS, super cutoff CMOS, variable threshold CMOS, and zigzag super cut-off CMOS [3-4]. However, power gating can cause power/ground bouncing noise during the transition from active to sleep mode and vice versa. More seriously, scaling technology lowers supply voltage level to 1V in 45nm Technology [5]. It makes noise become a serious threat to system reliability. Many researchers published the techniques to mitigate power gating noise which can affect the stored data in SARM [6]. Furthermore, technology scaling can affect the interconnection metal wire dimension, dielectric thickness, sleep transistor dimensions, MOSFET doping concentration. These variations can result in deviation from nominal values for electrical parameters such as threshold voltage, sheet resistance, parasitic induction and capacitance [7-8]. These variations including the manufacturing process, operation temperature, supply voltage is able to become more serious in shrinking technology. Recently, hardware-software collaboration is designed to guarantee certainly the stored data in these variations [9]. Besides, researchers published technique of inserting decoupling capacitance, power gating optimization, system level protection based resilience design for improving these variation fluctuations [9].

To reduce more and more leakage current, we often lower down voltage swing as much as possible in retention mode. Thus, improved power efficiency can be achieved by reducing the supply voltage. Often, we down voltage swing SRAM to voltage level where SRAM can achieve data at logic output 1 or 0 reliably. While we try to save power loss as much as possible in retention mode, the variation noise can be a big problem affecting retained data. The amount of power saving gets trade-off with robust again noise. To make a minor noise effect on SRAM cells, a voltage swing must be kept at a stable voltage level. By doing so, even much noise

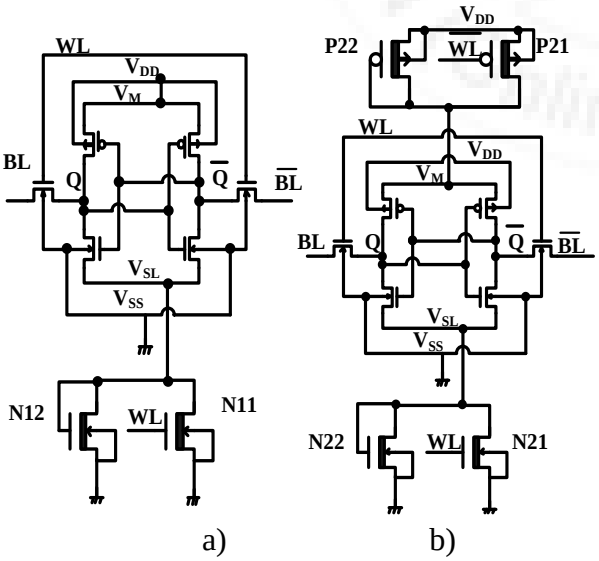
environment is also mitigated by this proposed regulation circuit. As noise can be cancelled out, voltage swing can be remained at a stable voltage level. Thus, data can be reliable even in noisy environment.

In this paper, we propose regulated power gating technique for variation-tolerant SRAMs. The proposed circuit can retain reliable data for SRAM cell by keeping two voltage rails against PVT variations in retention mode of SRAM cells.

2. Proposed Regulated Power Gating Circuit

The SRAM consumption current reduction is very important in retention mode. Reason is that memory consumes very large energy. By using the power gating technique together with NMOS connected diode or PMOS connected diode, the leakage can be decreased very much and data can also be retained without loss [10]. Here, NMOS and PMOS with dark bar are used with high threshold voltage to save power consumption [10].

Fig. 1 shows three schemes for power gating techniques. Fig. 1.a) illustrates conventional diode clamp power gating where a single NMOS switch, N11, is used to power off the circuit ground line by word line (WL) signal. In retention mode, the WL signal is "0" logic. At this moment, NMOS, N11 is turned OFF. The gate terminal of NMOS, N12, connected to the drain terminal, the N12 operates like a connected-NMOS diode. The voltage of V_{SL} node will be charged up to the threshold voltage of this connected NMOS diode which increases the voltage difference between V_{DD} and V_{SS} to V_{DD}-V_{th}. In normal mode, V_{SL} is equal to V_{SS}. Thus, SRAM is operated with full V_{DD}. In retention mode, the V_{SL} node is greater than V_{SS} approaching to V_{th} (N12). Thus, cell bias of SRAM is $V_{DD} - V_{th}$ (N12) in retention mode. Here, cell bias is defined by voltage difference between two power sources which supply to SRAM cells.



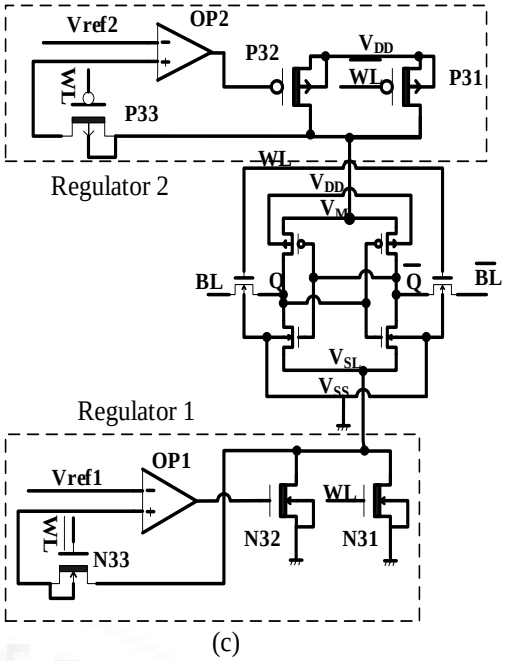


Figure 1: Three schemes of power gating technique a) The Conventional Diode Clamp Power gating (The Conventional DCPG). b) Dual Diode Clamp Power gating (Dual DCPG). c) Regulated power gating (Regulated PG).

Fig. 1.b) shows the technique of the Dual Diode Clamp Power Gating (Dual DCPG). Here, the WL and $\overline{WL}$ signal switch off NMOS of N21 and PMOS of P21. Similarly, we both increase V_{SL} decrease voltage V_M to reduce voltage swing between two power rails. Thus, cell bias is achieved $V_{DD} - V_{th}$(N22) – V_{th}(P22). Here, we optimize the width of NMOS, N21, is twice larger than NMOS, N11, of the conventional DCPG. The width of PMOS, P21, of the dual DCPG is twice larger than that of the NMOS, N21, of the dual DCPG. By doing so, we make a fair comparison in active mode [3]. The width of NMOS connected diode and PMOS connected diode achieves the smallest width to save area overhead and power loss.

In two above circuits, cell bias fluctuation is a function depending on voltage supply and threshold voltage. SRAM performance is significantly degraded according to threshold voltage variation. This is because the threshold voltage affects ON current of the transistor. The threshold voltage is also a function of temperature and process parameters [7]. Thus, change of voltage and temperature causes the threshold voltage variability. These parameters affect stable data for SRAM cell in retention mode.

Fig. 1.c) shows the proposed scheme of Regulated Power Gating. We examine the operation of active mode and retention mode of the proposed technique. In active mode, both N33 NMOS and P33 PMOS are turned OFF as WL signal is logic "1". Simultaneously, N31 NMOS and P31 PMOS transistor switches are turned ON. So that, the V_M and V_{SL} signal are corresponded to V_{DD} and V_{SS} to make a full V_{DD} voltage swing of SRAM Cell in normal operation surely. In retention mode, both N33 NMOS and P33 PMOS are turned ON as WL signal is applied to logic 0. Two circuits of regulator1 and regulator2 start their comparison function.

Here, two circuits are designed to automatically maintain a constant voltage level of VSL and VM node. The V_{SL} is stable at reference voltage, Vref1, by the regulator1. The VM is kept at reference voltage, Vref2, by regulator2. Here, if voltage fluctuation occurs to V_{SL} node or VM mode, the comparators using OPAM OP1, OP2 will regulate the voltage of V_{SL} node to Vref1 and VM node to Vref2 by feedback control loop. If V_{SL} node rises up to larger voltage than Vref1, comparator turns ON N32 NMOS to draw down V_{SL} signal to Vref1. Otherwise, if VSL node is smaller than Vref1, the comparator turns OFF N32 NMOS to charge VSL node up to Vref1. Similarly, if VM node discharges to lower voltage than Vref2, the comparator, OP2, turns on P32 PMOS to rise up VM signal to Vref2. Otherwise, if VM node is larger than Vref2, the comparator, OP2, turns OFF P32 PMOS to discharge VM node to Vref2. Sequentially, the V_{SL} node will be kept at a stable voltage of Vref1 while VM node is maintained at Vref2. Then, cell bias is achieved by Vref2-Vref1.

3. Simulation Results

We simulate 10 SRAM cells in 45 nm PTM [11]. The simulation compares three above circuit schemes in terms of cell bias variation and leakage current. The retention time is 10µs with small active time in simulations.

The Fig. *2* shows SRAM cell bias at various supply voltages of 0.8V, 0.9V, 1V, 1.1V, 1.2V, 1.3V at 27°C. When supply voltage increases, the cell bias of the Conventional DCPG and the Dual DCPG also increases. At a specific voltage supply, the cell bias is achieved in each scheme. As seen in fig. 2, the cell bias of conventional DCPG and Dual DCPG is not stable according to voltage variation. It means the supply voltage variation causes cell bias fluctuation very much. Thus, static noise margin of SRAM cell is affected deeply by supply voltage change. The data can be lost easily in retention mode if high supply voltage variation happens frequently. The highest cell bias variation is 351.1mV and 379mV for conventional DCPG and Dual DCPG, respectively according to voltage change. It means both conventional DCPG and Dual DCPG suffer from noise tolerance very badly. It means that the two conventional schemes are able to deal with noise not well. In case of Regulated Power Gating, the cell bias is very stable. The cell bias inconstancy is about 12.4mV. It means the cell bias is affected just slightly by supply voltage variation in the proposed power gating. If supply voltage variation occurs to three schemes, the proposed power gating has smaller cell bias change than two other schemes. It proves the proposed circuit is robust against supply voltage variation noise.

As technology scales down, the supply voltage level reduces continuously [2]. At a certain technology node, the reducing supply voltage is also necessary to lower power consumption. Similarly, the near-threshold supply voltage is often used in ultra low power consumption applications [12]. Regardless of changing supply voltage due to scaling or PVT variation, the regulator circuit can be kept intensively at a certain voltage level to mitigate supply voltage change effectively. Here, two reference voltages are applied to OPAMs, OP1 and OP2 which play a role as a comparator with a voltage level of V_{SL} and V_M.

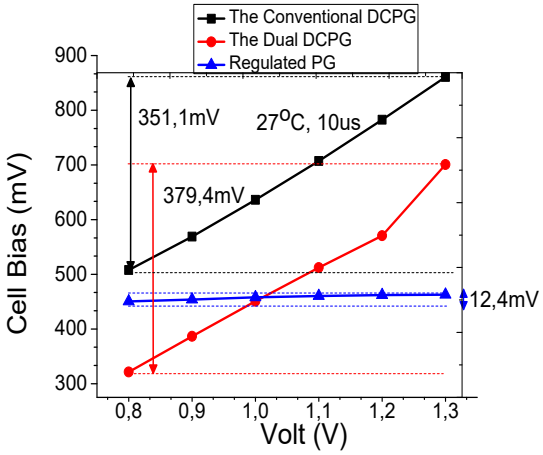


Figure 2: Various supply voltages affect cell bias.

To analyze the impact of the temperature variation to cell bias voltage, we simulate three circuits at different temperatures of 100°C, 0°C, 27°C and 100°C, with supply voltage at 1.2V. Fig. 3 illustrates the cell bias voltage still gets a fluctuation in the conventional DCPG and dual DCPG. In case of the regulated power gating circuit, the cell bias fluctuation almost does not change. The regulated PG still keeps a voltage stable regardless of temperature variation.

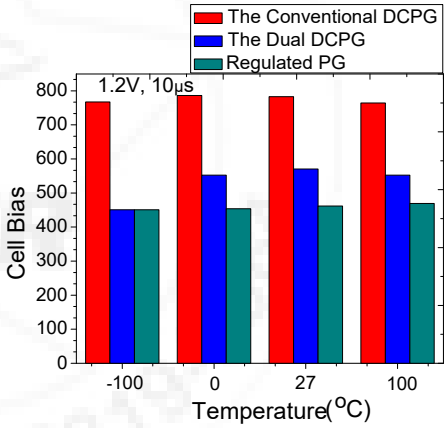


Figure 3: Temperature variation affects cell bias voltage at 1.2 V supply voltage, 10µs retention time.

Threshold voltage variation can be identified by 1) locality variability due to the randomness in number of dopants in the depletion region of MOSFET 2) global variability due to manufacturing fluctuations in the gate length, gate oxide thickness, implant impurity [5]. The modern deep submicron circuits are more prone to fail due to threshold variation. Table 1 shows the threshold variation impacts to cell bias voltage. The effects of fluctuation in MOSFET threshold voltage are investigated in the simulation. Here, the threshold voltage variation is added from ±0.05V to ±0.1V into the nominal value to analyze effects of low threshold NMOS (nfet), low threshold PMOS (pfet), high threshold NMOS (nfet_hv), and high threshold PMOS (pfet_hv). The simulation results indicate that cell bias fluctuation on the Regulated PG is smaller than the conventional DCPG and Dual DCPG. The proposed power gating has cell bias mean of amplitude change around 461.8mV, deviation of 20mV. In

the conventional DCPG and Dual DCPG, cell bias deviation is about 60mV and 153mV, respectively.

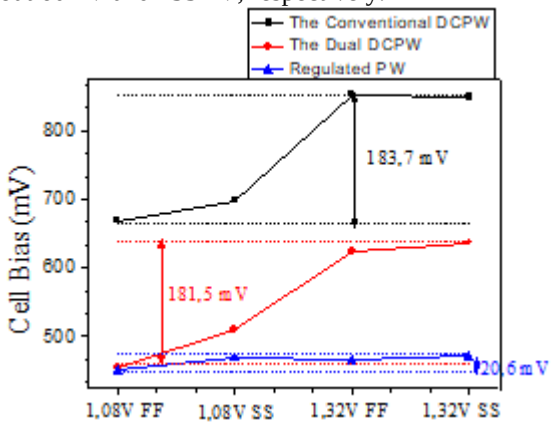


Figure 4: Different process corners for analyzing cell bias voltages.

Table 1: Threshold Voltage Variation To Cell Bias Deviation

Threshold voltage (V)	Cell bias (V)		
	Con. DCPG	Dual DCPG	Regulated PW
nfet =0.46893 pfet = - 0.49158 nfet_hv =0.62261 pfet_hv = - 0.587	782,7	570,7	461,8
nfet = 0.51893 pfet = - 0.54158 nfet_hv = 0.67261 pfet_hv = -0.637	761,4	516,1	450,8
nfet = 0.41893 pfet = - 0.44158 nfet_hv = 0.57261 pfet_hv = -0.537	786,4	588,2	471,2
nfet =0.36893 pfet = - 0.39158 nfet_hv = 0.52261 pfet_hv = - 0.487	777,3	587,1	471,5
nfet = 0.56893 pfet = - 0.59158 nfet_hv = 0.72261 pfet_hv = -0. 687	728	434,9	450,7

The process corner is analyzed to run devices at different aspects. The process corner of the circuit may run slower or faster at a lower or higher temperature and voltage. If the circuit does not function at all parameters, the design is considered to have inadequate design margin. This helps verify the chip design robustness to accommodate process variations. The purpose of process corner is to help you find out whether your design will immune to process variation in the future. We use two-letter designation to describe different corners where the first letter refers to the NMOS device and the second refers to the PMOS device. For example, FF means faster speed for NMOS and fast speed for PMOS, high temperature and increased threshold voltage. Basically, there are 5 classic corners, including FF (fast fast), SF (slow fast), SS (slow slow), FS (fast slow), and TT (typical typical). SS means slow speed NMOS and slow speed PMOS, low temperature, decreased threshold voltage. Then, various supply voltages from 1.08V to 1.32V are used in these results. Additionally, FF process corner increases threshold voltage to 0,1V, temperature to 86^{o}C while SS process corner decreases threshold voltage to 0.1V, temperature to 27 ^{o}C. The fig. 4 shows the cell bias variation is 20.6 mV, 181.5 mv and 183.7 mV corresponding to The conventional DCPW, the Dual DCPW and Regulated PW, respectively. The propose power gating is smaller cell bias fluctuation than two other schemes.

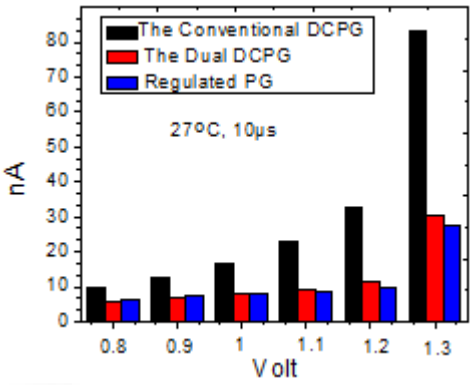


Figure 5: Impact of supply voltage to leakage current at 10µs sleep time and 27^{o}C.

As above results, we continue to consider the power efficiency in the proposed technique. Fig. 5 illustrates the impact of the supply voltage to leakage current at the 10µs sleep time and 27^{o}C. At various supply voltages, leakage current also achieves different amount of power consumption. The leakage current of conventional DCPG is the highest. At 0.8V supply voltage, the leakage current of Conventional DCPG is 9.941nA. The leakage current of the conventional DCPG is 12.67 nA, 16.79nA, 22.98nA, 32.78nA, 83.19nA corresponding to 0.9V, 1V, 1.1V, 1.2V and 1.3V, respectively. At 0.8V, the leakage power of the regulated PW is slightly larger than the Dual DCPG. This is because the proposed circuit needs an extra circuit to create the signal control and regulated circuit. The circuit overhead is occupied in the proposed circuit, making a small amount of extra leakage current dissipation. Here overhead area of two regulators consisting of OP1 OPAM, OP2 OPAM, N33 NMOS and P33 PMOS is not considerable compared to the SRAM area because they can be shared to all SRAM cells in memory. At 1.3 V high supply voltage, for example, the proposed technique shows the lowest leakage power consumption compared the two other schemes. The Dual DCPG gets body effect at both header and footer of the SRAM cell. Thus, the Dual DCPG is lower than the conventional DCPG in term of leakage current.

4. Conclusion

The Process (P), Voltage (V), temperature (T) variations in SRAM impact yield, cell size, bit density, swing voltage. In this paper, we proposed variation tolerant circuit in the SRAM cell in retention mode. The Regulated Power Gating can alleviate these impacts. The cell bias fluctuation of the proposed technique is the smallest compared with that of Conventional DCPG, and Dual DCPG. We evaluated the results based on the change of voltage, temperature and process to make the conclusion. The regulated power gating circuit shows more leakage power saving than the two other schemes.

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