International Journal of Science and Research (IJSR)
ISSN: 2319-7064
Index Copernicus Value (2016): 79.57 | Impact Factor (2017): 7.296

Simulation, Analysis and Implementation of 7 level Cascaded H Bridge MultiLevel Inverter

Aakash Suthar[1], Dr. Pramod S. Modi[2]

[1]Student of M S University, Electrical Engineering Department, M S University of Baroda

[2]Associate Professor, Electrical Engineering Department, M S University of Baroda

Abstract: ***This paper a contrivance of inverter of cascaded type is presented in which the number of switches needed is lowered compared to usual used inverters. In this paper, concept which discussed are THD and low dv/dt for multilevel converters . This topology is also work on high power quality and lower harmonic components. And also better work for electromagnetic consistence and low dv/dt as well as lower switching losses. This Theory also presented different voltage source in generating all voltage levels as positive or negative is verified by using the MATLAB/SIMULINK results of a 7,13 &19 -level 1-phase &3-phase inverter. This paper main focused on T.H.D, dv/dt losses, single phase and three phase 7 level, 13 level, 19 level inverter***

1. Introduction

This paper presents as recent research in applications of cascaded multilevel converters. Cascade multi level inverter are given are a very interesting solution in power distribution systems and also renewable energy D.C sources.

Multilevel inverter or rectifier are more finding considerable attention in academia and industry as one of the preferred for high power conversion applications, such as traction drives, active filters, reactive power compensators, photovoltaic power conversion, uninterruptible power supplies, static compensators and flexible AC transmission systems. In point of view, there are different three multilevel converter topologies. In this paper some of them which are following first is Diode-Clamped Multilevel Converter which is based on the neutral-point-clamper inverter topology introduced, second Capacitor-Clamped Multilevel Converter also known as flying capacitor or multi cell converter and third one is Cascaded multi cell Converter which is Cascaded H-bridge Multilevel Converter .

The disadvantage shown in diode clamped multilevel inverter topology is that it does not use high power range. if it use it require more high power diode for operations in the high power range. Second one is In flying capacitor method is required more flying capacitor if their method to be considered. The first topology introduced is the series H-bridge obtained by connected two different D.C source. This topology consists different series D.C source power conversion as cells . this d.c cell solve inform the cascaded H- bridge multilevel inverter .The power level in D.C series will be calculate easily with different equations. This topology has some disadvantage which is large number of isolated D.C voltage is required to supply each cell and also needed separately for pulse isolation. This topology has high number of step voltage multilevel inverter with lower number switches has a high number steps of power. This topology is generating all level odd and even output wave. The calculation for output voltage is very easy. In this topology also more benefit as compare Pulse with modulation technique.

Multi level inverter more useful for in medium level industry as power control, speed control, and other application. It's also for power distribution ,power controlling and power quality. It is important switching device such as IGBT and MOSFET to produce high level output. By Using that concept, the power conversion is performed in small voltage

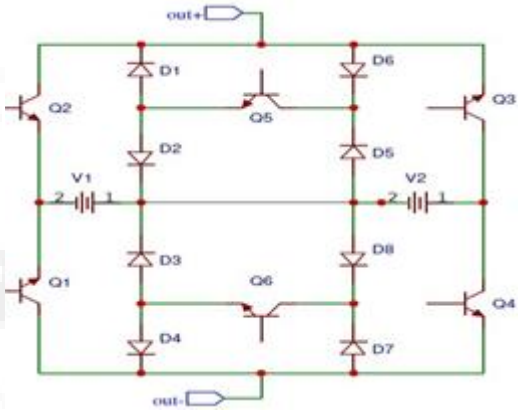


Figure 1: Two cascade 7 level block diagram

steps, resulting in better power and high-voltage applications due to produce stepped output voltage waveform and negligible harmonic content . So it attain higher voltages with a limited switch device rating. Basically, the harmonic content in output waveform decreases significantly with the number of inverter levels increases**.**

2. Cascade Topology

Cascade topology are efficient in HV with high capability and has low switching losses

Types of Cascade Topology

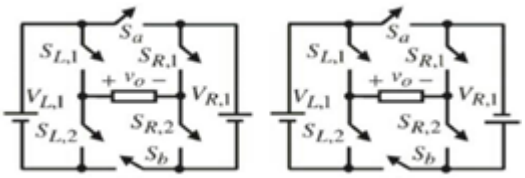


Figure 2: Power diagram of 7 level inverter bridge

2.1.1 First method

In this method, all of DC voltage sources in this method are same as Vdc, so inverter is known as symmetrical multi level inverter. The maximum output voltage is obtained by in this method as steps by N step = p+1 .The ‘‘maximum” word is used because of that it will be possible create value for all different states of the switches. The maximum Vo max output voltage presented by

Vo max=p*V DC

2.1.2 Second Method Concept of Cascade Theory

Basically concept of cascade theory is introduced by two H bridge 7 level inverter as shown in figure 2.This topology needed two d.c source such as renewable source or capacitor and connected it on input side and also there are already available AC voltage which will be converted in DC sources by generated using isolated transformers and rectifiers. Generally structure of cascaded multilevel inverter for single phase consists with two DC voltage sources. If voltage source Vs1 and Vs2 is connected in cascade with other source. All H-bridge consists of four active switching elements as igbt. So to get positive, negative or zero level by using switching sequence. Basically, multilevel power inverter topology employs multiple voltage of equal or double magnitudes.

If number of sources are p in H bridge
Numbers of output level N=2
If p= 3 the output wave form has 7 level (3,2,1,0,-1,-2,-3);
The number switching stage can be calculated by this way,
Vn=Vdc(n=1,2,3…)
Nstep=4p

2.1.3 Third Method

Third method is use as multiplier in input of d.c voltage such shown below,
Va= a*V DC where a is multiplier(a = 1,2,3.. n)
V q = 2 V DC For q=1,2,3……
The maximum output voltage steps can be determined by this equation: N step= 2p

3. 7-Level Inverter Topology

Construction of 7 level inverter same as 5th and 3thlevel inverter. The difference here is only pulse signal and switching device. Here we are taking six carrier signals for seven level.there are six pulse three of them positive half cycle other of them for negative half negative half cycle

Pulse Generation Analysis

Other view for total cost of inverter by using numbers of switch required. Therefore, in order to calculate this index which shown in below index diagram.

- In this diagram consider 1= on, 0=off
- Overall output voltage of equations suggested. Cascade multi-level inverter Vo=V1+V2+……+Vn
- Switch equations will be in this fashion S1, S2…..Sn-1.

	G1	G2	G3	G4	G5	G6	Vo
1	1	0	0	0	1	0	Va
2	0	0	1	0	0	1	Vb
3	1	0	1	0	0	0	Va+Vb
4	0	0	1	0	0	1	Vb
5	1	0	0	0	1	0	Va
6	0	0	0	0	1	1	0
7	0	1	0	0	0	1	-Va
8	0	0	0	1	1	0	-Vb
9	0	1	0	1	0	0	-Va-Vb
10	0	0	0	1	1	0	-Vb
11	0	1	0	0	0	1	-Va
12	0	0	0	0	1	1	0

3.3 Simulation Analysis of 7 Level Inverter With R Load

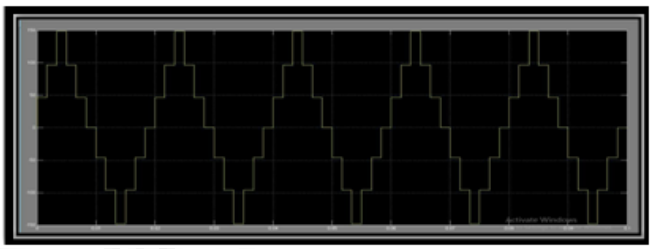


Figure 4: Output Voltage of 7 level inverter

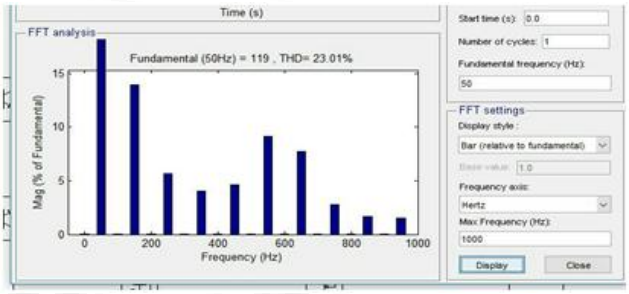


Figure 5: FFT analysis of 7 level inverter

3.4 Working Process

Working process shown power diagram fig 3.1.1 For seven level inverter For first half positive cycle, when IGBT number S1 and S5 are triggered then we get V1 positive. As discussed by theory V2 is 2time then V1.so after completed first step second step is IGBT S3 and S6 triggered then we get V2 on output side. The third step is IGBT S3and S1 is triggered as shown in pulse generation table. After that second step is repeat so IGBT S3 and S6 triggered then we get V2 on output side. Then firststep further come and repeat so IGBT number S1 and S5 are triggered then we get V1 positive. After completed positive cycle of first half cycle, negative half cycle process are there. When IGBT number S2 and S6 are triggered then we get V1 negative. As discussed by theory V2 is 2time then V1.so after completed first step second step is IGBT S4 and S5 triggered then we get V2 negative on output side. The third step is IGBT S2 and S4 is triggered as shown in pulse generation table. After that second step is repeat so IGBT S4 and S5 triggered then we get V2 negative on output side. Then first step further come and repeat so IGBT number S1 and S5 are triggered then we get V1 negative. This process for first half cycle then process is repeat and completed cycle.

4. Design Hardware and Components

4.1 Rectifier circuit circuit

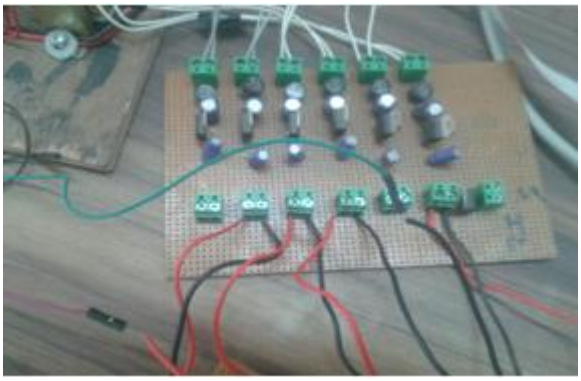


Figure 6: Rectifier circuit for 12 volt

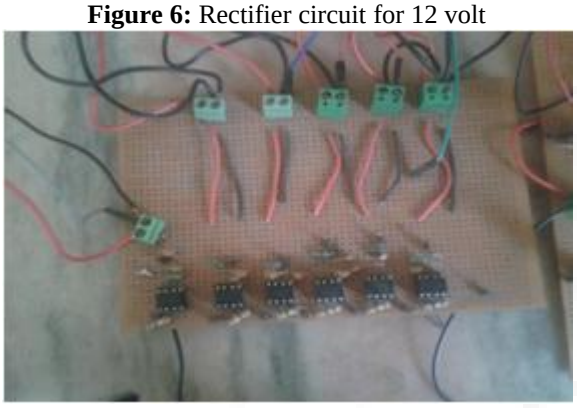


Figure 7: Hardware of pulse generation circuit

4.1.1. Specification and details

In rectified circuit hardware is used in output voltage of opto-coupler 6n136 . In this circuit ,first step down 230v AC to 12V AC and then this circuit rectified 12V DC which output is given to opto-coupler VC. In circuit we used two capacitor to filter DC output which are 25V &470 microfarad and 25V& 220 microfarad. Then we used regulator for 12 volte output DC which is L7812.

4.2 Pulse generation circuit

In this circuit first the Opto-coupler is used 6n136 which is taken because theoretical observation. Then we take input and output resistance as follow Ri – 350 ohm Ro – 1.9kilo ohm. And capacitor we take Capacitor C1 – 0.1 micro farad and C2 – 10 Pico farad in this circuit , 12 volt output which is came from rectified circuit is connected to Vcc (pin number 8) of Opto-coupler .

4.3. Microcontroller OF Rdino ATMEGA 2560

4.3.1Specification and details

- Active mode: 1MHZ & 1.8V 500 Micro Farad
- 32×8 general purpose working resistance
- DC Current per I/O Pin 40 mA
- DC Current for 3.3V Pin 50 mA
- Flash Memory 128 KB of which 4 KB used by Boot loader
- SRAM 8 KB, EEPROM 4 KB, Clock Speed 16 MHz

Figure 8: Diagram of microcontroller ATMEGA 2560

4.4 Source Rectifier circuit

4.4.1 Specification and details

In source circuit, we used for 50 V & 100 V AC to DC . for converting AC volt to DC volt used Rectifier bridge (AC to DC) .And for filter DC voltage capacitor are following, Capacitors. 160V & 1000 micro farad and 250V & 860 micro farad.

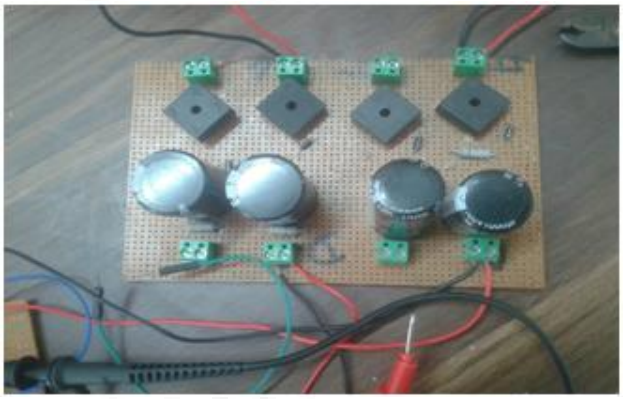
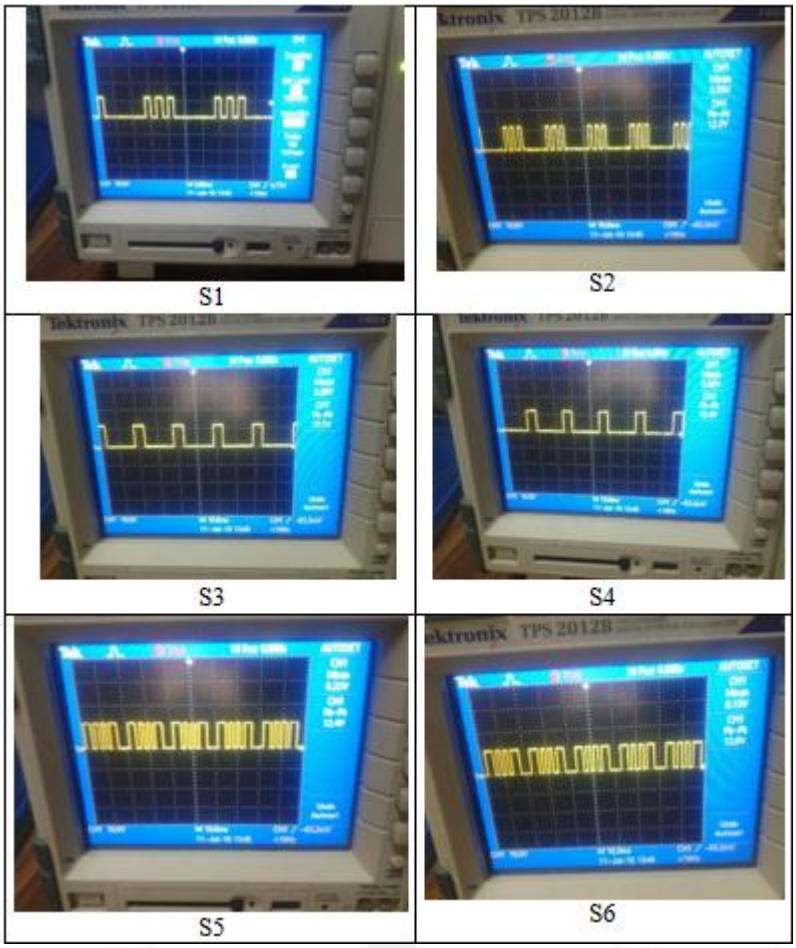


Figure 10: Source rectifier circuit diagram

Figure 9: Complete hardware diagram of pulse generation circuit

5. Result of hardware of bridge

5.1 Result of pulse generation by hardware circuit



5.2 Hardware of first 7 level bridge

Figure 12: hardware of 7 level bridge

5.3 Output on hardware of 7 level inverter (V1=10 and V2=20 volt)

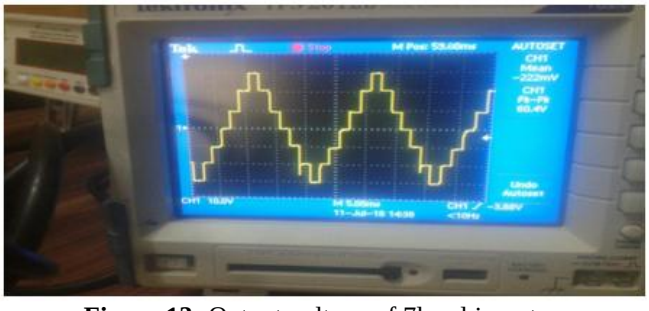


Figure 13: Output voltage of 7level inverter

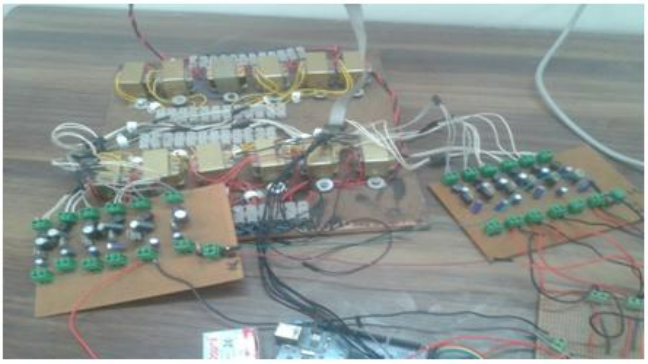


Figure 14: Output voltage with different scale of 7 level inverter

Figure 15: Final Hardware of 7 level inverter

6. Conclusion

A new topology of cascade multi level invert with increase level with few of switch and this topology also generated high power capability with all level odd as well as even level with low input d.c voltage .This topology also reduced THD ,dv/dt loss , switching losses with increase switching devices

References

[1] Jingsheng, L., H. Sepahvand, 2002. 'Investigationon Capacitor Voltage Regulation in Cascaded H-Bridge Multilevel Converters With Fundamental. 58 Frequency Switching'IEEE Transactionon Industrial Electronics, 11: 5102– 5111.
[2] Jose Rodriguez, Jih-Sheng Lai & Fang Zheng Peng, 2002. 'Multilevel Inverters: A Survey of Topologies, Controls and Application' IEEE Transactions on Industrial Electronics49(4): 724-738.
[3] Kim, J.H., S.K. Sul, P.N. Enjeti, 2008. 'A carrier-based PWM Method with Optimal Switching Sequence for a Multilevel four-leg Voltage Source Inverter,' IEEE Transactionon Industrial Electronics, 44(4): 1239-1248.
[4] Lai, Y.S., F.S. Shyu, 2002. 'Topology for Induction motor speed control by Multilevel Inverter,' IEEE Transactionon Industrial Electronics, 149(6): 449-458.
[5] Waltrich, G. and I. Barbi, 2010. "Three-phase cascaded multilevel inverter using powercells with two inverter legsinseries,"IEEETrans.Ind.Electron., 57(8): 2605–2612.
[6] Wang, K., Y. Li, Z. Zheng and L. Xu, 2013. "Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," IEEE Trans. Ind. Electron., 60(5): 1943–1954.
[7] Leon, J.I., S. Kouro, 2011. 'Multidimensional Modulation Technique for Cascaded Multilevel converters,'IEEE Transactionson Industrial Electronics, 58(2): 412-420