A Low Power CMOS 8T SRAM Cell for High Speed VLSI Design Using Transmission Gate Mode

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Abstract: In power consumption, reduction makes a device more reliable. In recent years, the demand of low power devices has increased and due to scaling of CMOS technology. Due to the scaling, the important advantage is the size of the chip decreases and the number of transistors increases in a system of chip (SOC). Power consumption is the most attentive parameter to design low power devices because it plays an important role in increasing the total power consumption of the devices. VLSI technology has created throughout the years thereby upgrading the performance of chips in terms of three fundamental constraints namely. Delay, area and power. A low power design has now become a most important issue in VLSI design, basically for high speed and high performance systems. At the technology level, technology optimization is the final tool that a designer can use to produce low power and a high-performance of SRAMs. In this paper, the 8T SRAM Cell has been design and implemented on 90nm and 45nm technology by using CADENCE VIRTUOSO. For simulation we are using 1V power supply and at different frequency (500MHz, 1GHz and 2GHz).

Keywords: conventional 6T SRAM Cell, Transmission Gate(TG), Delay, Power, PDP, VLSI circuit, integrated circuit (IC)

1. Introduction

The Moore’s law of scaling has been the main observation behind the semiconductor industry. Scaling has straightforwardly or in a roundabout way been the underlying driver of the colossal abilities of today’s ICs and their universal use in about all cutting edge electronic frameworks. In power consumption, reduction makes a device more reliable. In recent years, the demand of low power devices has increased and due to scaling of CMOS technology. Due to the scaling, the important advantage is the size of the chip decreases and the number of transistors increases in a system of chip (SOC). Power consumption is the most attentive parameter to design low power devices because it plays an important role in increasing the total power consumption of the devices. As the procedure technology keeps on scaling, the soundness of embedded Static Random Access Memories (SRAMs) is a developing worry in the configuration and test group.

A low power design has now become a most important issue in VLSI design, basically for high speed and high performance systems. A low power and high-performance of SRAMs cell requires an optimization of the technology and the circuits. At the technology level, technology optimization is the final tool that a designer can use to produce low power and a high-performance of SRAMs.

This paper presents a novel design technique for low power CMOS 8T SRAM circuits by using transmission gates for high speed VLSI design. In this paper, the proposed TG 8T SRAM cell decreases the voltage swing, which is defined as a difference between of maximum output voltage and minimum output voltage, however number of transistors are increased and area also in comparison to conventional SRAM cell but a low power dissipation at higher frequency can easily overcome this drawback.

Figure 1: Conventional 6T SRAM cell

However, if the operating frequency is increased of the SRAM Cell then the dynamic power dissipation will also be increased.
A. WRITE 0 OPERATION During the write 0 operation, WL will be precharged and bit line (BL) is low and bit bar line (BLB) goes to high. M5 and M3 transistor is on and charge stored in the BL goes to the M5-M4 path to ground. Due to zero value stored at Q, the M2 transistor gets on and M4 is off. So the charge is stored at Q Bar line.

B. WRITE 1 OPERATION During the write 1 operation, WL will be precharged and bit line (BL) is high and bit bar line (BLB) goes to low. M5 and M1 is on and M4 is off. The charge is stored on the Q is discharged through the M6-M4 path and due to this the low value is stored on the Q bar line.

3. Proposed SRAM Cell

In this paper, we have modified the SRAM Cell by using transmission gate as shown in Figure 2 below:

This paper proposes a design of TG based 8T SRAM cell. TG 8T SRAM cell does not possess any architectural changes except adding a PMOS in parallel with each access NMOS in conventional 6T SRAM cell shown by M5 and M6. The NMOS switch passes a good zero but a poor 1 and similarly, the PMOS switch passes a good one but a poor 0.

The working of TG 8T SRAM cell is: While we perform a write operation, both the bit lines (BL) are at opposite voltages which represent if bit line (BL) is at high i.e, 1 then BLB is at low i.e, 0 (BL=1 and BLB =0) or BL =0 and BLB =1). When WL becomes high and also WLB =0 which enables NMOS and PMOS transistors M5 and M6 then data writes on the output nodes Q and QB (Q Bar line).

4. Simulation and Results

This section performs the detailed simulation analysis performed for the proposed SRAM Cell at 90nm and 45nm CMOS technology. We simulate the proposed 8T SRAM cell to calculate the power dissipation, delay and Power delay product (PDP) during write 0 operation and write 1 operation at various operating frequency(500MHz, 1GHz, 2GHz).

A. At 90nm Technology

B. At 45nm Technology
The schematic of proposed SRAM cell is designed and implemented by using CADENCE VIRTUOSO at 90nm CMOS technology and 45nm CMOS technology. For simulation we are using 1V power supply and for different frequency (500MHz, 1GHz and 2GHz) we are using 0.5 volt during simulation. These simulated results are compared with the proposed TG8T SRAM cell at 90nm CMOS technology and at 45nm CMOS technology.

We simulate the proposed SRAM Cell at frequencies of 500MHz, 1GHz, and 2GHz respectively. The Simulated results of 500MHz, 1GHz and 2GHz at 90nm CMOS technology and 45nm CMOS technology have been shown in Figure 4, 5, 6, and 7 respectively.

Proposed model has been simulated in 90nm CMOS technology and 45nm CMOS technology that's why we select 90nm and 45nm length of all the transistors.

Finally we have calculated the power dissipation, delay and power delay product (PDP) in the proposed TG8T SRAM Cell at 500MHz, 1GHz and 2GHz frequency and have compared the result on two different technology i.e., 90nm CMOS technology and 45nm CMOS technology shown below in Table I:

**Table 1: Comparison table for TG8T (90NM Technology) and TG8T (45NM Technology)**

<table>
<thead>
<tr>
<th>parameters</th>
<th>POWER</th>
<th>WRITE ‘1’ DELAY</th>
<th>WRITE ‘0’ DELAY</th>
<th>PDP ‘1’</th>
<th>PDP ‘0’</th>
</tr>
</thead>
<tbody>
<tr>
<td>500MHz</td>
<td>4.972uW</td>
<td>30.91ps</td>
<td>21.29ps</td>
<td>71.71J</td>
<td>49.39J</td>
</tr>
<tr>
<td>1GHz</td>
<td>137.9nW</td>
<td>73.51ps</td>
<td>23.48ps</td>
<td>10.07J</td>
<td>3.21J</td>
</tr>
<tr>
<td>90nm tech.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45nm tech.</td>
<td>4.822uW</td>
<td>30.91ps</td>
<td>21.29ps</td>
<td>148.32J</td>
<td>102.19J</td>
</tr>
<tr>
<td>45nm tech.</td>
<td>229.9nW</td>
<td>73.51ps</td>
<td>23.48ps</td>
<td>16.83J</td>
<td>5.37J</td>
</tr>
</tbody>
</table>

So from these results it is proofed that the proposed TG8T SRAM cell approaches for CMOS based SRAM design is suitable for high speed VLSI design. Hence, if the operating frequency of the SRAM cell is increased then the dynamic power dissipation will also be increased.
and power delay product (PDP) at '1' and '0' write operation between the TG8T SRAM (90nm Technology) and TG8T SRAM (45nm Technology) shows that the power dissipation is reduced and also the delay and PDP are reduced. That is my aim to reduce these things. It is graph representation at 90nm and 45nm technology.

5. Conclusions

As it is noticed that the proposed design of SRAM cell contributes to major reduction in power dissipation, future research to develop a more power efficient and area minimized SRAM architecture and memory designing. In future, the operating voltage should be minimized for technology scaling system. Also speed and delay consideration should be developed for the system so that both power and speed is optimized. By developing these research works, the proposed system can be taken to a better efficiency level considering power, speed and area.

References

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