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Comparison of 3 Level and 5 Level NPC Inverter using SPWM

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Abstract: ***Multilevel inverters are becoming increasingly popular for high and medium power applications. The diode clamped multilevel inverter (DCMLI) is an attractive high voltage multilevel inverter due to its robustness. For pulse generation the Sinusoidal Pulse Width Modulation (SPWM) technique is used. In this paper a comparative study of 3level multilevel inverter and 5 level multilevel inverter using Sinusoidal Pulse Width Modulation is done. The total harmonic distortion present in the output waveform of 5 level multilevel inverter is reduced compared to 3 level inverter. The inverter is connected to a 1HP induction motor and its performance analysis is done. Torque ripple is reduced in a 5 level inverter compared to 3 level inverter. The result is verified using Matlab simulation.***

Keywords: Multilevel inverter, Three level diode clamped MLI, Five level diode clamped MLI, Sinusoidal Pulse Width Modulation

1. Introduction

Multilevel voltage source inverters (VSI) are now well-accepted in high power applications which need high waveform quality, using an array of semiconductor switches connected in series/parallel combinations. Multilevel topologies can synthesize near sinusoidal voltage with low harmonic distortion that reduces the size of output filter [1], [2]. These topologies have also low switch stress, reduced common mode voltage, and high voltage capability [3], [4]. The diode clamped converter (DCC), flying capacitor converter (FC), and the cascaded H-bridge (CHB) converter are the most well-known multilevel converter topologies [5], [6]. The increasing number of levels in the inverter will generate more steps of staircase waveform at the output voltages which will result in the reduction of total harmonic distortion. The two most widely used PWM schemes for multilevel inverters are the carrier-based sine-triangle PWM (SPWM)technique and the space vector PWM (SVPWM) technique. These modulation techniques have been extensively studied and compared for the performance parameters with two level inverters [7], [8]. The SPWM schemes are more flexible and simpler to implement. The SPWM technique, when applied to multilevel inverters, uses a number of level-shifted carrier waves to compare with the reference phase voltage signals [9]. Switching technique and the number of levels for multilevel inverter plays an important role in reducing the total harmonics distortion (THD).

AC motors combined with their drives have replaced DC motors in industrial applications due to their lower cost, better reliability, lower weight, and reduced maintenance requirement. Squirrel cage Induction motors are more widely used than all the rest of the electric motors put together as they have all the advantages of AC motors and they are easy to build [10]. By improving the output voltage of the inverter, the torque ripple present in the induction motor is reduced.

2. Sinusoidal Pulse Width Modulation Technique

This is a very simple technique for harmonic reduction. In this technique pulse magnitude will be constant and only pulse time (width) can be changed. In this pure sine wave is compared with carrier (triangular) wave and produces gate pulses. Sine wave has fundamental frequency and carrier wave can be taken more than fundamental frequency. In the modulation techniques, there are two important defined parameters: 1) the ratio P = ωc/ωm known as frequency ratio, 2) the ratio Ma = A_m/A_C known as modulation index, where ωm is the reference frequency, ωc is the carrier frequency, A_m is reference signal amplitude and A_C is carrier signal amplitude. Instead of maintaining the width of all pulses, the width of each pulse is varied proportional to the amplitude of a sin-wave evaluated at the center of the same pulse.

By comparing a sinusoidal reference signal with a triangular carrier wave, the gating signals are generated. The frequency of reference signal determines the inverter output frequency and its peak amplitude, controls the modulation index, Ma, and then in turn the RMS output voltage. Figure 3 shows the most common carrier technique, the conventional sinusoidal pulse width Modulation (SPWM) technique, which is based on the principle of comparing a triangular carrier signal with a sinusoidal reference waveform (natural sampling).

3. Diode Clamped Multilevel Inverter (DCMLI)

3.1 Three Level NPC Inverter

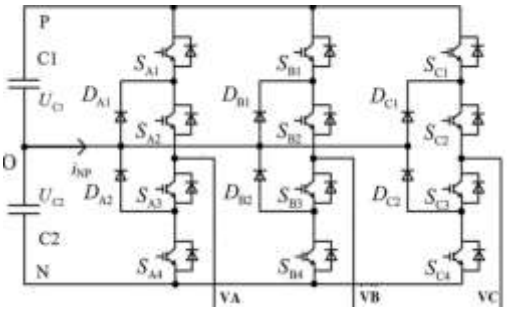

Figure 1: Three Level NPC inverter

In a diode-clamped inverter, a single DC bus voltage is shared by a series of capacitors arranged as a string. An array of semiconductor switches and diodes make each leg of the three phase inverter capable of being switched to any of the available voltage levels. Figure 1 shows the structure of three phase three level NPC inverter. It is composed of two capacitors for a common DC-link, four active switches S_{A1}, S_{A2}, S_{A3} and S_{A4} and two clamping diodes D_{A1} and D_{A2} in each phase leg. The switches S_{A1} and S_{A3} and S_{A2} and S_{A4} are two complementary pairs in phase A. Similarly, the switches S_{B1} and S_{B3} and S_{B2} and S_{B4} are complementary pairs in phase B and switches S_{C1} and S_{C3} and S_{C2} and S_{C4} are complementary pairs in phase C. If E is the input voltage, the switching states and respective pole voltages of phase leg A are provided in Table 1.

Table 1: Switching states of three level NPC inverter

Symbol	*Switching States*				*Terminal Voltage*
	S_{A1}	S_{A2}	S_{A3}	S_{A4}	
P	ON	ON	OFF	OFF	E
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-E

3.2 Five-level inverter topology and operation principle

Fig 2 shows the structure of a five level NPC inverter. It has capacitors C1, C2, C3 and C4 for common DC link of which the magnitude of each capacitors should be E which is equal to $V_{dc}/4$, where V_{dc} is the input DC voltage. Phase A, phase B and phase C has eight active switches and six clamped diodes connected to the neutral point of the DC link. The eight active switches in phase A are Sw1, Sw2, Sw3, Sw4, Sw4a, Sw3a, Sw2a, Sw1a, in phase B are Sw5, Sw6, Sw7, Sw8, Sw8a, Sw7a, Sw6a, Sw5a and in phase C are Sw9, Sw10, Sw11, Sw12, Sw12a, Sw11a, Sw10a, Sw9a. The six clamped diodes in phase A are D1, D2, D3, D4, D5, D6, in phase B are D7, D8, D9, D10, D11, D12 and in phase C are D13, D14, D15, D16, D17 and D18. The upper four switches are complementary to the lower four switches. For example, Sw1, Sw2, Sw3, Sw4 and Sw4a, Sw3a, Sw2a, Sw1a are complimentary pairs of switches respectively for phase leg A.

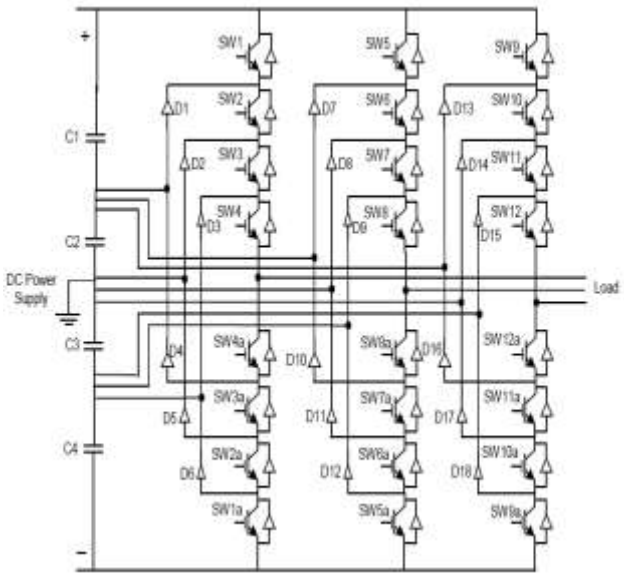

Figure 2: Structure of five level NPC inverter [11]

4. Principle of Voltage Shifted Modulation

Voltage shifted modulation is way based on the carrier modulation. If the DC side capacitor voltage is equal to four, the carrier number is m-1 when five level diode clamped inverter level number is m. all of these carriers have the same frequency and the same amplitude. This (m-1)a triangular carrier in the space is distributed vertically, and the occupied area is continuous, with each other closely connected, symmetrically distributed on the horizontal axis on both sides, and then with a sinusoidal modulation wave are compared, to generate a trigger pulse.

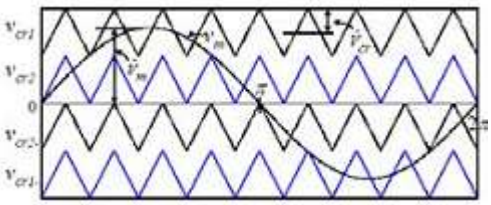

Figure 3: Principle of Phase Disposition Modulation

Voltage shifted modulation is used to generate the pulse for 5 level Neutral Point Clamped Inverter.

5. Simulation Results

The three level and five level MLI are simulated using matlab and its results are verified. The parameters used for the simulation of the three level NPC inverter is shown in Table 2.

Table 2: Parameters for simulation of MLI

Parameters	*Values*
DC input voltage	400 V
DC link capacitance	200F
Switching frequency	4 kHz
Rated output frequency	50 Hz

The inverter is connected to a 1 HP induction motor. The parameters used for the modelling of Induction motor is given in Table 3.

Table 3: Parameters for simulation of IM

Parameters	*Values*
Rotor resistance	0.39
Stator resistance	0.19
Stator leakage inductance	0.21e-3
Rotor leakage inductance	0.6e-3
Magnetising winding inductance	4e-3
Frequency	50

The three level NPC inverter is simulated. and Figure 4(a) shows the output line voltage obtained when 3 level NPC inverter is operated with SPWM

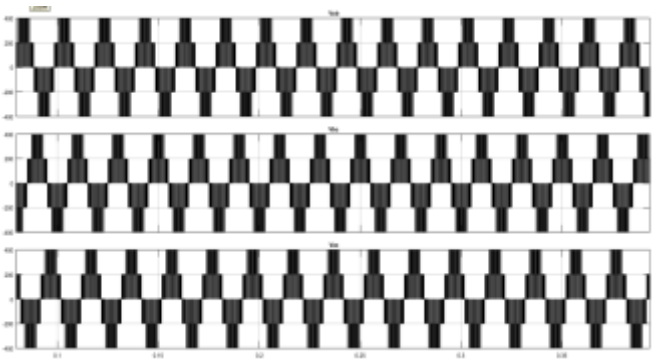

Figure 4(a): Line- Line output Voltage of 3 level NPC inverter

FFT analysis of the output line voltage of the inverter is done. Figure.4(b) shows the harmonic spectrum. The fundamental component and THD is obtained when 3 level NPC inverter is operated with SPWM. The THD obtained is 66.45%.

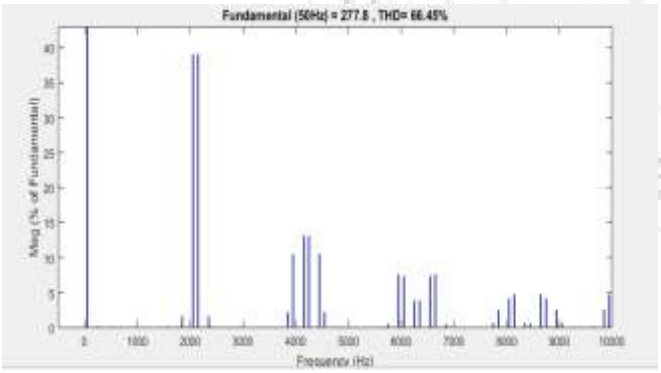

Figure 4(b): FFT of Line- Line output Voltage of 3 level NPC inverter

Figure 4(c): shows the torque response, phase current and speed of 1HP induction motor fed from 3 level inverter, Torque waveform contains large amount of ripples. The speed is of the motor is settled to 314rad/sec.

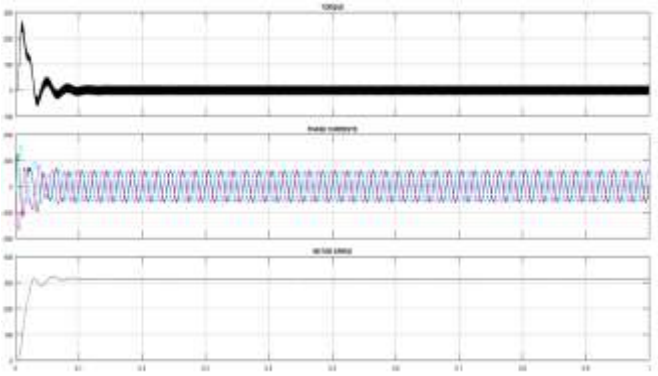

Figure 4(c): Torque, current and speed of Induction Motor

Figure. 4(d) shows the output line voltage obtained when 5 level NPC inverter is operated with SPWM

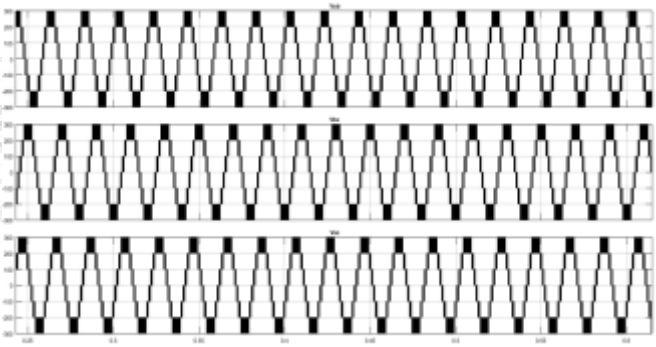

Figure 4(d): Line- Line output Voltage of 5 level NPC inverter

Figure.4(e) shows the harmonic spectrum of output voltage of 5 level inverter. The fundamental component and THD is obtained when 5 level NPC inverter is operated with SPWM. The THD obtained is 21.69%. The THD obtained is reduced by using a 5 level NPC inverter.

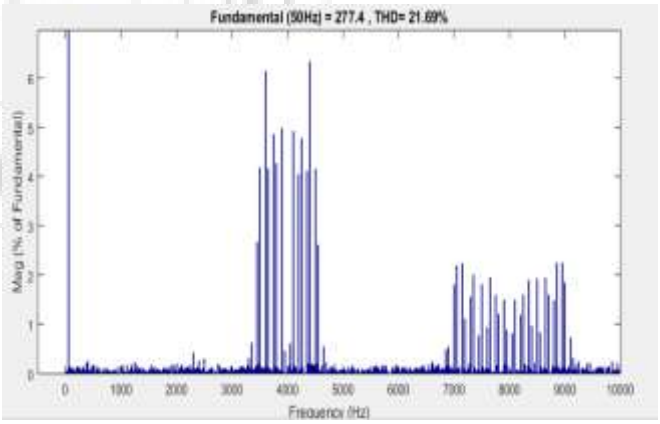

Figure 4(e): FFT of Line- Line output Voltage of 5 level NPC inverter

Figure 4(f) shows the torque response, phase current and speed of 1HP induction motor fed from 5 level inverter. The ripple present in the torque waveform is reduced.

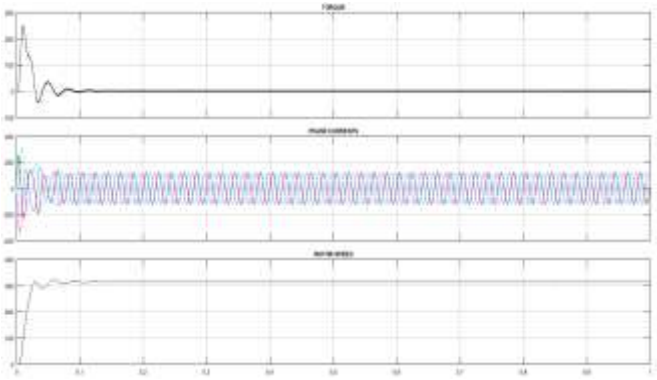

Figure 4(f): Torque, current and speed of Induction Motor

6. Conclusion

The working of 3 level and 5 level NPC inverter is studied. The concept of SPWM and voltage shifted modulation is analyzed. The 3 level and 5 level inverter is simulated using matlab and the results are verified. In waveform obtained at the output of 5 level inverter has more number of steps and THD obtained is less compared to 3 level NPC inverter. The Multilevel inverters are connected to induction motor and the output waveforms are analyzed. It is inferred that the torque ripple present in the induction motor is very much reduced by using 5 level NPC inverter.

References

[1] B.Wu, High-Power Converters and AC Drives. Piscataway, NJ: IEEE Press, 2006.
[2] J. Rodriguez, S. Bernet, B.Wu, J. Pontt, and S.Kouro, "Multilevel voltage source- converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
[3] S. Kouro et.al, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., Vol. 57, No. 8, 2553-2580, Aug. 2010.
[4] G Murgesan et.al (2011) , "A new multilevel inverter topology using less number of switches," International Journal of Engineering Science and Technology,2, 5000-5010.
[5] W. Chenchen and L. Yondong, "A survey on topologies of multilevel converters and study of two novel topologies," in IEEE 6th International Conference on Power Electronics and Motion Control (IPEMC), pp. 860-865, 2009.
[6] J.Rodriguez, L.Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," Industrial Electronics, IEEE Transactions on, vol. 49, pp. 724-738, 2002.
[7] Holtz, J, "Pulsewidth modulation–A survey", IEEE Trans. Ind.Electron., vol.30, no. 5, pp. 410–420, 2009.
[8] Zhou, K., and Wang, D, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis",IEEE Trans. Ind. Electron., vol. 49, no.1, pp. 186–196, 2002.
[9] Carrara,G.,Gardella,S.G.,Archesoni,M.,Salutari,R.,andS ciutto,G, "A new multi-level PWM method: A theoretical analysis," IEEE Trans. Power Electron., vol.7, no. 3, pp. 497–505, 1992.
[10] Novotny, D. W.and Lipo, T. A."Vector Control and Dynamics of AC Drives." Oxford University Press Inc, New York, 1996.
[11] Quoc Anh Le and Dong-Choon Lee, "Modified SVPWM to Eliminate Common-ModeVoltages for Five-Level ANPC Inverters," *IEEE Conference on ECCE, 2016*

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