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A Novel Approach towards Bridgeless Converter based SMPS for Power Quality Improvement

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Abstract: ***The conventional SMPS used in computer & other similar appliances has major issues in supplied power on distorted input current, harmonic rich, poor power quality etc. To mitigate these issues , bridgeless SEPIC converter was proposed which provides stiffly regulated output dc voltage even under input/ load voltage variations. So that harmonics at the input side was reduced. Model was developed in MATLAB/ Sim power systems. The superior results demonstrated by the proposed model.***

Keywords: Bridgeless converter, PFC, SMPS, PCC, PWM, DBR

1. Introduction

Personal computer is one of the electronic equipment which is severely affected by power quality problems. Single stage and two stage conversion of ac voltage into dc voltage have been used in computers to maintain harmonic content within limits and also to obtain stiffly regulated output. Many electronic appliances powered up from the utility utilize the classical method of ac-dc rectification which involves a diode bridge rectifier (DBR) followed by a large electrolytic capacitor. The uncontrolled charging and discharging of this capacitor instigates a harmonic rich current being drawn from the utility. Modern ac-dc converters incorporate power factor correction (PFC) and harmonic current reduction at the point of common coupling (PCC) which improves voltage regulation and efficiency at the load end.

Single stage power conversion is simple, compact and cost effective. However, it suffers from poor dynamic response, high capacitance value and high component stress. So, two stage conversion of ac voltage into multiple dc voltages is mostly preferred in computers [6]. It provides better output voltage regulation, fast dynamic response and blocks the 100Hz component in the first stage itself so that large capacitors at the output side are avoided.

A boost converter is the common choice for providing PFC in power supplies. However, it is not the preferred choice in computer power supplies due to its large input voltage range. The output voltage of a boost converter cannot be controlled to a value less than 300V for a 220V ac input supply. Therefore, buck-boost converter is preferred in computers where wide variations in input voltages and load are expected.

The efficiency of a two stage SMPS is lower than the conventional SMPS, to eliminate this disadvantage, a new bridgeless front end converter is proposed in this paper for computer power supplies and other similar appliances. The elimination of DBR at the front end results in reduced conduction losses and large output voltage range with enhanced efficiency .At the output of the front end converter, a half bridge converter is used which provides isolation, regulation and multiple dc outputs .The half bridge converter is a common choice because it offers better core utilization.

2. Proposed Work

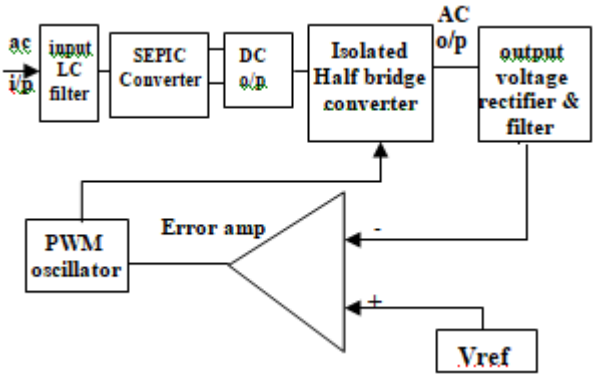

Figure 1: Block diagram for proposed work

Fig 1 shows block diagram for proposed work. The proposed PFC Converter consists of mainly two parts, bridgeless front end ac-dc converter and multi-output isolated dc-dc converter. The front end converter is designed in discontinuous conduction mode (DCM) for achieving inherent PFC while the isolated converter is designed in continuous conduction mode(CCM).

The configuration of proposed PFC converter SMPS with dc output voltage is shown in Fig 2. At the input side, DBR is eliminated by using two SEPICs. The upper converter operates in the positive half cycle and the lower one in the negative half cycle of the input ac voltage. The switching frequency of both the converters is set at 20kHz for efficient control. The design of output inductors for both the converters is carried out in DCM to reduce the complexity in control. The regulation of the output voltage is able to take care of wide variations in the input voltage and load.

The output dc voltage is sensed and compared with a reference voltage from which the voltage error is obtained which is given to a proportional and integral (PI) controller; the PI controller output is compared with a high frequency

saw-tooth wave to yield PWM pulses that are given to both switches simultaneously.

The width of these PWM pulses varies according to the output of the PI controller so that the output dc voltage is regulated effectively which is, in turn, fed to the isolated half bridge converter in the second stage to obtain regulated output voltage. The isolated converter is operated in CCM to take the advantage of reduced stress. If the load in any of the winding changes, the duty cycle changes accordingly to ensure regulated dc outputs.

3. Operating Principle

During the positive half cycle of the input voltage, the upper SEPIC operates, in the same way, during negative half cycle the lower SEPIC would operate. The operation of the SEPIC in one PWM cycle is described with the help of the following modes: In the first mode, the high frequency switch Sp turns on, the input inductor Lp1 starts storing the energy which is transferred from the single phase ac mains. Diode Dp1 completes the current path. In the second mode, Sp is turned off and diode Dp2 starts conducting. The energy in output inductor Lp2 starts decreasing to zero in . In the last switching state, the current in the output inductor remains zero until the start of next switching cycle. This mode ensures the DCM operation.

Two high frequency switches are turned on and off alternately in one switching cycle. So, the operation of the converter in one half of the switching cycle is the same as that of the other half cycle.

4. Simulation Model

The model is implemented and designed as per the above block diagram. In MATLAB Library, we had selected sinusoidal AC voltage source is selected to provide the voltage to the circuit. To reduce the higher order harmonics, an L-C filter is used at the input side. The chopped AC voltage is converted into DC with the help of diodes used in the SEPIC converter.

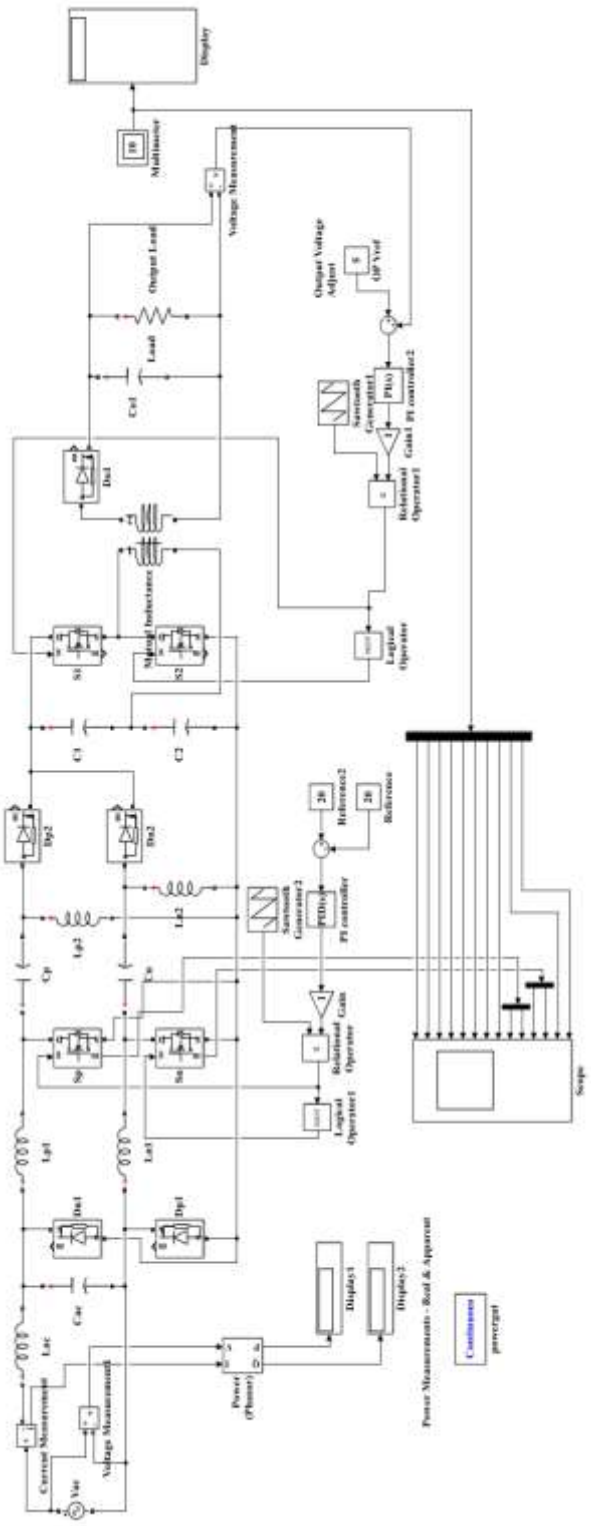

Figure 2: Schematic diagram of PFC converter based SMPS

In the first half cycle, the upper switch S1 is turned on. The diodes on the secondary side start conducting and the inductors in all the secondary windings start storing energy. All the filter capacitors discharge through the loads to maintain dc output voltages as constants. In the next half cycle of the PWM period, the upper switch is turned off. The secondary diodes are turned on to free-wheel the inductors currents.

Design of the proposed bridgeless converter based SMPS System

The design for the positive half cycle operated PFC converter is carried out here. The negative half cycle operated converter is designed in the same way. The average voltage Vacav is calculated as,

$$V_{acav} = \frac{2\sqrt{2}\times Vac}{\pi} = \frac{2\sqrt{2}\times 250V}{3.14} = 225V \quad \ldots\ldots(1)$$

The duty cycle D of the PFC buck-boost converter is expressed as the ratio of its output dc voltage to the sum of output dc voltage and input voltage .

$$\text{Duty cycle, } D = \frac{V_{PFC}}{V_{PFC} + Vacav} \quad \ldots\ldots(2)$$

The input inductor value is calculated for the permitted ripple of 40% of input current.

$$Lp1 = \frac{DVacav}{f \times (i \text{ in ripple})} \quad \ldots\ldots(3)$$

where, f is the switching frequency of the PFC converter

The equivalent value of inductance of the PFC converter is given as,

$$Leq = \frac{Rdc\ Ka}{2f} \quad \ldots\ldots(4)$$

Where, Ka is critical conduction parameter

The output inductor value is calculated as,

$$Lp2 = \frac{Lp1}{Lp1\text{-}Leq} \quad \ldots\ldots(5)$$

The intermediate capacitor value is estimated as,

$$Cp = \frac{1}{(\omega r)^2 (Lp1+Lp2)} \quad \ldots\ldots(6)$$

Where ω_r is the angular frequency ($\omega_r = 2\pi fr$)

Specifications:

Frequency	50Hz
Switching frequency	20kHz
Input inductors (Lp1, Ln1)	4.35mH
Output inductors (Lp2, Ln2)	225µH
Intermediate capacitors (Cp, Cn)	0.22µF
Output voltage	5Vdc

5. Results &Discussions

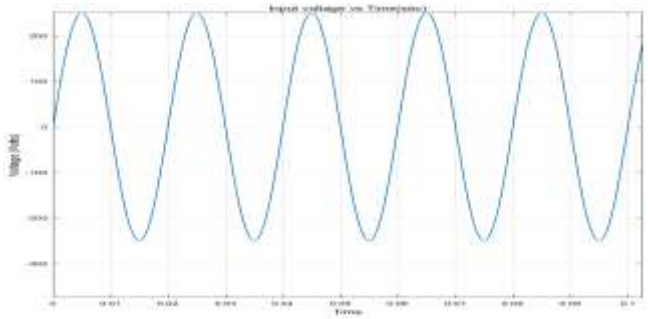

Figure 3 A

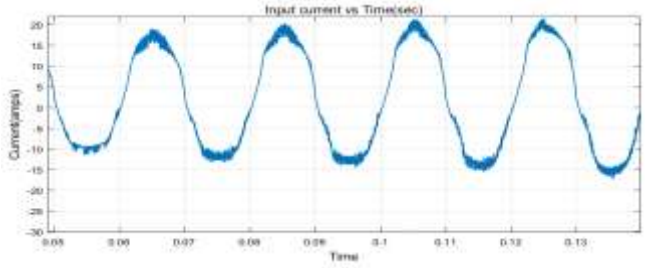

Figure 3 b

Figure 3: Input voltage and current of PFC power supply at rated condition

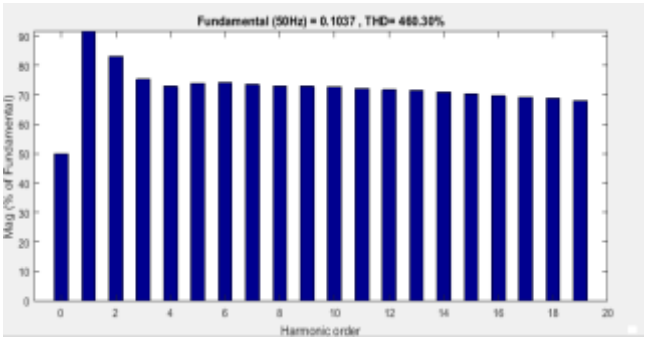

Figure 4: Harmonic spectrum of conventional SMPS

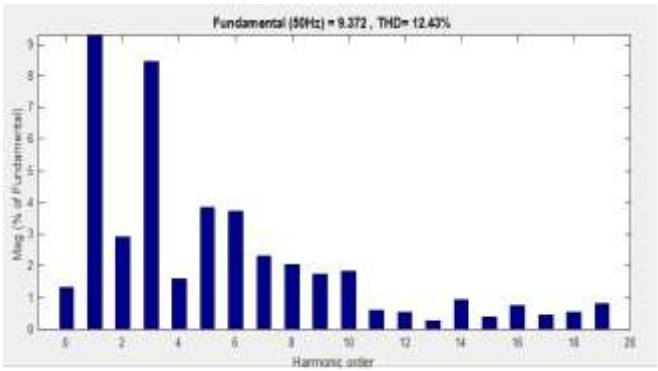

Figure 5: Harmonic spectrum of PFC converter based MPS

Table 1: THD Comparison

Parameters	Conventional SMPS	PFC converter based SMPS
Input line current	460.30%	12.43%
Input voltage	24.89%	0.01%

From fig 3, the input ac voltage and current are found to be sinusoidal. So there is no harmonics at the input side, thus power quality is improved. From fig 4 & fig 5, we can observe that harmonic distortion is reduced to 12.42%.The comparison is shown in table 1.The output voltages are maintained constant with their respective output currents.

6. Conclusion

In this bridgeless SEPIC Converter based Switch Mode Power Supply were implemented. SEPIC converter is used to reduce the harmonics and to get stiffly regulated output. The proposed scheme was implemented in MATLAB/ SimPowerSystem, the results are achieved experimentally.

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