

Design and Implementation of a PLL using a Single-Event-Transient Hardened-by-Design (SETHBD) Charge Pump

Pallavi. K. R¹, Dr. K. N. Muralidhara²

¹Dept.of Electronics and communication PESCE Mandya, Karnataka, India

²Professor of Department of Electronics and Communication PESCE Mandya

Abstract: The Phase Locked Loop (PLL) is a combined system of phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO), frequency divider (FD). The PLL is widely used in RF and wireless transceivers, optical fiber receivers and carrier synthesis in cellular telephones etc. The PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages- free running, capture and locked or tracking. Once the PLL is locked, it can track frequency changes in the incoming signals. In the proposed PLL, the designed PFD is free from dead zone. The single-event-transient hardened-by-design (SETHBD) charge pump is used instead of traditional CP to overcome the single event effect's (SEEs) such as single-event upset (SEU), multiple bit upset, single-event transient (SET), and latch up problems. Here we use the radiation hardened circuit and reference circuit along with the charge pump circuit. And the 5-stage current starved voltage controlled oscillator is used. And the divided by 4 frequency divider circuit is designed for feedback circuit using a 2-D flip-flop's (N/4). The PLL design is implemented in cadence virtuoso 180nm technology with a supply voltage of 1.8V operates at a frequency of 1GHZ and all the simulations are done using cadence simulator.

1. Introduction

The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, parallel and serial data communication, and frequency synthesizers. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a mixed signal PLL which must operate in the GHz range with less lock time.

PLL is simple feedback system that compares the output phase with the input phase and produces the output frequency which is proportional to the input phase difference. Since it consists of a four primary blocks namely phase frequency detector (PFD), charge pump and low pass filter (CPLPF), voltage controlled oscillator (VCO), and frequency divider (FD) as shown in figure 1.

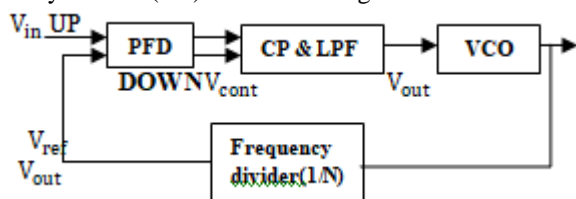


Figure 1: Phase locked loop.

The output of the phase detector is applied to CP and then to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO. The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies. PLL goes through 3 states, i) free running ii) Capture iii) Phase lock. Before applying the input, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change

until it equals the input frequency and the PLL is in phase lock mode.

When phase locked, the loop tracks any changes in the input frequency through its repetitive action. If an input signal V_{in} of frequency f_{in} is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V_{out} and f_{out} of the VCO. If the two signals differ in frequency and/or phase an error voltage is generated. And is applied to the low pass filter which removes the high frequency components is amplified and then feed as a input to the voltage controlled oscillator this signal will shifts the VCO frequency in order to reduce the difference between input and feedback signal from VCO.

The VCO will change frequency until its output frequency is exactly same as the input frequency hence the circuit is said to be locked, but there is small phase difference this phase difference generates a control voltage to shift the VCO frequency from f_{in} to f_{out} and to maintain the phase lock condition.

The charge pump circuit is interpose between PFD and LPF. It consists of two switches that pump charge into or out of the LPF. The loop locks when the phase difference drops to zero and the charge pump remains relatively idle.

Single-event effects (SEEs), which include single-event upset (SEU), multiple bit upset, single-event transient (SET) and latch up, present a major challenge to the function and reliability of integrated circuits in spaceflight systems [1]. The SET is a well-known problem for analog, digital and mixed signal circuit with technology scaling and as the clock speed continues to increase. In fact, phase-locked loops (PLLs) are used as a clock generation circuit for microprocessors, space satellites and communication circuits.

Any malfunction due to SETs on PLLs can result in system-wide errors in communication networks. So, it is important to ensure the highest level of radiation tolerance for PLL circuits. Recently, many SET effects in PLL systems have reported and solutions have been proposed to mitigate the SET effects by adopting radiation-hardened-by-design (RHBD) techniques.

2. Objectives

- To design, simulate, and synthesis phase frequency detector (PFD).
- To design, simulate, and synthesis Single-event-transient hardened-by-design (SET HBD) charge pump with low pass filter (CP LPF).
- To design, simulate, and synthesis 5 stage current starved voltage controlled oscillator (CS-VCO).
- To design, simulate, and synthesis the frequency divider.
- To design, simulate, and synthesis PLL which includes PFD, SET HBD charge pump and LPF, CS-VCO, FD as quoted above using 180nm technology.

3. Architecture of PLL

A PLL in the most basic of terms is a feedback system. It consists of a Phase detector, charge pump loop filter and a voltage controlled oscillator, figure 1 shows a basic phase locked loop. The PLL is said to achieve lock when the phase difference between the two input signals becomes constant and the corresponding frequencies become equal. The phase frequency detector (PFD) generates an error pulse for a phase difference between the two signals. This error signal is often amplified and converted into an analog signal by a charge pump. The analog output of the charge pump is passed onto the low pass filter which suppresses the high frequencies, enabling the dc component called control voltage. This control voltage is the controlling input of the VCO which determines the oscillation frequency of the VCO. The VCO changes its frequency to accumulate enough phase for the PLL to achieve lock. The VCO output is fed back into the PFD for comparison. A PLL can be modified such that it multiplies its input frequency by factor of N. Figure shows basic frequency multiplication concept. Just like a voltage divider is used in feedback in voltage amplifier, as shown in figure 1, output frequency of PLL is divided by M and applied to the phase detector, we get, $f_{out} = Nf_{in}$. Also, since f_{in} and f_{out} must be equal, PLL multiplies f_{in} by N.

a) Phase frequency detector (PFD) :-

Phase detectors compare the phase between the input data and the recovered clock used to sample the data and use the information to align the sampling clocks phase to the data. Thus, they should provide two essential functions: Data transition detection and Phase difference detection. The obtained phase/frequency difference is detected and given as an input to CPLF which generates appropriate control voltage that modifies the VCO frequency according to the error.

PFD will works similar to X-OR gate as the phase difference between the two inputs varies, so does the width of the output pulse will rise, thereby providing a dc level proportional to the phase difference $\Delta\phi$ as shown in figure 2 and figure 3.

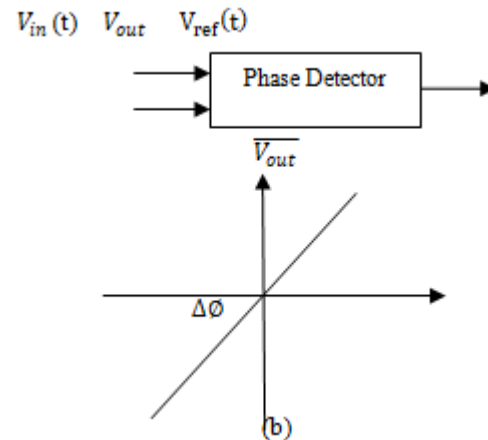


Figure 2: Definition of phase detector

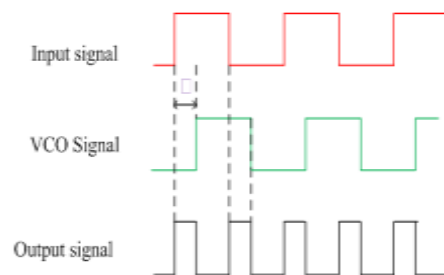
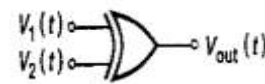


Figure 3: Exclusive OR gate as phase detector.

The Phase Frequency Detector (PFD) generate a phase error (UP/DOWN) signal by comparing phase of input (reference) signal and VCO output signal. UP signal will be HIGH when phase of input (reference) signal leads to VCO output signal otherwise DOWN signal will be HIGH.

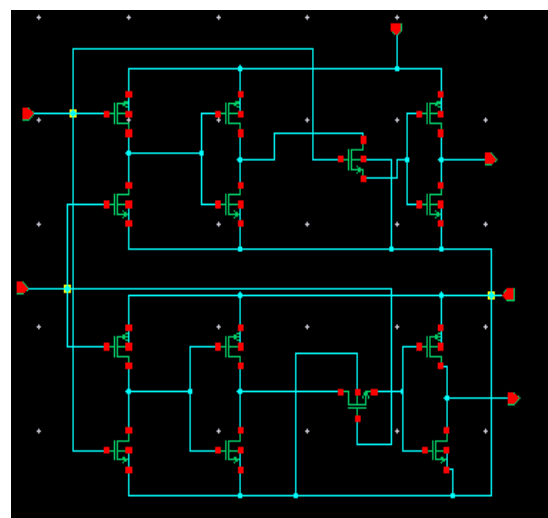


Figure 4: Proposed PFD

Here the inputs they named as aV_{in1} and V_{in2} for inputs V_{in} and reference input V_{ref} respectively. When the input V_{in1}

leads V_{in2} in phase, the PFD will generate a pulse signal on UP line. When input V_{in1} lags V_{in2} in phase the PFD will generate a pulse signal on the DOWN line. The generated pulse signal on the UP (DOWN) line, represents the phase difference between the leading edges of the inputs V_{in1} and V_{in2} , will activate the charge pump model to source (sink) the current to (from) the low pass filter.

The PLL compares the phase of the input V_{in} and the feedback V_{ref} , so the phase difference between the input V_{in} and the feedback V_{ref} is expected to be invariable in the steady state. That is to say, when F_{in} and F_{ref} does not change with time, the PLL is in lock state. Here, F_{in} and F_{ref} are those phases of the input V_{in} , the output V_{out} and the feedback signal V_{ref} respectively. Therefore

$$\frac{\partial \phi_{ref}}{\partial t} - \frac{\partial \phi_{in}}{\partial t} = 0 \text{ -----Eq.1}$$

Where, ϕ_{in} is input phase
 ϕ_{ref} is the reference phase

The gain of PFD is given by,

$$K_{PFD} = \frac{V_{DD}}{\pi} \text{ -----Eq.2}$$

$$= \frac{1.8}{\pi}$$

$$= 0.5729 \text{ V/radians}$$

A. Charge pump and low pass filter (CPLPF):-

Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO. The CP is an essential component of the PLL, because it generates the signal and renews the clock pulses at high speeds while integrating the loop filter. In the CP, two switches process the conversion of up and down signals from the PFD into current. The PLL's Performance is determined by the PFD and CP optimized to match with zero static phase error.

The charge pump output current is given by,

$$I_{CP} = K_{CP} \times \Delta\phi \text{ -----Eq.3}$$

Where, $K_{CP} = \frac{I_{PUMP}}{2\pi} \text{ -----Eq.4}$

$$\Delta\phi = \phi_{in} - \phi_{ref} \text{ -----Eq.5}$$

The phase difference $\Delta\phi$ is zero when loop voltage is in lock.

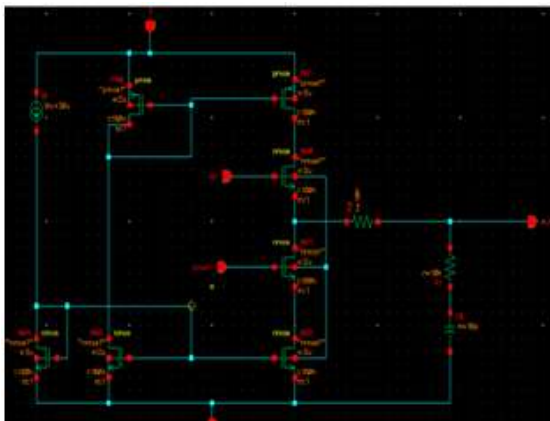


Figure 5: Conventional Charge pump with low pass filter

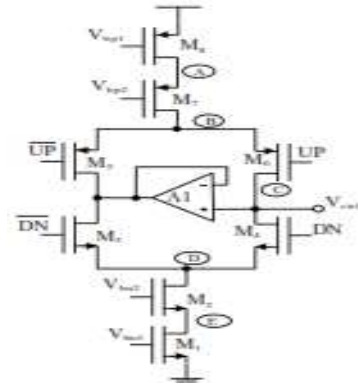


Figure 6: Proposed charge pump

B. Voltage controlled oscillator (VCO) :-

A voltage controlled oscillator generates an output signal in response to its control voltage. The frequency of the output voltage is often proportional to the control voltage. The control voltage is the output of the Loop Filter. If the control voltage rises the VCO produces an output with a higher frequency and vice versa. In the locked state control voltage becomes constant, thus the oscillation frequency of the VCO clock is also fixed.

A current starved VCO has odd number of inverter stages can be used in PLL. Here 5 stage current starved voltage controlled oscillator (CS-VCO) [2] is used it will generate a sinusoidal oscillation and last inverter is used to convert sinusoidal wave into square wave. The output node of the last inverter is connected to the input node of the first one and the schematic diagram of 5 stage CS-VCO is as shown in figure 7.

The VCO input voltage is given by,

$$V_{inVCO} = K_f \times I_{CP} \text{ -----Eq.5}$$

Where,

K_{CP} is gain of charge pump

K_f is gain of low pass filter

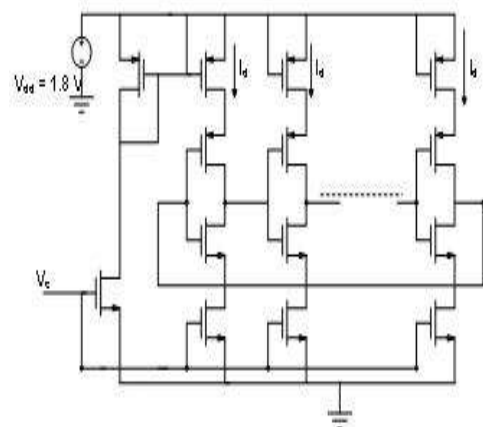


Figure 7: Conventional CS-VCO.

Frequency divider (FD):

A frequency divider is used in the feedback path to divide the output frequency of VCO and send the signal as one of the inputs to the phase frequency detector. A simple D-flip flop is used as a frequency divider.

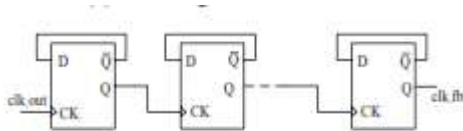


Figure 8: The frequency divider

Table 1: Design parameters

Parameters	value
Transistors W/L ratio	2um/180nm
Capacitor	10pF
Resistor	10KΩ
Number of inverters in VCO	5
Supply voltage	1.8 V

4. Proposed Set-Hardened PLL

For the PLL shown in figure 9, a transient in the output phase will be produced when nodes of the PLL are struck by Single event (SE). And, the transient in the output phase are often long enough to cause the PLL to lose lock. PFD and FD are less sensitive to SET because of their inherent digital circuit characteristics. When the signal V_{cont} is struck by SE, the PLL will have the frequency deviation and signal distortion, or even temporarily do not work. In recent years, many researches have shown that the CP is a critical module of PLL and is most sensitive to SETs.

SET on the CP causes a degradation of the output phase. The output of the CP is directly connected to capacitor of LPF, so the charge collected by capacitor will directly affect the control voltage V_{cont} of the VCO. And there is a frequency offset in the VCO, and which will cause the PLL to lose lock. Therefore, the SET on the CP will be mainly discussed here. To improve SET tolerance of the PLL, a SET-HBD-CP is proposed in this paper, as shown in figure 10.

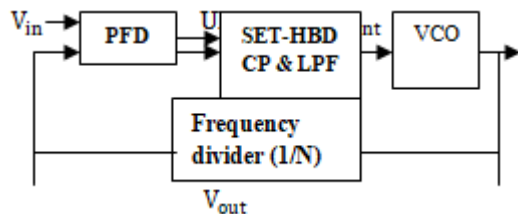


Figure 9: Proposed SET-HBD PLL

The SET-HBD-PLL is designed by adopting the proposed SET-HBD-CP instead of the conventional CP, and the architecture of the proposed SET-HBD-PLL is shown in figure 9. These modules including PFD, VCO and FD are entirely the same as that adopted in the PLL. The proposed SET-HBD-CP consists of a basic CP, a reference circuit and a radiation-hardened circuit. The basic CP shown in figure 10(a) consists of MOS transistors $M_1 \sim M_8$ and amplifier A_1 , and whose function is similar to the CP shown in figure 6.

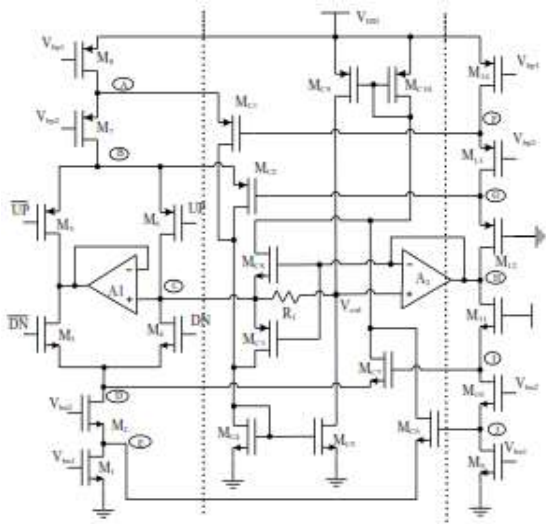
In figure 10(c), the reference circuit consists of MOS transistors $M_9 \sim M_{14}$ and amplifier A_2 , and which will provide bias voltages of the basic CP and the radiation-hardened circuit. MOS transistors M_8 and M_{14} , MOS transistors M_7 and M_{13} , MOS transistors M_2 and M_{10} , and MOS transistors M_1 and M_9 have entirely the same width-length ratio respectively. The width-length ratio of MOS

transistor M_{12} , and the width-length ratio of MOS transistor M_{11} two times that of MOS transistor M_6 is two times that of MOS transistor M_4 . Amplifier A_2 have high dc-gain and which forces the voltage V_H of node H and the voltage V_C of node C to be equal. It is concluded that $V_A = V_F$, $V_B = V_G$, $V_D = V_I$ and $V_E = V_J$. Here, $V_A, V_B, V_D, V_E, V_F, V_G, V_I$ and V_J are voltages of node A, node B, node D, node E, node F, node G, node I, and node J respectively.

As shown in figure 10(b), the radiation hardened circuit consists of MOS transistors $M_{C1} \sim M_{C10}$ and resistor R1. PMOS transistors $M_{C1} \sim M_{C3}$ will, respectively, determine whether nodes A ~ C of the basic CP are struck by SE and whether the radiation-hardened circuit starts to work. At the same time, MOS transistors $M_{C6} \sim M_{C8}$ will, respectively, determine whether node E, node D and node C of the basic CP are struck by SE Resistor R1 is adopted to isolate V_{cont} from the output node C of the CP. Therefore, resistor R1 will also restrain the SET current into the LPF and reduce the perturbation of the voltage V_{cont} . MOS transistors $M_{C4} \sim M_{C5}$ and $M_{C9} \sim M_{C10}$ form the current mirror pairs respectively. When the basic CP shown in figure 10(a) is not struck by SE, all gate-source voltages of PMOS transistors $M_{C1} \sim M_{C3}$ and NMOS transistors $M_{C6} \sim M_{C8}$ are equal to zero. Current mirror pairs $M_{C9} \sim M_{C10}$ and $M_{C4} \sim M_{C5}$ work, and the SET-HBD-PLL is in normal mode. However, when a SE strikes on the basic CP nodes, and whose voltage will increase or decrease. At the same time, all node voltages of the reference circuit shown in figure 10(c) are almost constant. These corresponding MOS transistors of the radiation hardened circuit shown in figure 10(b) will work and provide the compensation current so as to compensate the additional charge of the struck node.

For example, MOS transistor M_{C1} is turned on when a SE strikes on the drain of MOS transistor M_8 . The drain current of MOS transistor M_{C1} is mirrored by current pair $M_{C4} \sim M_{C5}$, and the drain current of MOS transistor M_{C5} will compensate the loss charge of capacitor in the LPF.

Similarly, when drains of MOS transistor M_7 and M_6 are struck by SE respectively, MOS transistors M_{C2} and M_{C3} are turned on respectively and the drain current of MOS transistor M_{C5} will compensate the loss charge of capacitor in the LPF. When drain of MOS transistors $M_1 \sim M_2$ and M_4 are struck by SE, MOS transistors $M_{C6} \sim M_{C8}$ are turned on respectively and the drain current of MOS transistor M_{C10} will compensate the loss charge of capacitor in the LPF. Then, the perturbation of voltage V_{cont} will be restrained, so PLL can quickly return to the lock state.



(a) basic CP (b) radiation-hardened circuit (c) reference circuit
Figure 10: The proposed SET-HBD-CP

5. Results & Discussion

The PFD compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase difference between the two frequencies. The PFD generates two output signals UP and DOWN as shown in figure 11(a) that switches the output current of the pump.

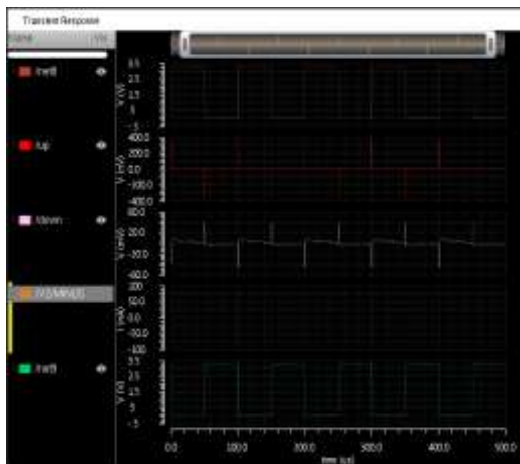


Figure 11(a): Transient response of PFD

Charge pump circuit is used to combine both the UP and DOWN outputs of the PFD and give a single output which is fed to the input of the LPF. The LPF is used to convert back the charge pump current into the voltage and the simulation result for SETCP LPF is as shown in figure 11(b) & 11(c). The output voltage of LPF controls the oscillation frequency of the VCO.

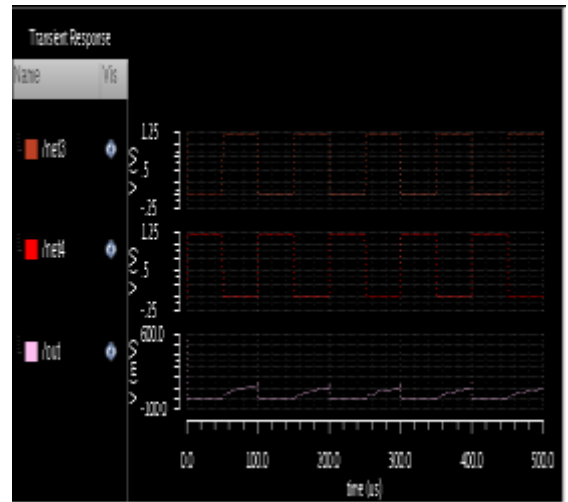


Figure 11(b): Transient response SET CP with LPF

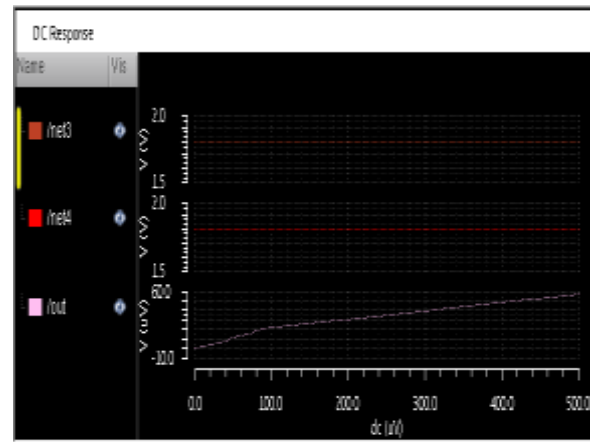


Figure 11(c): DC response SET CP with LPF

The characteristic curve of VCO is as shown in figure 11(d). The gain of VCO is given by,

$$K_{VCO} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \text{ -----Eq.6}$$

$$= \frac{1M - 0.1M}{1.8 - 1.2}$$

$$= 1.5$$

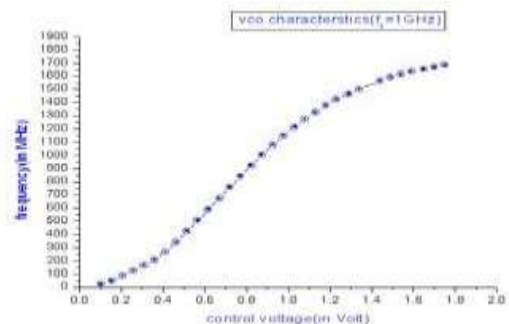


Figure 11(d): Frequency vs input voltage for 5 stage CS-VCO

The output of the VCO is fed to the frequency divider circuit. The frequency divider in the circuit forms a closed loop. Here divide by 2 frequency divider is used. The output waveform of the divider is as shown in figure 11(e)

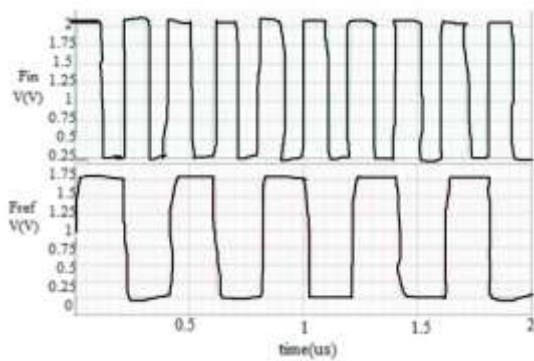


Figure 11(e): Divided by 2 Frequency divider waveform

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Table 2: Summary of PLL

Parameter	Result
Technology	180nm
VDD	1.8V
Frequency	1GHz
Power dissipation	500mW

6. Conclusion

In this paper we presented a PLL with a better lock time which is designed in cadence virtuoso 180nm technology using GPDK180 library. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values we can achieve a better lock time.

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