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PV Fed Quasi Z Source Multi Level Inverter Based DVR

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Abstract: ***This paper presents a photo voltaic fed quasi z source cascaded Multi level inverter based DVR to enhance the quality of power and to compensate the voltage abnormalities seen in the industrial and consumer premises. The Quasi Z-Source structure present in the proposed multilevel inverter performs buck/boost inversion in a single stage with a wide range of gain, assuring reliable operation against short circuit occurrence and leakage current issues faced by the series/multi string PV systems. Switching Frequency Optimal pulse width modulation for enhanced fundamental output voltage has been implemented along with constant boost control for controlling the switches of the proposed nine level inverter. The proposed synchronous reference frame control with PI controller is employed for closed loop operation of DVR to regulate the load terminal voltage during sag, swell in the voltage at the point of common coupling (PCC).The voltage injected by the proposed nine level inverter structure is able to mitigate balanced, unbalanced voltage sag, voltage swell with reduced harmonic content.***

Keywords: Quasi Z source cascaded Multi level inverter, Switching Frequency Optimal pulse width modulation, constant boost control, synchronous reference frame control.

1. Introduction

The concern towards power quality has been viewed as a serious issue owing to the sensitivity of digital computers, miniaturised process controllers involved in automated equipment, Programmable logic controllers (PLCs), adjustable speed drives and robotic systems. They are prone to failure when subjected to power quality anomalies [1] which has a direct economic impact. One of the most common power frequency disturbances is voltage sag and swell [2]. Voltage sag is a decrease to between 0.1 and 0.9 p.u. in rms voltage or current at the power frequency for durations from 0.5 cycle to 1 min caused by starting of large induction motors and utility faults. Voltage swell is an increase in rms voltage from 1.2 to 1.8 p.u. for durations from 0.5 cycle to 1 min. caused by a single line-to-ground fault, removal of bulk loads, switching on a large capacitor bank, etc. in the system resulting in a temporary voltage rise on the healthy phases [5].In order to curtail the power quality aberrations i.e. voltage sag and swell, DVR is effective owing to its faster response less than $1/4^{th}$ cycle, modular in construction, low maintenance which guarantee reliable operation with low cost among the other custom power devices. Dynamic Voltage restorer is a Static Series Synchronous Compensator (SSSC) that is connected in series with the distribution line feeder whose function is to inject or absorb the required compensating voltage so that the load voltage profile is restored at required magnitude, phase angle and frequency even when the source voltage is unbalanced or distorted. Thus the power quality is ensured by the DVR protecting the most sensitive equipments from voltage sags, swells, harmonics, unbalanced voltage and etc. [3].

The voltage source inverter is the heart of the DVR unit which converts the DC voltage into AC voltage of desired magnitude and phase injecting into the line for mitigating the voltage disturbance problem. Hence it is highly important the injected ac voltage should be clean, with minimal harmonic distortion without disturbing the operation of other equipments connected in the same distribution system. The conventional two-level PWM inverter based DVR suffers from voltage and current sharing problems, high switching losses and device rating constraints, contaminated output voltage necessitating the use of bulk filters increasing the size and cost of the entire system.

1.1 Motivation

In this paper, the two-level VSC along with its energy storage unit of the DVR structure is replaced by PV fed quasi Z source cascaded Multi-level inverter. The cascaded type unique structure paves way for utilising the distributed generators such as solar cell, fuel cell, ultra capacitors, batteries or micro-turbines for reinstituting the load voltage in the DVR operation. The modularized circuit layout without any dc link voltage unbalancing issues paves way for achieving any number of output levels with reduced harmonic content. The switching voltage stress is alleviated owing to its modularity makes the high voltage operation feasible utilising only low rated switches, promoting the rating of the inverter with reduced RFI and EMI issues.

1.2 Problem statement

1) The cascaded Multi-level inverters lack the ability of boost/buck function requiring a DC-DC converter or a transformer adding the cost and complexity of the circuit [2].
2) The leakage current issue between the PV panels and the earth remains a challenging factor indesigning a reliable CMI-basedPV system [8].
3) Reliability against short circuit occurrence is not assured.

The proposed Quasi Z source multilevel inverter is one among the alternative to solve these issues.

1) It exhibits the continuous input current, realising buck or boost inversion in a single stage processing, capable of handling a wide input voltage range for PV cell's output

which varies widely with solar irradiation and temperature.
2) It can offer low-impedance paths for the high-frequency noises solving the leakage current issue[8].
3) Comparatively with its predecessor Z source inverter, the stress of the source is alleviated, suppresses the inrush of harmonic current and switching ripples reducing the passive filter components.

2. Block Diagram

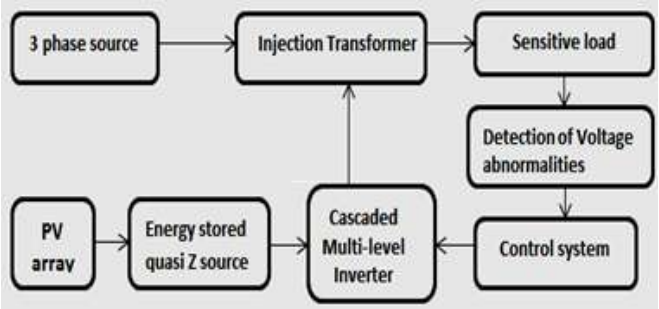

Figure 1: Block diagram representation

2.1 PV moduleas a dispersed generator

Among various types of renewable energy sources, solar energy is the most promising, pollution free cleanest energy available naturally with zero carbon dioxide emissions, and fuel disposal issues.

Table 1: PV module specificationsfor single H bridge

Name of the parameters	Parametric Notation	Value
Output power	P	250 W
Insolation	*G*	1000W/m^2
Open circuit voltage per cell	V_{oc}	0.5 V
Short circuit current	I_{sc}	8.3 A
No of cells for each module	N_s	60
Series resistance	R_s	5.1mΩ
Operating temperature	T	298 K

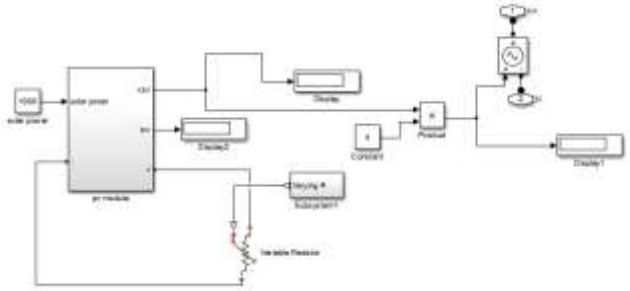

Figure 2: Simulink model of PV subsystem

The solar cellis modelled as a parallel combination of a current source with two exponential diodes, a parallel resistance Rp connected in series with a series resistance Rs in the Simulink model which is governed by the equation

$$I = I_{ph} - I_s\left(e\left(\frac{V+I*Rs}{(N*Vt)}\right)-1\right) - I_{s2}\left(e\left(\frac{V+I*Rs}{(N2*Vt)}\right)-1\right) - \left(\frac{V+I*Rs}{Rp}\right) \quad [1]$$

Where I is the output current of the PV module
$I_{ph}$is thesolar generated current
I_s and I_{s2} are the diode saturation currents
$V_t$is the thermal voltage
N, N2represent the diodeemission coefficients.

2.2 Proposed Inverter topology

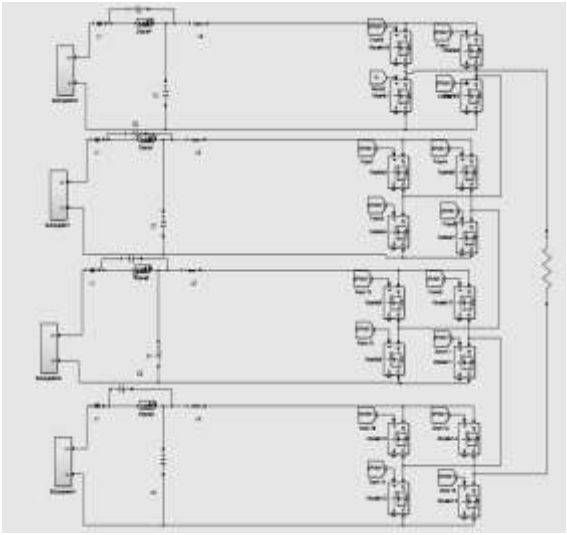

Figure 3: PV fedQuasi Z-Source Multilevel Inverter of one phase of the three phase Structure

The Quasi Z-Source Multilevel Inverter employs placement of impedance network to each H bridge PV modules shown in figure 3which modifies the operation of the circuit, allowing the shoot-through state, thereby boosting the input PV voltage, besides ensuring reliability against cross conduction of switches of same leg of the inverter. A common dc rail is present between the source and inverter, hence easier to assemble and produces less EMI problems [10].

2.2.1Circuit Analysis

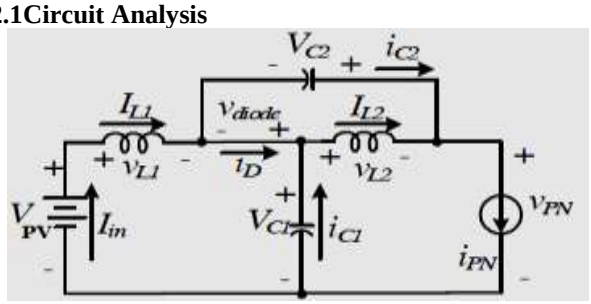

Figure 4: Equivalent circuit of the quasi ZSource Multi level Inverterin non-shoot-through state

V_{L1} = V_{PV} - V_{C1}
V_{L2} = -V_{C2}
V_{PN} = V_{C1} - V_{L2} = V_{C1} + V_{C2}
V_{Diode} = 0

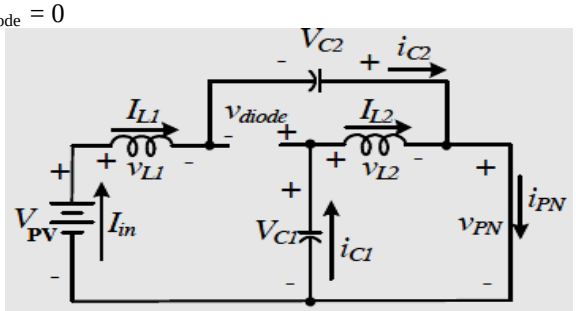

Figure 5: Equivalent circuit of the quasi ZSource Multi level Inverter in shoot-through state

$V_{L1} = V_{C2} + V_{PV}$
$V_{L2} = V_{C1}$
$V_{PN} = 0$
$V_{Diode} = V_{C1} + V_{C2}$

The performance indices for the proposed quasi z source Multi level inverter are expressed as,

Shoot through ratio, $D_o = \frac{2\Pi - 3\sqrt{3}M}{2\Pi}$

Boost factor $B = \frac{\Pi}{3\sqrt{3M} - \Pi}$

Voltage gain of the inverter $G = \frac{\Pi M}{3\sqrt{3M} - \Pi}$

Each boosted voltage from the Quasi Z Source network is connected in cascade with other boosted voltages. The boosted voltage is represented by V_{boost}. Each individual H bridge generates three levels of voltages at its output: $+V_{boost}$,0,$-V_{boost}$.Since the number of PV sources is four, the output voltage swings from $-4V_{boost}$ to $+ 4V_{boost}$with nine levels and the resulting staircase waveform is nearly sinusoidal.

Table 2: Design specifications of Quasi Z source cascaded Multi level inverter based DVR

Parameter	Notation	Value	Unit
Input PV module voltage	V_{PV}	30	Volt
Carrier frequency	f_c	10	KHz
Modulation index	M	1	-
Shoot through ratio	D	0.173	-
Boost factor	B	1.529	-
Boosted voltage	V_{boost}	45	Volt
Voltage Gain	G	1.5	
Inductors	L_1,L_2	3.5	mH
Capacitors	C_1,C_2	1000	µf

3. Control unit of DVR

In normal conditions, the dynamic voltage restorer operates in stand-by mode. However, during disturbances, nominal system voltage will be compared to the voltage variation. This is to get the differential voltage that should be injected by the DVR in order to maintain supply voltage to the load within limits.

The Modified Discrete Phase Locked Loop [PLL] is adopted for synthesising the positive sequence components of the system voltage signals and to get the (ωt) information for synchronising the control signals with the system voltage. The filtering performance of the DVR for a highly distorted and unbalanced transient network conditions is far superior compared to the conventional PLL.

The principal aim of the dynamic voltage restorer is to maintain constant load voltage at the point of common coupling (PCC) even when there is a voltage sag or swell or any other voltage disturbances. To accomplish this task, the PCC system load voltage is measured and its RMS value is calculated [12]. The Synchronous Reference Frame controller proposed in this paper computes abc to dqo transformation for the RMS value of the system load voltage transforming into the rotating reference frame. The dqo reference frame highlights the information regarding the depth (d) and phase shift (q) of voltage sag/swell with the commencement and the end time.

The dqo component voltages are computed using the equations.

$V_o = \frac{1}{3}(V_a + V_b + V_c) = 0$ [2]

$V_d = \frac{2}{3}[V_a \sin\omega t + V_b \sin(\omega t - \frac{2\Pi}{3}) + V_c \sin(\omega t + \frac{2\Pi}{3})]$ [3]

$V_q = \frac{2}{3}[V_a \cos\omega t + V_b \cos(\omega t - \frac{2\Pi}{3}) + V_c \cos(\omega t + \frac{2\Pi}{3})]$ [4]

If there are any voltage anomalies, then it would be reflected in the dq components of voltage by comparing it with the reference set voltage. And so an error signal will be generated. The PI controller parameters K_p and K_i works on this feedback signal to control the stability of the system. The PI controller response is again transformed back into the stationary frame to yield V_a,V_b,V_c quantities using equations [4],[5],[6] based on dq to abc transformations. These quantities represent the reference signals for the proposed PV fed Quasi Z source cascaded Multi-level inverter section of the DVR unit.

$V_a = V_d \sin\omega t + V_q \cos\omega t + V_o$ [5]

$V_b = V_d \sin(\omega t - \frac{2\Pi}{3}) + V_q \cos(\omega t - \frac{2\Pi}{3}) + V_o$ [6]

$V_c = V_d \sin(\omega t + \frac{2\Pi}{3}) + V_q \cos(\omega t + \frac{2\Pi}{3}) + V_o$ [7]

The technique selected in this work isconstant frequency Switching Frequency Optimal Phase Opposition Disposition Pulse Width Modulation for increasing the fundamental magnitude of the inverter output voltage waveform. This is better than conventional phase-shifted multi carrier PWM as it provides better quality of voltage with reduced harmonic contents and switching losses. It is effective compared to hysteresis current control, linear current control which are limited to low power levels. Moreover the proposed logic circuit for DVR action is simple and flexible.

3.1 Switching frequency Optimal PWM along with constant boost control

First the instantaneous average of the maximum and minimum of the three reference voltages (V_a, V_b, V_c) is calculated from which the individual reference voltages are subtracted to obtain the third harmonic modulating waveform with a 15% increase in modulation index for each of the phases.

The governing equations for this switching strategy is as follows,

$V_{offset} = \frac{\max(Va + Vb + Vc) + \min(Va + Vb + Vc)}{2}$ [8]

$V_{a\,SFO}^{*} = V_a - V_{offset}$ [9]

$V_{b\,SFO}^{*} = V_b - V_{offset}$ [10]

$V_{c\,SFO}^{*} = V_c - V_{offset}$ [11]

The inverter fundamental output voltage is increased to 112% without compromising on the quality of the output waveform and emulation of Space Vector Pulse Width Modulation (SVPWM) highlights the merits of this strategy.

Thedesired modulating reference waveform is mathematically expressed in time domain as follows,

$V_{a\,SFO}^{*}(t) = 1.12V_m [\sin\omega t + 0.1666\sin 3\omega t]$ [12]

$V_{b\,SFO}^{*}(t) = 1.12V_m [\sin(\omega t - 120°) + 0.1666\sin(3(\omega t - 120°))]$ [13]

$V_c^*{}_{SFO}(t) = 1.12V_m [\sin(\omega t + 120°) + 0.1666\sin(3(\omega t + 120°))]$[14]

This third harmonic injection along with constant boost control for insertion of shoot through state is utilised for achieving maximum boosted voltage, reduced voltage stress while keeping the shoot through duty ratio constant [8-10].The SFO modulating signal is further compared with eight carrier waveforms which are placed above and below reference levels to generate the nine level inverter. Positive pulses are produced for generation of positive voltage level whenever the amplitude of reference modulating signal is greater than the amplitude of carrier wave for switching on the active devices. Similarly when the reference wave is lesser than the carrier wave, negative pulses are produced for creation of negative voltage level.

Table 3: DVR system parameters

Electrical Distribution grid	
Rated line-to-line voltage	440 V
Frequency	50 Hz
Distribution Grid impedance	
Resistance,R_s	11 mΩ
Inductance,L_s	0.6 mH
Sensitive load	
Resistance,$R_{sensitive}$	20 Ω
Inductance $L_{sensitive}$	50 mH
Injection transformer	
Rated apparent power,S	10 KVA
Rated voltage windings	440 V/440 V
Winding resistance R_w	0.6Ω
Leakage inductance L_w	2.8 mH
Output filter	
Filter inductance (L_f)	9.6 mH
Filter capacitance (C_f)	250 µf
SRF based PI controller	
PI controller	K_p = 0.005; K_i =500

3. Simulation Results and Discussions

Figure6 shows the Simulink model of proposed PV fed Quasi Z source Multilevel inverter based DVR with its synchronous reference frame control for closed loop operation.

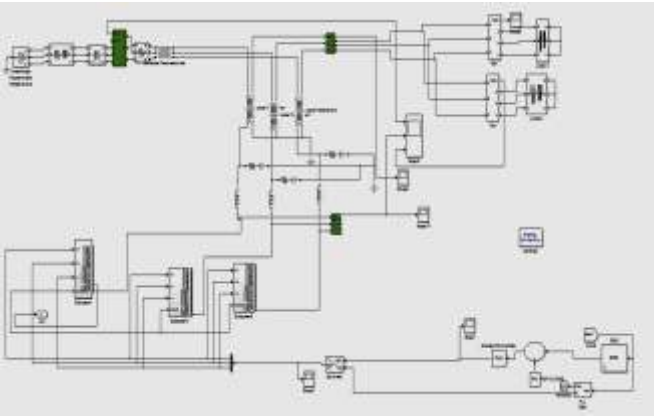

Figure 6: Simulink model of proposed PV fed Quasi Z Source Multilevel inverter based DVR

Figure 7illustrates the third harmonic injected modulating signal along with the high frequency carrier waves using the Switching Frequency Optimal PWM.

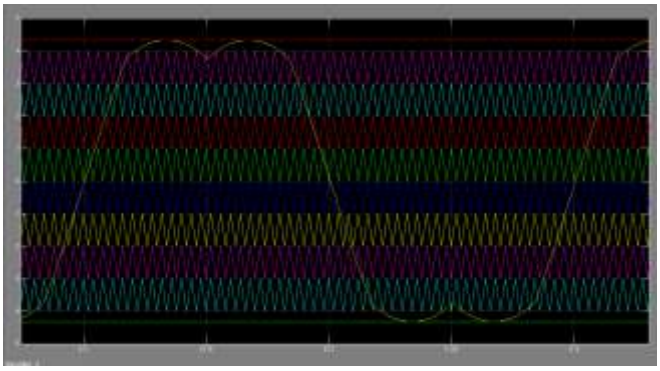

Figure 7: Switching frequency optimal PWM control along with constant boost controlscheme

Figure8 shows the stepped nine level output waveform of the proposed PV fed Quasi Z source Multilevel inverter.

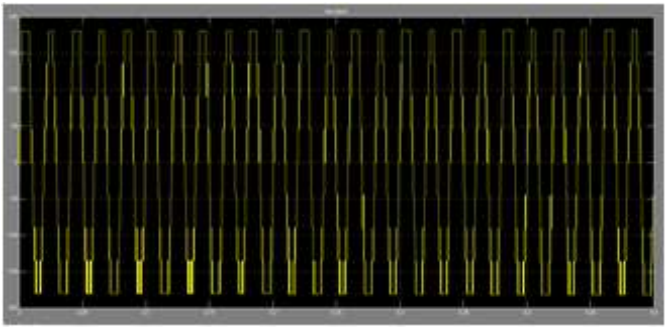

Figure 8: Generation of nine level output waveform of the proposed PV fed Quasi Z source Multi level inverter

4.1 Single voltage sag mitigation for balanced supply

Figure 9 shows creation of single voltage sag from t=5ms to 1ms for a duration of 5ms.The DVR with its closed loop control reacts to this voltage abnormality and injects the desired voltage magnitude to the PCC both in phase and magnitude using the proposed PV fed cascaded multilevel inverter. The load voltage is maintained constant irrespective of voltage sag aberrations and sensitive load equipments are protected.

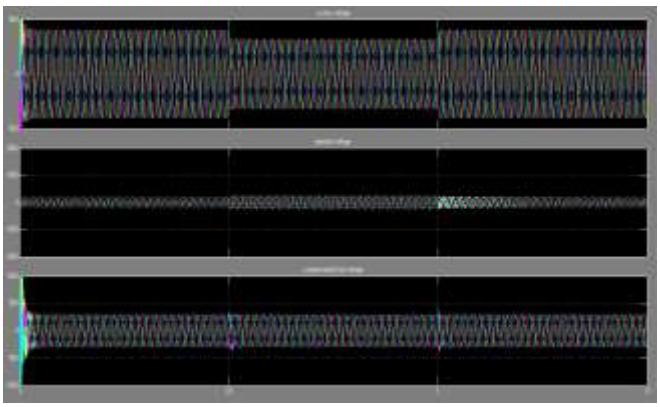

Figure 9: DVR response tosingle voltage sag for balanced supply (a) supply voltage,(b)DVR injectedvoltage, (c) load voltage.

4.2 Balanced Multiple Voltage sag mitigation

Multiple voltage sags for a balanced voltage supply about 20% and 40% are created at t= 0.5 sec for a durations of 0.2

seconds and at t= 1.1ms for a duration of 0.3 ms. The proposed control method is able to drive the DVR to compensate for these multiple balanced voltage sags.

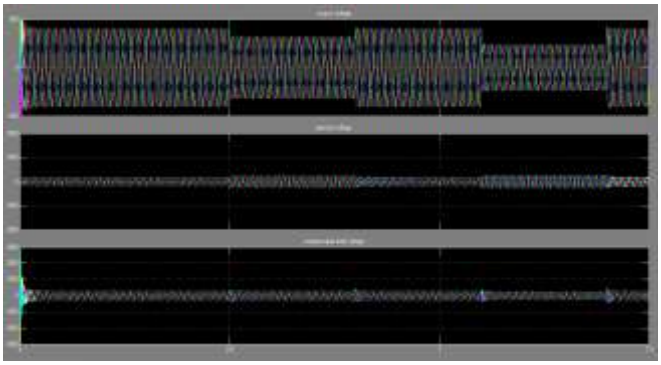

Figure 10: DVR response to multiple voltage sag for balanced supply (a) supply voltage, (b) DVR injected voltage, (c) load voltage.

4.3 Unbalanced Multiple Voltage sagmitigation

Only in one phase of three phase voltages, for example R phase multiple voltage sags of about 20% and 40% are created at t= 0.5 ms for a durations of 0.2 ms and at t= 1.1ms for a duration of 0.3 ms. The proposed PV fed Quasi Z source multilevel inverter based DVR is able to cope these unbalanced voltage disturbances and maintain the constant PCC voltage, thereby protecting the critical equipments.

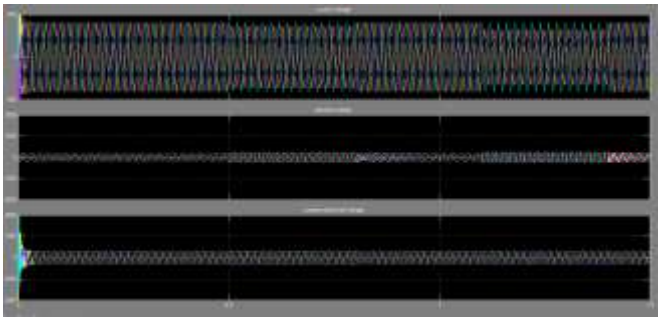

Figure 11: DVR response to unbalanced multiple voltage sag for balanced supply (a) supply voltage, (b) DVR injected voltage, (c) load voltage.

4.4 Balanced Single voltage swell mitigation

Figure 12 depicts the voltage swell creation from t=5ms to 1ms for duration of 5ms.The DVR handles these voltage abnormalities much faster and maintains the constant load voltage.

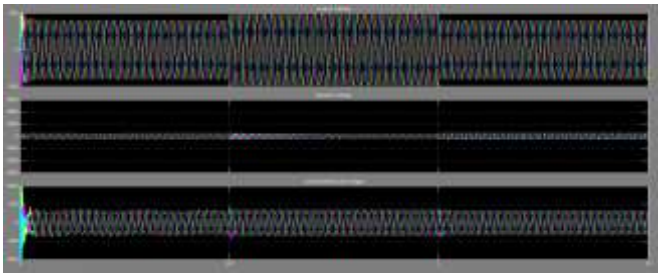

Figure 12: DVR responseto Single voltage swell for balanced supply(a) supply voltage,(b)DVR injectedvoltage, (c) load voltage.

4.5 Balanced voltage sag and swell mitigation

The DVR is tested for its dynamic response by creating voltage swell and sag at t=0.5 sec and t= 1 sec. The proposed DVR detects these voltage anomalies and with its synchronous reference control strategy mitigates these voltage disturbances which is shown in figure 13.

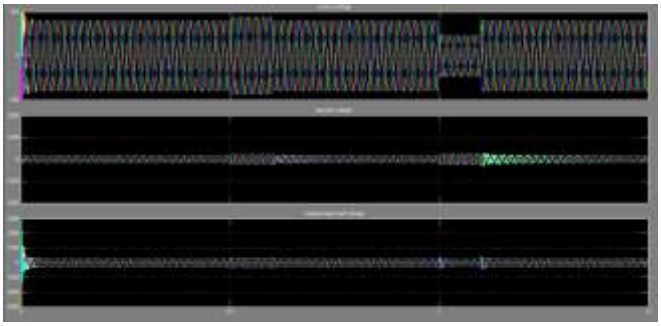

Figure 13: DVR dynamic response to balanced voltage sag and swell (a) supply voltage,(b)DVR injectedvoltage, (c) load voltage.

4.6 Unbalanced voltage sag and swellmitigation

The DVR is again tested for unbalanced voltage sag and swell conditions. The proposed DVR is able to manage these unbalanced voltage aberrations and reinstitute a constant load voltage with desired magnitude, phase and frequency.

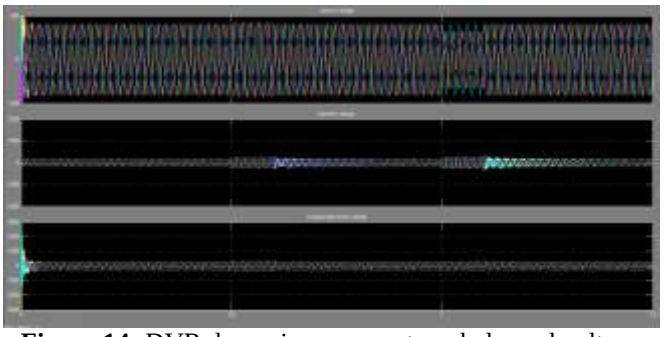

Figure 14: DVR dynamic response to unbalanced voltage sag and swell (a) supply voltage,(b)DVR injectedvoltage, (c) load voltage.

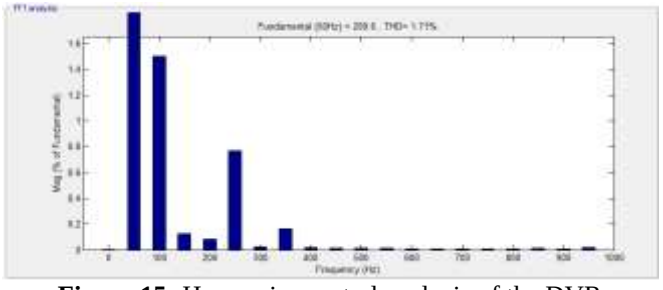

Figure 15: Harmonic spectral analysis of the DVR compensated system

The FFT analysis shown in figure 15 shows the effectiveness of the proposed PV fed quasi Z source nine level inverter producing only 1.71% in the line voltage of the system voltage which is well below the IEEE standard harmonic limits.

4.7 Harmonic mitigation

A non- linear load is simulated and inserted at about t=0.7 sec for a duration of 3 seconds in the sensitive distribution feeder which is shown in figure 16. An abrupt change in voltage and harmonic distorted waveform is observed. The proposed DVR is able to handle these power quality disturbances and maintains the constant PCC voltage with a THD of 2.01% meeting the IEEE standard harmonic limits which is illustrated in the FFT analysis shown in the figure 17.

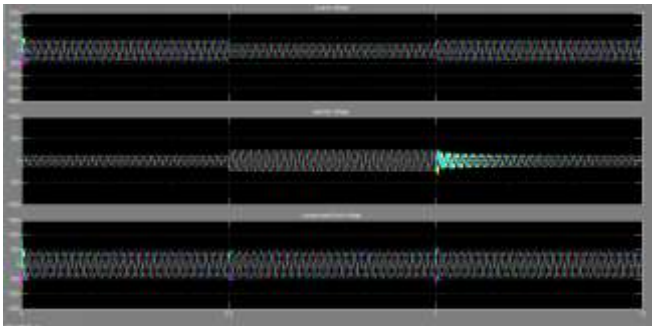

Figure 16: DVR response to harmonic injected non-linear load (a) supply voltage, (b) DVR injected voltage, (c) load voltage.

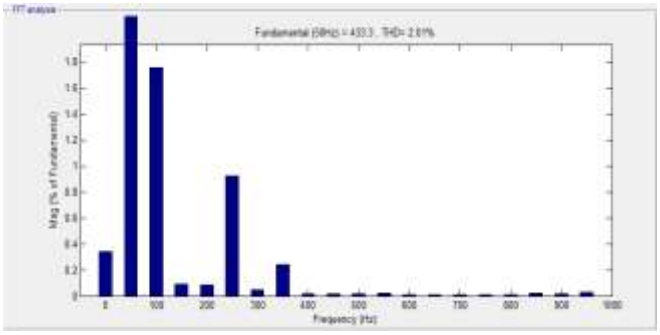

Figure 17: Harmonic spectral analysis of the DVR compensated non-linear load

4. Conclusion

This paper has proposed an energy stored Quasi Z source Multi level inverter for curtailing the intermittent and stochastic characteristics of photovoltaic system to be effectively used for DVR operation. The synchronous reference frame control theory is effectively utilised for reinstituting the constant load voltage at the PCC. The performance of DVR is studied under voltage sag/swell and in presence of nonlinear loads and the simulation results prove the dynamic voltage restoration property mitigating the PQ disturbances achieving excellent voltage regulation. The THD was found to be 1.71% for linear loads in the PCC voltage which is well below IEEE standards thus enhancing the quality of power.

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