International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2016): 79.57 | Impact Factor (2017): 7.296

A Dynamic Threshold MOS Logic Based Low Power 8-Bit Pipe Line ADC for Wireless Communications

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Abstract: ***The Most necessary units in wireless communication applications, Broadband transceivers are.Low power and high performance data converters. Therefore the data converters must have less power dissipation, high sampling rate, and resolution. This paper presents a design with low power and high conversion rate Pipe line architecture ADC. The major sub circuits in this design are subtractor, residue amplifier and comparator. These threedevices are developed by using Operational. The designed ADC consists of 8 single bit ADCs, i.e. each stage having 1-bit resolutions, which are designed by using Cadence virtuoso with 180nm technology. The Pipeline architecture and Opamp works with 1.8V supply voltage, and the power dissipation is 11mw.***

Keywords: ADC, Low power, residue amplifier

1. Introduction

An Analog-to-Digital converter is a device, which translates an analog voltage signal into a corresponding digital number. Whenever we relate to the real world most of the signals are analog in nature. But some applications such as digital signal processing requires signals to be digital. In such situations it becomes necessary to get analog to digital conversion using an ADC. Analog-to-digital converter is a fundamental block in mixed signal VLSI circuits [1]. ADC is the key components in communication and video system. With development of these electronics system, high resolution and high-speed ADCs are becoming more and more important. High-speed power efficient Analog-to-Digital converters (ADCs) are the critical building blocks for modern communication and signal processing systems. They are the interface between the analog and digital signal processing. Since the mid-1970s, ADCs have been widely designed using integrating, successive approximation, flash, and delta-sigma techniques. More recently, there has appeared a new class of ADC with an architecture known as pipeline, which offered an attractive combination of high speed, high resolution and low power dissipation. The pipeline ADC, therefore, became the optimum solution for present low power applications, such as a wireless communication system. A continued search for circuit architectures and techniques enabling ADCs to obtain higher speed and resolution with smaller chip area and lower power dissipation, therefore, is necessary. Pipeline analog-to-digital converters represent the majority of the ADC market for medium to high resolution ADC.

2. DTMOS Technique

The technique behind the dynamic threshold MOS is that the input voltage V_{bs} is greater than Zero for NMOS and for PMOS it is negative and hence the threshold voltage can be reduced accordingly. The DTMOS structure uses both the gate and the body terminal to provide the signal input. Since in DTMOS both the gate and the body terminal are shorted V_{bs} become the function of the input signal which is applied to the gate terminal thus $V_{bs}=V_{gs}$is maintained. Due to dynamic body bias, potential in the channel region is strongly controlled by the gate and body terminals, leading to a high trans-conductance owing to faster current transport. The relation between input signal and V_T is described using the following equation

$$V_{T0} = 2\phi_B + V_{FB} + \frac{\sqrt{2q\varepsilon s Na(2\phi B)}}{Cox}$$

Where VFB is the flat band voltage and ϕB is the inversion layer voltage the inversion layer potential, Na is the channel doping, εs is the Si permittivity, q is the electron charge. Considering body biasing, VT is given as

$$V_T = V_{T0} + \gamma(\sqrt{\Psi s + VBS} - \sqrt{\Psi s})$$

$$\gamma = \frac{\sqrt{2q\varepsilon s Na(2\phi B)}}{Cox}$$

and VT is threshold voltage due to body effect. The DTMOS transistor and its small signal model is shown in Fig.1.and Fig.2 it has two transconductances, the gate tranconductance (gm) and body transconductance (gmb).

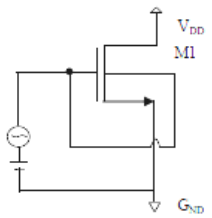

Figure 1: DTMOS Transistor

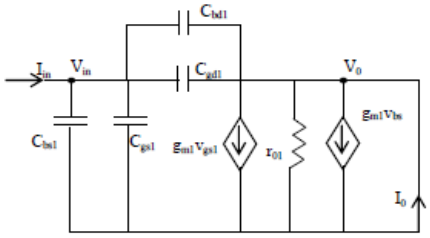

Figure 2: Small signal model of DTMOS Transistor

Pipelined Analog-to-Digital Converter is an architecture which offers the attractive combination of low power dissipation, high resolution and high speed. Hence the Pipelined ADC is an optimum solution for low power applications like wireless communication systems. The CMOS IC technology is widely for digital and analog applications. Pipeline architecture allows digital gain calibration, power minimization and also digital error correction through capacitor scaling. Hence, for high resolution and high speed application Pipeline ADC is suitable.

3. Operational Amplifier

To design pipelined ADC, the basic block required is Operational Amplifier [3]. The op-amp is designed using gpdk180 nm technology with 1.8V power supply. This is a two stage op-amp, where first stage is differential amplifier and the second stage is CS-amplifier to control the gain. The schematic is shown in the fig. 3.

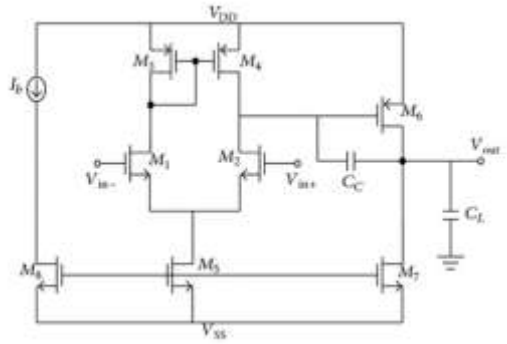

Figure 3: Operational Amplifier

4. 8-bit Pipelined ADC

The operating principle of the pipeline ADC is multi-stage conversion [4]. Each pipelined stage realizes the digital quantization, the analog to digital conversion, computing and amplifying the residue voltage. The architecture design of the pipelined ADC is flexible. The distribution of stage resolution is complex and important. For one bit per stage, the offset voltage requirements of the comparator ADC is relax, and the conversion speed of the stage is faster. The noise and errors introduced by the later stages influence the overall conversion accuracy.

In this paper, the pipelined ADC architecture is shown in Fig.4, with 1 bits/stage. The ADC also includes the dedicated sample and hold circuit, Optimized comparator, subtractor, residue amplifier, and switch architecture is adopted to further reduce the power dissipation based on high speed and high resolution [1].

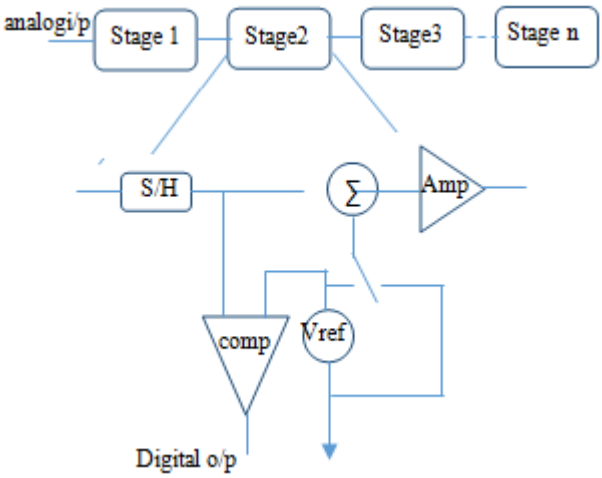

Figure 4: Architecture of the Pipelined ADC

5. Pipelined ADC Blocks

5.1 Sample and Hold

The Sample and Hold circuit creates the samples of voltage given to it as input, and after that, it holds these samples for the definite time [11]. The time during which sample and hold circuit generates the sample of the input signal is called sampling time**.** Similarly, the time duration of the circuit during which it holds the sampled value is called holding time**.** This block allows the samples of input analog signal at the required rate. The Figure 5 shows the sample and hold circuit

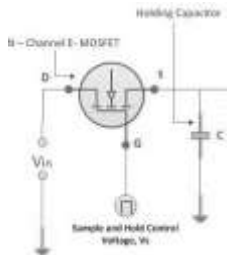

Figure 5: Sample and Hold circuit

5.2 Comparator

The op-amp is used as a comparator with one of the input as sampled analog signal and the other input as reference voltage. It is a 1 bit analog to digital converter. If the input to the non-inverting input is greater than that to the inverting input, the output is a logical 1. If the input to the non-inverting input is less than that to the inverting input, the output is a logical 0. We thus have the key element for asking "is the signal above or below a threshold level?" We will use comparators in EVERY analog-to-digital converter to detect analog thresholds.

5.3 Subtractor

In pipeline architecture subtractor circuit is used to subtract the sample and hold's output and transmission gate switch output. And output of subtractor is given to the residue amplifier. The schematic is shown in the fig. (6).

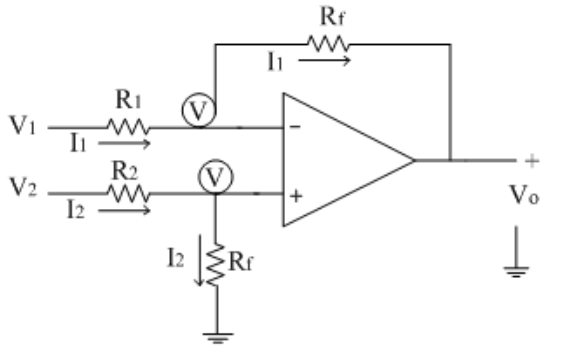

Figure 6: Subtractor Circuit

5.4 Residue Amplifier

In pipelined architecture, the residue amplifier is used to get the required amount of gain. It is used to increase the gain of the degraded signal The schematic is shown in the fig. (7).

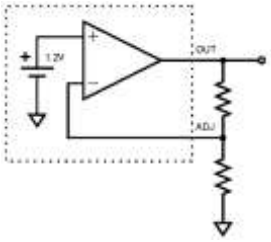

Figure 7: Residue Amplifier**c**ircuit

5.5 Switch

The transmission gate is modified by stacking the transistors as shown in Fig 8- to obtain the original signal without any loss. The stacking of transistors improves the aspect ratio, performance and ON resistance. Thetransistor widths are maintained in the ratio 1:2 for NMOS to PMOS.

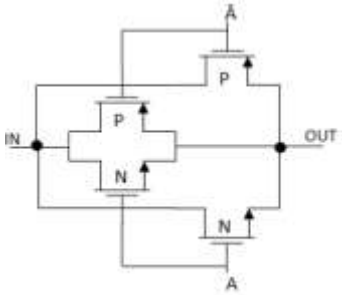

Figure 8: Schematic of Switch

The performance varieslargely because of stacking as the variation almost doubles with two fingers than that of a singletransistor.

6. Measured results

The ADC was designed in 0.18µm CMOS technology. The total power dissipation is 5mWwith a single 1.8V power supply at 10MS/s.The differential nonlinearity (DNL) and the integralnonlinearity (INL) of the ADC were measured, DNL iswithin ±0.3LSB and the INL is within ±1.3LSB, which isenough for the ADC.

For The 8-stage pipeline ADC simulated output Waveforms are depicted below. When an input is 1.8V, reference voltage (Vref) is 500mv waveform for this is shown in fig 9. Power dissipation is 11.mW with a conversion rate of 10MS/s.

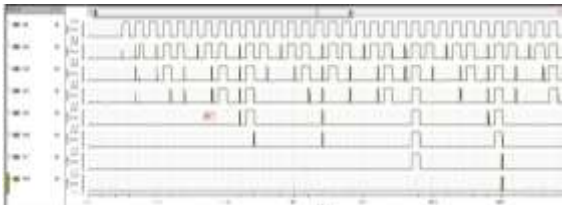

Figure 9: Simulated wave forms of 8-bit pipeline ADC

7. Conclusion

A 8bit 10MS/s pipelined ADC which exploits high performance devices with low power dissipation has been presented in this paper. We presented a simplified architecture with DTMOS technique which don't influence the performance of the ADC. We also designed a high performance low power Op-Amp with high gain, bandwidth and slew rate. We introduced the DTMOS in the Op-Amp to further reduce the power dissipation.

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