International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2016): 79.57 | Impact Factor (2015): 6.391

A Brief Review on CDMA Systems for Ad-hoc Network

Ruchi Agrawal[1], Ekata Patil[2]

[1]M. Tech Student, CCEM, Raipur, Chhattisgarh, India

[2]Assistant Professor, CCEM, Raipur, Chhattisgarh, India

Abstract: ***In this paper, we have presented a brief review on the use of Spread Spectrum technique in the field of Ad-hoc networking. Various studies have revealed that Spread Spectrum technique is appropriate for ad-hoc networking because of its tremendous advantages such as security, interference robustness, capacity enhancement etc. Direct Sequence Spread Spectrum CDMA is a type of spread-spectrum communication system in which multiple signal channels share the same frequency band. They are distinguished by the use of different spreading codes known as Pseudo random codes. The Direct Sequence CDMA is one of the most promising medium access technology which is expected to play a vital role in the upcoming communication systems due to its robustness and higher capacities. A brief review of different systems employing different methodologies has been discussed in this paper. A DS-CDMA transmitter and receiver with BPSK modulator and demodulator has been implemented in previous works. On the other hand some of them makes use of Frequency Hopping as the Spreading technique. Others employ the use of Gold codes and others as the spreading sequence. The use of these techniques and their disadvantages has been discussed briefly.***

Keywords: DS-CDMA, Ad-hoc, Spread Spectrum, BPSK

1. Introduction

An Ad-hoc network is a decentralized type of wireless network. An ad hoc network is so called because it does not depend on any pre-existing infrastructure (or access point), such as routers in wired networks or access points in managed wireless network. Ad hoc networks has been a topic of interest for researchers in the domain of wireless networking since a long time. Due to the absence of any centralized infrastructure, these networks have to be self organized and self configured. The popularity of Ad hoc networks has led its applications to not only the military or wireless sensor networks, but also to other exciting applications like community broadband access. This wide application of ad hoc networking requires more and more efficient technologies for the development of its devices.

One of the promising technologies that has been studied for a few years is the Spread Spectrum technology. It permits interference averaging and tolerate co-located simultaneous transmissions. A Spread Spectrum system is often referred as Code Division Multiple Access. It is used world wide in communication systems involving interference challenges such as cellular and cordless telephones, military applications and GPS. Spread Spectrum technique has been considered good for ad hoc networks since a long time because of the tremendous advantages offered by it. Some of them include security and interference robustness.

A Direct Sequence Spread Spectrum CDMA based transmitter and receiver can be realized for an ad hoc network by spreading the user data using a PN Sequence which is unique for each user. The users share the same band of frequencies using the entire allocated spectrum without any time slot distribution. This is possible since the users have differ in the spreading sequences. This property of DS-CDMA adds to its numerous advantages for use in ad hoc networks. Other factors include increased number of users with no sharp upper bounds, retrieving benefits from the inactive terminals in the network and higher network efficiency. Furthermore, these systems exhibit resistant to interference, interception, and frequency-selective fading.

The Code Division Multiple Access transmission method has been a popular choice for the early ad hoc network protocol standards such the IEEE 802.11 standard.

2. Problem Statement

A major drawback with present systems is the use of microprocessors, like an Application Specific Integrated Circuit (ASIC). These chips are very expensive and take a long time to market. FPGA does not have a fixed hardware structure so it has to be defined by the user. This is done by determining the interconnections between the logic cells in the FPGA and the functions performed by them. So operations of FPGA are not predefined. We can have the processes done according to the written HDL code "in parallel" which means simultaneously.

Any node of an ad hoc network receives only one packet at a time. If multiple packets arrived at the receiver simultaneously, they will be discarded because of collision. So, packet collision among uncoordinated transmitters is the key factor limiting the throughput of an ad hoc network. To greatly promote the throughput of an ad hoc network, we need to break this bottleneck, i.e., let node be capable of receiving multiple packets simultaneously. To implement this goal, signal processing techniques can be used to separate mixing packets. . If ad hoc network uses DS-CDMA in its physical layer, the separation of mixing packets becomes comparatively easy, because deterministic pre-allocated signature code for each node can be used to extract expected packet from mixing data.

Present systems use BPSK as the modulation technique in which one bit is carried by one single analog carrier. Hence data rate in bits per second is same as the symbol rate. As compared to other modulation techniques such as QPSK, the data rate achieved is just half. Infact it is many times less as compared to other higher modulation techniques such as 16QAM, 64QAM etc. Due to this reason, BPSK is not bandwidth efficient modulation technique compared to other modulation types.

3. Literature Survey

Sreedevi, B., et al. in their paper [1] titled, "FPGA implementation of DSSS-CDMA transmitter and receiver for ADHOC networks." presented a Direct Sequence principle based CDMA transmitter and Receiver for a single user transmitting single bit data. The transmitter section described in this paper mainly consists of a block for symbol generation, PN sequence generation, spreading of data and BPSK modulation of spread data. The receiver section described in this paper consists of blocks for demodulation of received signal, matched filter, PN sequence generation and threshold detection. To generate the carrier signal at transmitter and receiver, a Direct Digital Frequency Synthesizer (DDFS) principle is employed. The receiver gets its input and recovers the data using matched filter. The tool used for functional simulation and logic verification is Model Sim Xilinx Edition 5.8 (MXE). The synthesis of transmitter and receiver on FPGAs is done using Xilinx Synthesis Technology (XST) of Xilinx ISE tool. Applications of the developed CDMA system for ADHOC networks and defense communication links were studied in this paper.

Ullah, M. Habib, Akhmad Unggul Priantoro, and M. Jasim Uddin. In their paper [2], titled "Design and construction of direct sequence spread spectrum CDMA transmitter and receiver.", presented the design and construction of a CDMA transmitter and receiver based on the Direct Sequence Spread Spectrum principle. The paper also describes the features of Spread Spectrum system and its advantages in using it in the communication systems such as CDMA.
This paper also presents the use of a BPSK modulator and Demodulator but with a different approach to its design. The design and simulations are based on the use of ideal components. In BPSK modulation the phase of the carrier signal is changed whenever the incoming bit changes its state. For example, if the incoming signal changes state from 0–1, the carrier changes its phase by +180°, and if it changes its state from 1–0 the carrier changes its phase by -180°. The BPSK modulator is designed using two inverting Op-amps with the gain 1, two analog switches and one inverter. The switches are controlled by the data. This paper described the design of the modulation technique of direct sequence-spread spectrum with its hardware implementation. It also describes the characteristics of BPSK modulator. In this paper a comparison of circuit's output characteristics and the BPSK modulated signal's characteristic has been done and it has revealed that some faults exists. The amplitude of the observed output is not found to be uniform all along. Sudden jumps were observed in the output wave shape. The cause of these jumps may be non uniformity in manufacturing of the integrated circuits.

Kakade, Vaibhav K. in his paper [3], titled, "Implementation of DS-CDMA Transmitter and Receiver in VHDL for FPGA." presented a design and implementation of a DS-CDMA transmitter and receiver for a single user. It represents the use of a 4-bit PN sequence for a single user transmitter and a single user receiver. The 4 bit PN sequence will no longer be useful if we increase the number of users, since it will not provide the level of security required in the case of multiple users. This paper also describes the advantages of using CDMA over FDMA and TDMA in today's communication systems. A BPSK modulator and demodulator has been used for modulation and demodulation of the spread signal. Direct Digital Frequency Synthesizers (DDFS) are used for generating the Look-Up Tables (LUT) for modulation. An oscillator is used at the receiver to multiply the BPSK modulated signal with the locally generated carrier. After this, a Low Pass Filter gives the low frequency components only. A decision device then approximates the signal to a binary sequence which is the spread sequence of the data signal. The most sensitive part of the DS-SS receiver is the synchronization of the locally generated PN sequence and the sequence obtained from the decision device . If even a single bit mismatch occurs, it may lead to noise instead of the data signal.

Ahmad, Bilal, Malik Junaid Aziz, and Syed Asfandyar Gilani., in their paper [4], titled, "Design and Implementation of Frequency Hopping using Hardware Descriptive Language." presented a new design and implementation of a prototype for Frequency Hopping Spread Spectrum in Verilog HDL. The paper describes that the benefit of using Verilog HDL is that, instead of buying expensive circuits, a programmable FPGA can be chipped to reduce the cost. This paper describes the benefits of using FPGA for the development of a transmitter based on the spread spectrum principle. To obtain the spread spectrum, the technique used here is Frequency Hopping Spread Spectrum. Since FPGAs are used, the system is designed according to the required algorithm without concerning the hardware implementation. In this paper, the biggest problem is that Verilog does not support analog waves as well as negative values. For the efficient implementation of modulation, it is essential to generate real analog waes (sine and cosine). This leads to a complex solution of generating and maintaining a Look Up Table (LUT). This paper mainly describes the tremendous advantages of using an FPGA as compared to the traditional chips. The programming language used is Verilog HDL (Hardware Descriptive Language) which is a language used to describe a digital system.

Banerjee, Subhasish, et al., in their paper [5], titled, "ASIC Implementation of CDMA Transmitter using VHDL." presented the design of a CDMA based transmitter. The paper describes the design of a transmitter consisting of blocks for the PN sequence (Gold code) Generation, Modulator etc. The modulation used here is BPSK. The gold code is generated by using two different maximal length sequences of the same length (2^n-1). The exclusive or of

these two sequences gives the Gold code of length (2^n-1). Though the Gold codes have better cross-correlation properties than the maximal length sequence, but it requires excessive amount of hardware to implement it. This fact renders gold code less useful than maximal length sequences. This increased amount of hardware is not necessary for a simple design. This kind of design is not suitable where cost is a major concern. Also, using a Maximal Length Sequence instead of a Gold Code does not really compromise with the security of the system. It can be used in systems where cost is more concerned compared to security.

Gupta, Ashutosh, et al. in their paper [6], titled, "Performance analysis of different PN sequence and Orthogonal Spreading sequences in DS-SS.", presented, a comparative analysis of different PN sequences. The paper described the features of Direct Sequence CDMA and discussed the orthogonal codes. It presents a comparative analysis of different short codes such as Barker, Hadamard, Kasami on the basis of BER measurement.The codes are executed and compared with PN code length of 64 bit and 128 bit and it concludes that the bit error rate of barker code is better than that of other codes. But considering the simplicity of the design of transmitter and receiver for ad-hoc networks, a maximal length sequence can also be used without much compromise in the probability of error or Bit error rate. The paper also describes about Pseudo-noise sequence and explains about the complete block diagram of DS/SS transmitter and receiver system and their specification needed.

Memon, Tayab D., Walliullah Ghangro, and B. S. Chowdhry, in their paper [7], titled, "Quadrature phase shift keying modulator & demodulator for wireless modem." presented, the design of a Quadrature Phase Shift Keying (QPSK) modulator and demodulator. The model has been developed in Matlab and simulated using Simulink. This paper describes the major advantages of using a QPSK modulation in present systems. The paper gives a brief review of Digital Modulation and Quadrature Phase Shift Keying (QPSK). It then discussed the block diagrams for QPSK modulation and demodulation and presented the simulation of them in Matlab Simulink. The paper proposed a hardware implementation of the represented model.

Popescu, S. O., A. S. Gontean, and D. Ianchis., in their paper [8], titled, "QPSK modulator on FPGA." presented, the theoretical backgrounds of a QPSK Modulation. The tool used for simulation of the model is Matlab / Simulink. The model is developed in VHDL language and implemented on an Spartan 3E Starter Kit board by synthesizing it with Xilinx ISE 12.3. The paper proposes the implementation of the QPSK modulator in System Generator. The paper aims at the design of a simple but robust form of digital modulation that is Quadrature Phase Shift Keying (QPSK). This kind of modulation is very popular in satellite communication since it conveys 2 bits per symbol.

Andrews, Jeffrey G., Steven Weber, and Martin Haenggi, in their paper [9], titled, "Ad hoc networks: to spread or not to spread?" presented, the advantages and disadvantages of CDMA as an appropriate design approach for wireless ad-hoc or mesh networks. The paper mentions that the interference averaging effect of CDMA is not appreciable in ad hoc networks. The advantages of Spread Spectrum mentioned in the paper are that they allow for longer hop distances. The advantages of spread spectrum for ad hoc networks dominate the minor disadvantages and hence prove to be suitable for ad hoc networks. The paper carefully scrutinized the supposed advantages and concludes that the advantages of CDMA in ad hoc networking are different than those in cellular communications and may differ for the two different types of CDMA i.e., FHSS and DSSS. The main advantages stated in this paper are Longer hops, Capacity enhancements, Network efficiency, Increased Security etc. This paper consists of a modern overview of CDMA with brief discussions on Frequency Hopping and Direct Sequence Spread Spectrum. The paper presents the key features of a CDMA ad-hoc network which include Capacity or throughput, Interference range and others.

Channe, Gaurav P., and C. N. Bhoyar, in their paper [10], titled, "VHDL Design of W-CDMA DS-SS System using Gold Code.", presented, the design of a DSSS system using Gold code as the spreading sequence. In this project DSSS principle based code division multiple access transmitter and receiver is designed in VHDL for FPGA. The transmitter section consists of blocks of data generator, PN sequence generator, and direct digital frequency synthesizer (DDFS) and modulator. The receiver section consists of demodulator, PN sequence generator, matched filters and threshold detector blocks. The modulation used here is Binary Phase Shift Keying (BPSK). The functional and logic verification of each block is done with the Model Sim Altera 13.1 tool. The synthesis of the design on FPGA has been done by using the Xilinx synthesis technology of Xilinx ISE 9.2i tool. This paper described an implementation of the basic CDMA principle with user cost benefit tradeoff as the primary focal point.

4. Conclusion

This study examined the various types of CDMA transmitters and receivers used for ad-hoc networks and the pros and cons of using the techniques involved thereby. The present study focuses on the design of a transmitter and receiver with more efficient modulation techniques and increased capacity.

References

[1] Sreedevi, B., et al. "FPGA implementation of DSSS-CDMA transmitter and receiver for ADHOC networks." Computers & Informatics (ISCI), 2011 IEEE Symposium on. IEEE, 2011.
[2] Ullah, M. Habib, Akhmad Unggul Priantoro, and M. Jasim Uddin. "Design and construction of direct sequence spread spectrum CDMA transmitter and receiver." Computer and Information Technology, 2008. ICCIT 2008. 11th International Conference on. IEEE, 2008.
[3] Kakade, Vaibhav K. "Implementation of DS-CDMA Transmitter and Receiver in VHDL for

FPGA." International Journal of Latest Trends in Engineering and Technology (2013).
[4] Ahmad, Bilal, Malik Junaid Aziz, and Syed Asfandyar Gilani. "Design and Implementation of Frequency Hopping using Hardware Descriptive Language." International Journal of Advanced Research in Computer Science 5.7 (2014).
[5] Banerjee, Subhasish, et al. "ASIC Implementation of CDMA Transmitter using VHDL." International Journal of Advanced Engineering and Global Technology I Vol-04, Issue-01, January 2016.
[6] Gupta, Ashutosh, et al. "Performance analysis of different PN sequence and Orthogonal Spreading sequences in DS-SS." Confluence The Next Generation Information Technology Summit (Confluence), 2014 5th International Conference-. IEEE, 2014.
[7] Memon, Tayab D., Walliullah Ghangro, and B. S. Chowdhry. "Quadrature phase shift keying modulator & demodulator for wireless modem." Computer, Control and Communication, 2009. IC4 2009. 2nd International Conference on. IEEE, 2009.
[8] Popescu, S. O., A. S. Gontean, and D. Ianchis. "QPSK modulator on FPGA." Intelligent Systems and Informatics (SISY), 2011 IEEE 9th International Symposium on. IEEE, 2011.
[9] Andrews, Jeffrey G., Steven Weber, and Martin Haenggi. "Ad hoc networks: to spread or not to spread?[Ad hoc and sensor networks]." IEEE Communications Magazine 45.12 (2007): 84-91.
[10] Channe, Gaurav P., and C. N. Bhoyar. "VHDL Design of W-CDMA DS-SS System using Gold Code." Journal of Basic and Applied Engineering Research, Volume 1, Number 6; October, 2014.
[11] Qian, Xiaocong, Baoyu Zheng, and Jingwu Cui. "Application of multiuser detection on CDMA-based MANET." Signal Processing and Its Applications, 2005. Proceedings of the Eighth International Symposium on. Vol. 1. IEEE, 2005.
[12] Olšovský, Peter, and P. Podhoranský. "Design and simulation of frequency hopping technique in MATLAB." Institute of Electronics and Photonics, Faculty of Electrical Engineering and Information Technology, Slovak University of Technology.
[13] John G. Proakis and Masoud Salehi. "Communications Systems Engineering" Prentice Hall, Inc. Englewood Cliffs, New Jersey 1994.