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Analytical Analysis of Current Comparator Circuit Based on CMOS with 0.5µm & 0.35µm Technology

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Abstract: ***This paper presents current comparator designed by using CMOS having less power dissipation & less propagation delay. Power consumption and delay in propagation is a big problem can be reduced by the proper architecture. All designs have been implemented using two different technologies that is 0.35µm technologies with 3V supply voltage. There are many versions of comparator has come to improve the outcome. There is a comparison have been made with three earlier circuit comparing power dissipation and propagation delay and it has been found that the overall performance is better than the existing circuits. The proposed design of current comparator by using CMOS technology is having more speed with less power consumption.***

Keywords: Current Comparator, CMOS, Propagation, Delay, low power consumption, slew rate

1. Introduction

Over the past few decades CMOS based current comparator has been widely used in analogue, several electronics products & multiple-valued logic (MUL) circuits. This is mainly used in analog to digital conversion and any sensing detector & devices with the reduction in size and high speed having low power consumption. This circuit is based on current mode circuit technique. The main aim of modern VLSI technology is to design low power high speed circuits. Achieving for this goal, technology moved from voltage mode to current mode circuit technique. The first CMOS current comparator was designed by H. Traff [4] having four CMOS with high speed, low input impedance uses a simple inverter circuit. After that several proposal has come with several modifications by a number of designs, A. T. K. Tang [1], Lu Chen [2] and C. B. Kushwah [3], where speed increases but the power consumption also increased. It is desirable that comparators must have high speed with low power consumption. The input impedance must be high so that the comparator amplifies the small input differences to provide large variation in output.

2. Current Comparator

A current comparator determines if a current signal exceeds a given threshold and produces an output voltage. The current comparator device receives an input signal in form of current and compares it with given threshold current and the output would be inform of voltage. Current comparator circuit is a key element of analog and mixed signals processing. This circuit is not purely in current mode operation as the input signal is current and the output signal is digital logics in terms of voltage signal.

The earlier proposed CMOS current comparator having high output resistance reduced the frequency performance. The operating frequency was limited by high output resistance, caused a serious restriction on the available processing.

For getting the high dynamic range low power circuits latched feedback system from CMOS inverters is used, which increases the speed and reduces the power consumption and that was proposed by C. B. Kushwaha [3] which was more efficient than the existing circuits. Figure.[1] shows the block diagram of conventional current comparator circuit, where Iin represents the difference of the input currents and Vout shows the output voltage. In this circuit there are two inverters A1 and A2 and one buffer B1 implemented.

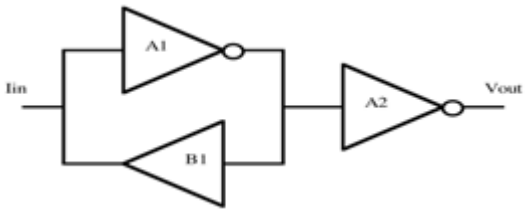

Figure 1: Block diagram of conventional current comparator circuit
Source: Google

When the value of current applied on the transimpedance stage of inverter A1 is lower than the particular value, then the V1 output voltage is that much small, so that inverter A2 will not operate in proper manner. To operate inverter A2 and providing higher and lower values of output voltages according to input current the applied input current must be that much high, so that the output voltage V1 is adequately high.

2.1 Circuit Description

A circuit with modified design is shown in figure. [2]

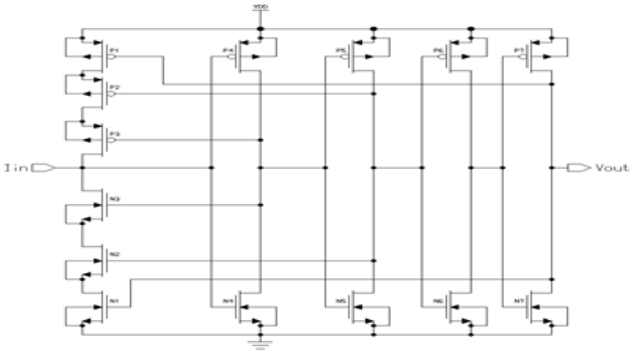

Figure 2: Schematic diagram of proposed current comparator using CMOS

In the implementation of this circuit there is the use of seven CMOS gates, redesigned feedback system which provides high speed operation at low current decision. Here there is an addition of two more inverters for providing positive feedback at P6/N6 and P7/N7 for improving the performance. At nodes P4/N4, P5/N5 and P7/N7 positive feedback operates respectively. In the predecision state transistors P3 & N3 are closed and transistors P1, P2 and N1, N2 are open. As the voltage on the comparator node is affected by input current, so the inverter P3/N3 begins to switch. As this slew rate to either rail the transistors P2 or N2 is switched closed. The output of P6/N6 affects the input of inverter P7/N7, therefore after few nano seconds the transistors P1 or N1 also closed. The redesigning of this latched feedback system dumps enough charge on the comparator node to significantly speed the decision process, especially at low input current. Without changing the chip area size of the comparator this circuit giving better performance by reducing propagation delay and power consumption.

3. Results and Discussion

The SPICE is used to show the simulation results of this proposed current comparator circuit shown in Figure 2. The proposed circuit using 0.35µm and 0.5µm CMOS with 3V supply voltage has less delay as compared to the existing. The simulation of this circuit in four different value of input current which followings 1ma, 100µA, 10µA & 1µA are. Figure 3 shows the simulation result of proposed circuit having applied input current is of 1ma with 0.5µm technology. In simulation result the propagation delay time, power dissipation and slew rate of proposed comparator circuit has observed. On increasing the current, delay time decreases. Table 1 & 2 shows the result of proposed current comparator circuit on different value of input currents with 0.5µm & 0.35µm technology. Figure [3], [5], [7] & [9] shows the delay with input current of 1000µA, 100µA, 10µA & 1µA with 0.5µm technology of proposed circuit respectively. Whereas Figure [4], [6], [8] & [10] shows the output voltage with applied input current of 1000µA, 100µA, 10µA & 1µA respectively with 0.5µm technology. Similarly Figure [11], [13], [15] & [17] shows the delay with input current of 1000µA, 100µA, 10µA & 1µA with 0.35µm technology of proposed circuit respectively. In Figure [12], [14], [16] & [18] shows the out voltage with applied input current of 1000µA, 100µA, 10µA & 1µA respectively with 0.35µm technology.

Table 1: Results of proposed current comparator circuit with 0.5µm CMOS technology

Input current (µA)	Propagation Delay (ns)	Power dissipation	Slew rate V/ns
1000	0.292	12.19 mW	30.849
100	0.513	248.38 µW	22.719
10	1.51	10.87 µW	6.99
1	10.10	854.69 nW	6.041

Table 2: Results of proposed current comparator circuit with 0.35µm technology

Input current (µA)	Propagation Delay (ns)	Power dissipation	Slew rate V/ns
1000	0.390	7.32 mW	24.779
100	0.729	156.32 µW	17.292
10	2.683	7.66 µW	12.168
1	20.223	572.88 nW	11.070

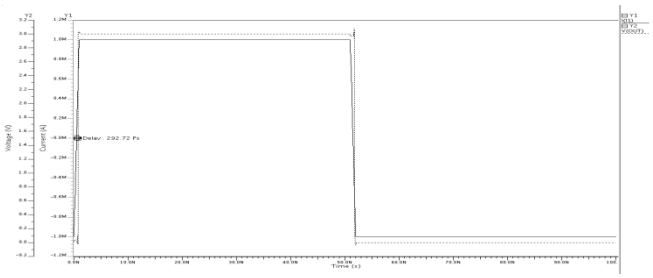

Figure 3: Delay with input current of 1mA with 0.5µm technology

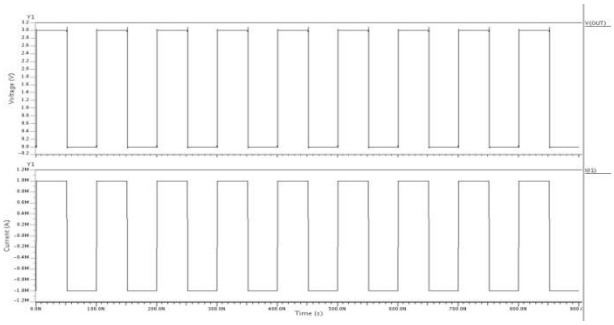

Figure 4: Voltage at output node with applied input current of 1mA with 0.5µm technology

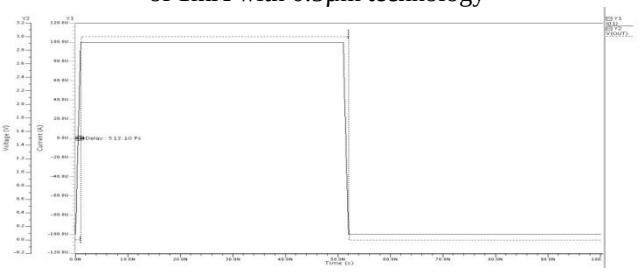

Figure 5: Delay with input current of 100µA with 0.5µm technology

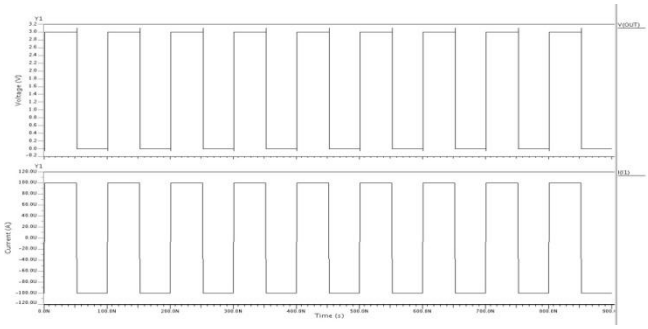

Figure 6: Voltage at output node with applied input current of 100µA with 0.5µm technology

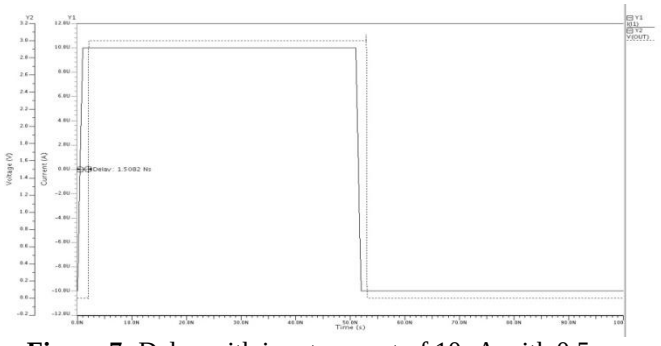

Figure 7: Delay with input current of 10µA with 0.5µm technology

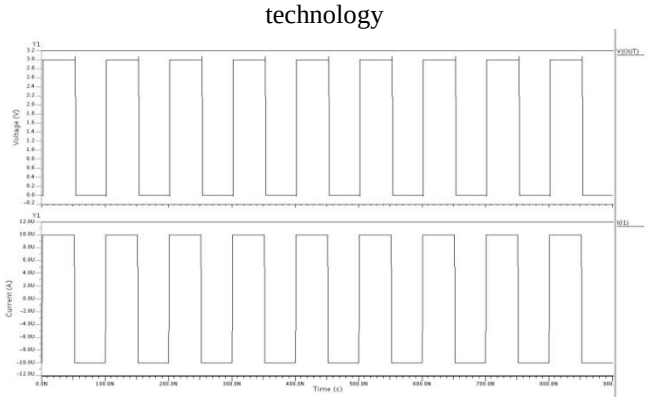

Figure 8: Voltage at output node with applied input current of 10µA with 0.5µm technology

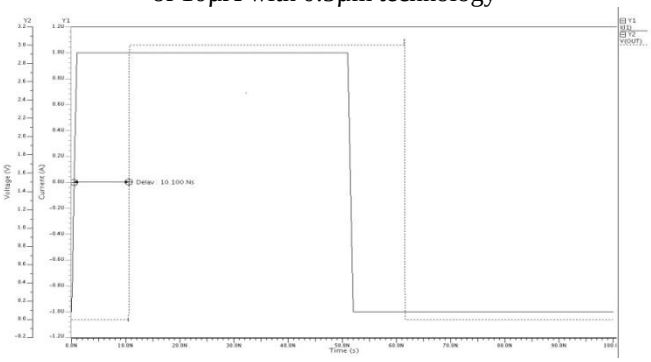

Figure 9: Delay with input current of 1µA with 0.5µm technology

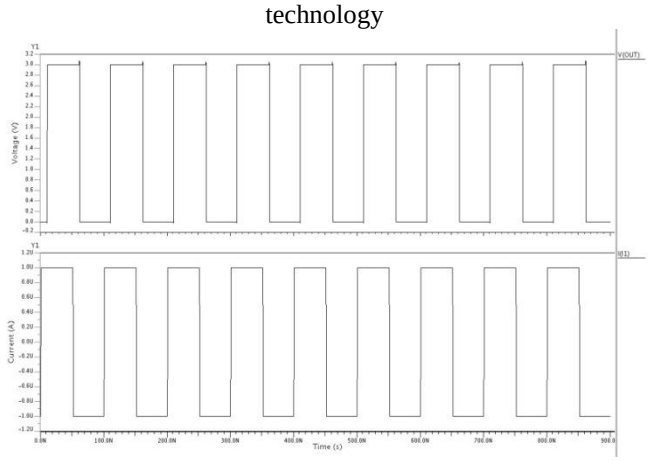

Figure 6: Voltage at output node with applied input current of 1µA with 0.5µm technology

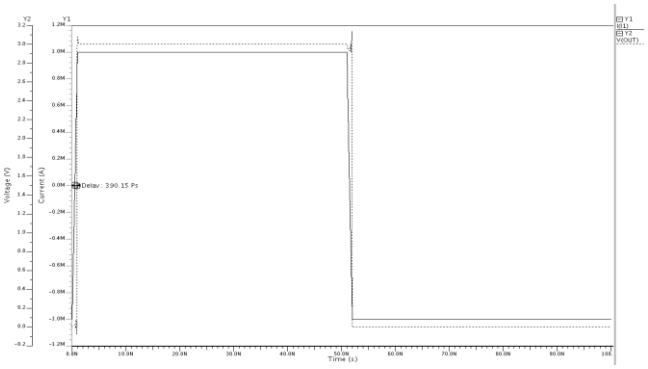

Figure 11: Delay with input current of 1mA with 0.35µm technology

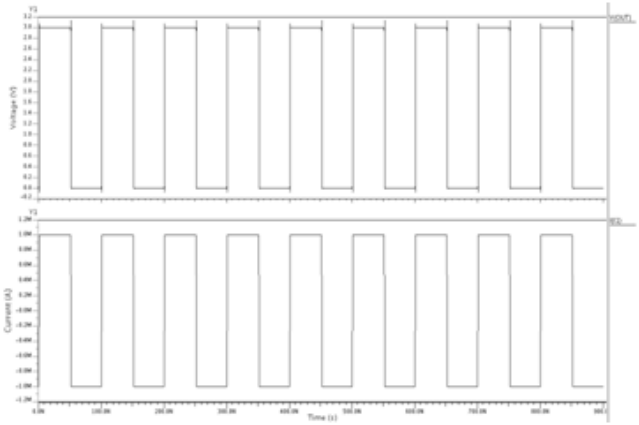

Figure 12: Voltage at output node with applied input current of 1mA with 0.35µm technology

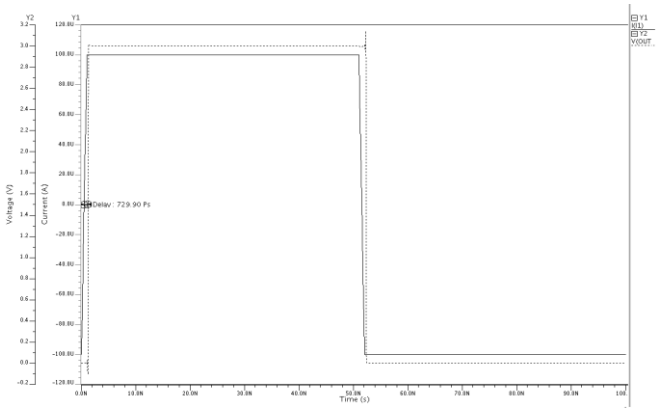

Figure 13: Delay with input current of 100µA with 0.35µm technology

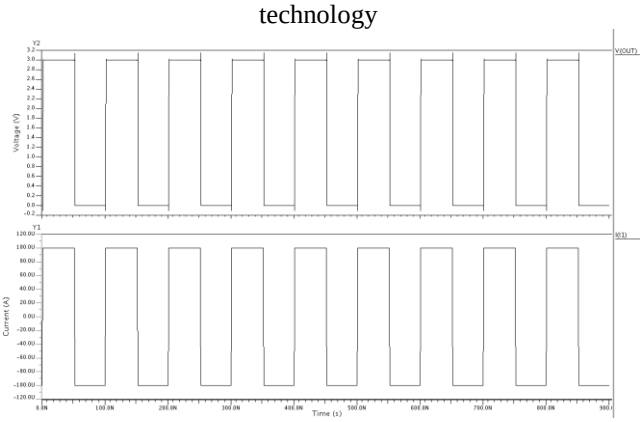

Figure 14: Voltage at output node with applied input current of 100µA with 0.35µm technology

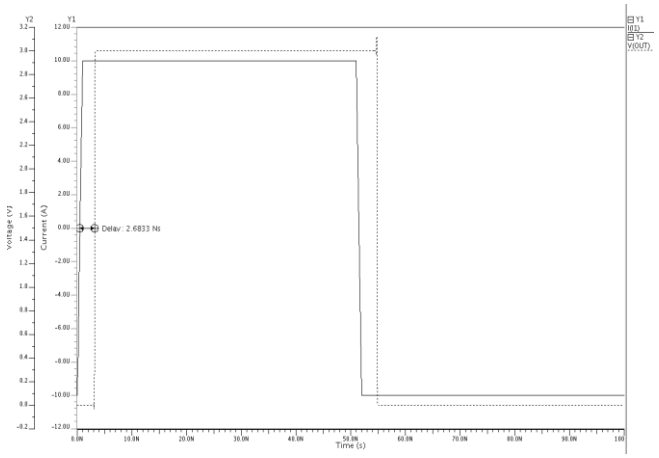

Figure 15: Delay with input current of 10µA with 0.35µm technology

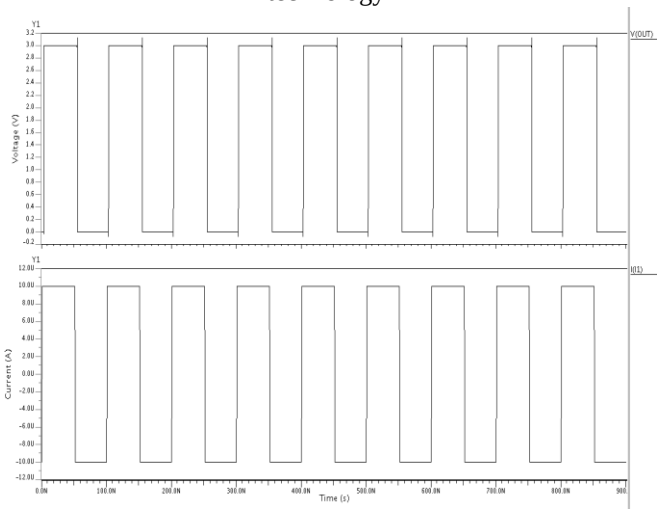

Figure 16: Voltage at output node with applied input current of 10µA with 0.35µm technology

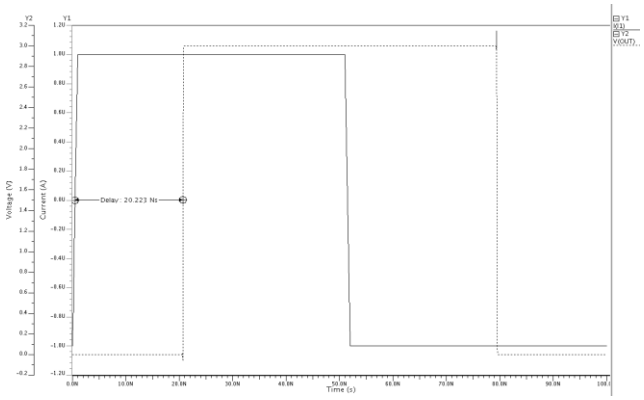

Figure 17: Delay with input current of 1µA with 0.35µm technology

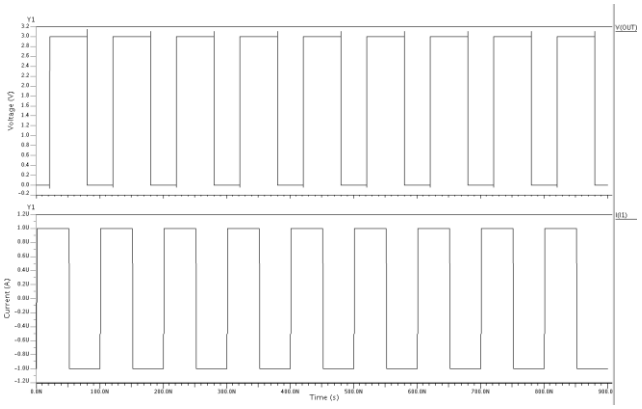

Figure 18: Voltage at output node with applied input current of 1µA with 0.35µm technology

4. Conclusion

In this we compare the different type of current comparator circuits on the basis of various parameters like current sensibility, power dissipation and delay time. All current comparator circuits are implemented and simulated in 0.35 µm CMOS technology using TSMC0.35 model file of simulation tool. In this work comparison of five existing, two modified and one proposed current comparator circuits is presented.

Analyzing the simulation results of different current comparator circuit we conclude some important points about the various

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