

Implementation of High Speed Flash ADC Using Multiplexer with Reduced Number of Preamplifier and Comparator Count

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Abstract: A high speed Flash analog-to-digital converter (ADC) using multiplexer with reduced number of preamplifiers and comparators is introduced. A conventional N-bit flash ADC requires 2^N-1 preamplifiers and comparators while The high speed flash ADC only needs $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators .For a 6-bit resolution, the high speed flash ADC requires a reduce number of preamplifiers and comparator, compare with those of the conventional flash ADC. The high speed flash 6-bit ADC consists of a reference ladder network, track and hold circuit, 10 preamplifiers, 17 comparators, a (2x1)-MUX, 8 (4x1)-MUXs and logic gates for encoder and registers. The high speed flash ADC is simulated with tanner suit 180nm CMOS process with 1-V supply voltage and consumes 0.378mW. At 50 MS/s, high speed flash ADC has the effective number of bits of 5.97-bit and the figure of merit of 0.12 pJ/conversion-step , signal to noise distortion ratio is 37.74 db and SFDR is 46.7 db.

Keywords: ADC, Multiplexers, comparator, Preamplifiers, Ladder Network and Buffer

1. Introduction

In many mobile applications, a low power and low resolution ADC is required to cover a wide range of sampling rates. A flash ADC is suitable for such applications because of its simplicity and fast operation. However, the large number of preamplifiers and comparators connected to input results in a voltage variable junction capacitance. This signal dependent capacitance results in flash ADCs having reduced effective number of bit (ENOB) and higher distortion at high input frequencies. Also, Flash ADCs have suffered from rather large input referred noise and comparator offsets. To overcome this problem, averaging techniques have been introduced. Interpolation techniques are also used to reduce the number of preamplifiers for low power operation. However, the number of comparators remains the same (2^N-1) for an N-bit converter. In this paper, a flash ADC architecture using multiplexers (MUXs) with a new comparator design is proposed. The MUXs are used to reduce the number of preamplifiers and comparators.

The applications of digital system can range from audio to communications applications to medical applications. These converters are implemented using a variety of architectures, sizes and speeds. The demand for the converter is oriented on area, speed, power of the converters. This has led to the investigation of alternative ADC design techniques. A conventional N-bit flash ADC requires 2^N-1 preamplifiers and comparators while The high speed flash ADC only needs $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators. As a result, the this flash ADC architecture has smaller size and lower power consumption. In addition, the operation speed is improved since the total input capacitance of the preamplifiers and comparators is decreased respectively.

2. Mux Based Flash ADC Architecture

Fig. 1 shows the architecture of the high speed 6-bit Flash ADC using multiplexers with track and hold circuit. This 6-bit high speed ADC consists of a reference ladder, preamplifiers, comparators, a (2x1)-MUX, and (4x1)-MUXs and logic gates for encoder and registers.

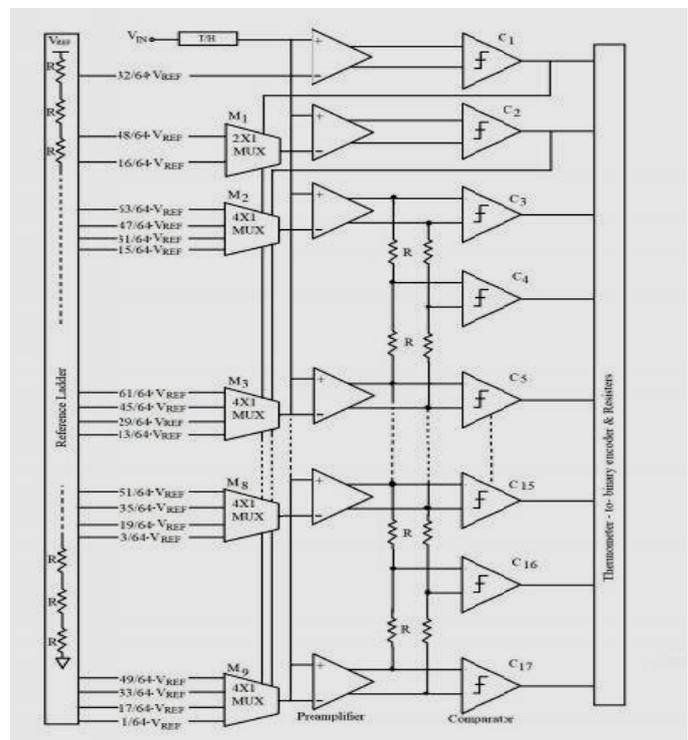


Figure 2.1: High Speed Flash ADC Architecture

The first comparator, C1, compares the sampled and amplified input signal with the middle reference level, $32/64 \cdot V_{ref}$. It decides the most significant bit (MSB) of the digital

output and the MSB becomes the control signal for the MUXs, M1 – M9. The second comparator, C2, does the same but its reference signal is either $16/64 \cdot V_{REF}$ or $48/64 \cdot V_{ref}$ through the (2x1)-MUX, which is determined by the control signal from the output of the first comparator. And then these two MSBs, the outputs of the first and second comparators, decide the reference voltages for the remaining comparators, C3 – C17 through (4x1)-MUXs. In order to reduce the number of preamplifiers and (4x1) MUXs, the interpolation technique using two resistors is applied. The outputs of the remaining comparators are encoded into appropriate values and then all digital bits are output at the same time. The main problem with the conventional flash architecture is that the number of comparators increases exponentially with the number of bits. For N bits, $2^N - 1$ comparators are needed. Due to the large number of comparators the number of bits is usually limited to 10, since the chip area and power consumption would be too large for higher resolutions. One more problem caused by the large number of comparators is the large input capacitance To drive such a large input capacitance, preamplifiers are needed. Since such preamplifiers consume extra power, it is therefore important to reduce the number of input preamplifier pairs. The interpolation techniques are used to reduce the number of preamplifiers, but the number of comparators still remains at $2^N - 1$ for an N-bit converter. On the other hand, the proposed ADC architecture using multiplexers needs only $2^{(N-3)} + 2$ preamplifiers and $2^{(N-2)} + 1$ comparators. The number of comparators needed for the proposed ADC can be calculated as below. Since the first comparator (C1) decides the MSB with the middle reference level, the number of comparators except for it can be reduced by half, compare to the traditional flash architecture.. The number of preamplifiers required is also reduced from $2^{(N-2)} + 1$ to $2^{(N-3)} + 2$ since the interpolation by two resistor technique was used.

Resolution (Bit)	Flash		Proposed	
	Preamp	Comparator	Preamp	Comparator
N	$2^N - 1$	$2^N - 1$	$2^{(N-3)} + 2$	$2^{(N-2)} + 1$
4	15	15	4	5
6	63	63	10	17
8	255	255	34	65
10	1023	1023	130	257

When the above circuit is simulated in S-edit for the given input and output we get the only 1 wrong levels in this ADC. Wrong levels are counted if voltage difference between and output signal is greater than quantization error. Therefore

number of correct levels will be 63 out of 64 .Hence the Effective Number of bit (ENOB) will be improve.

$$\text{No. of correct Levels} = 2^{\text{ENOB}}$$

When we simulate this circuit only for the input and output we get the corresponding waveform as shown in fig 2.2

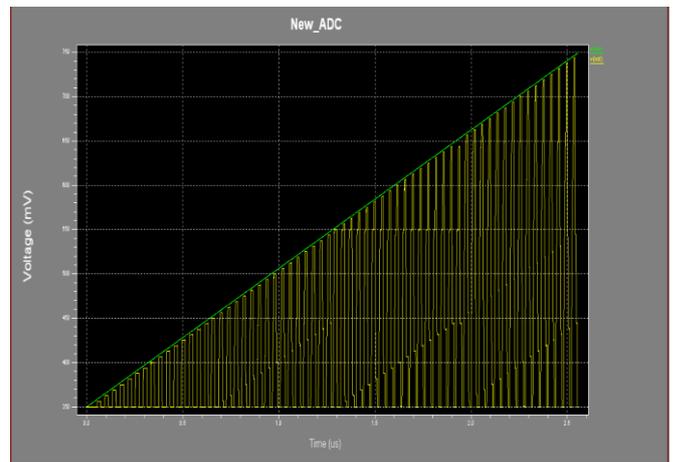


Figure 2.2: Waveform of input and output for 6-bit flash ADC in S-Edit

3. Used Preamplifier Based Comparator

Comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison and works on two phases reset and regeneration phase. It is a very crucial component of an analog to digital converter (ADC). the preamplifier based comparators are being used in today's A/D converters extensively because these comparators are high speed, lesser power consumption. It is used to compare the input signal with the reference voltage levels. The cross-coupled inverter placed above the input pair regenerates the input analog signal into a full-scale digital signal. This circuit is connected with SR latch to hold the output from the comparator. This gives the output at clock pulse when the input is greater than the reference voltage level. The fig shows the preamplifier based comparator simulation and performance.

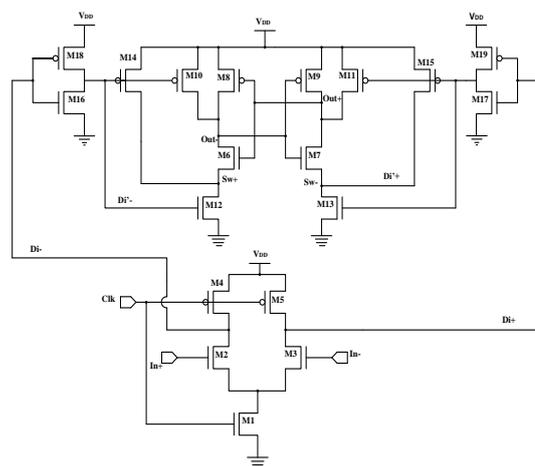


Figure 3.1: The Preamplifier based Comparator

When clock goes high the MOSFETS M1, M2, M5, M6 turn off and M11 turn on. This provides a discharge path to ground for nodes N1 and N2 and these nodes start discharging at different rates depending on the input voltages V_{tp} and V_{tn} at M9 and M10.

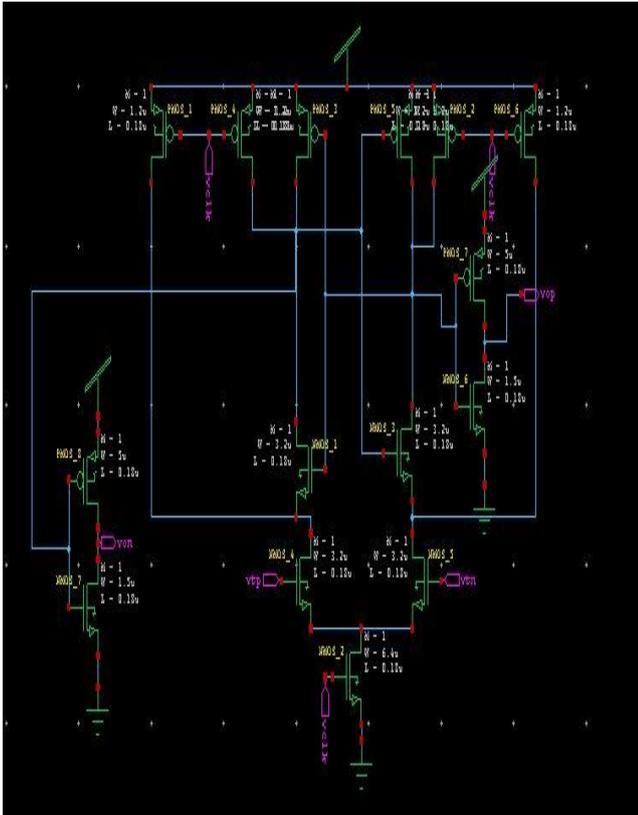


Figure 3.2: Simulation of Comparator design

The main problem with this comparator is that the output signal of the latch stage is fluctuating during clock transition. This is happening due to the presence of noise in input terminals

4. Proposed Comparator Design

Circuit Diagram of Proposed Comparator is shown in Figure 4.1. This circuit mainly is a derived version of the [5]. The back-to-back latch stage is replaced with back-to-back dual-input single output differential amplifier. Differential amplifier has so many advantages over the conventional latch which nothing but an inverter. It has higher immunity to environmental noise and it rejects common mode noise or in other words it has better CMRR. Another property of differential signaling is the increase in maximum achievable voltage swings. It also provides simpler biasing and higher linearity. Here our main purpose is to eliminating the noise that is present in the latch stage and for which output is getting fluctuated with clock transition.

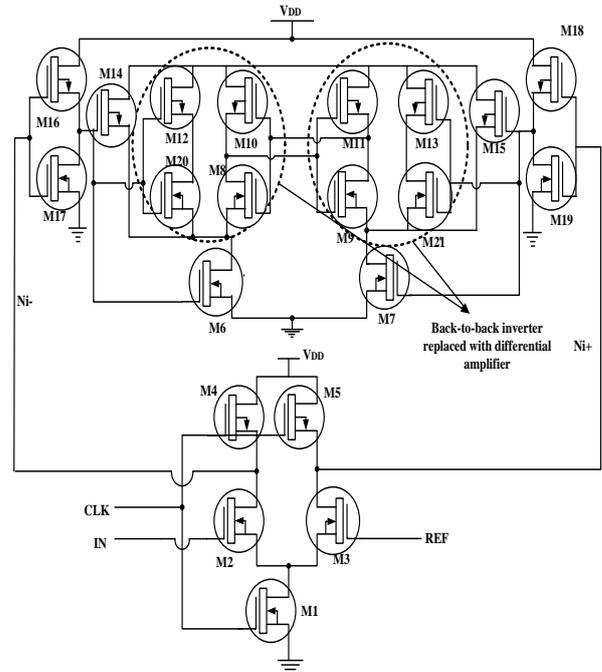


Figure 4.1: Proposed Comparator Circuit

During reset phase (clk= 0V), PMOS transistor M4 and M5 turn on and they charge Ni node voltages to V DD and Hence NMOS transistors M17 and M19 turns on and discharges Ni' nodes voltages to GND. Then M14, M15 and PMOS transistors of differential amplifier blocks M12 and M13 turns on, NMOS transistors of differential amplifier block M8, M9 and M6, M7 turns off. The out nodes are charges to VDD. Hence the back-to-back differential pair again regenerates the Ni' node signals and because of M6 and M7 being on, the output latch stage converts the small voltage difference transmitted from Ni' node into a full scale digital level output.

After discussing the circuit of proposed comparator our next aim is to simulate the circuit using TANNER tool .The simulation of this circuit is shown below. The simulated waveform of high speed proposed comparator for flash ADC circuit is shown below in fig. 4.2

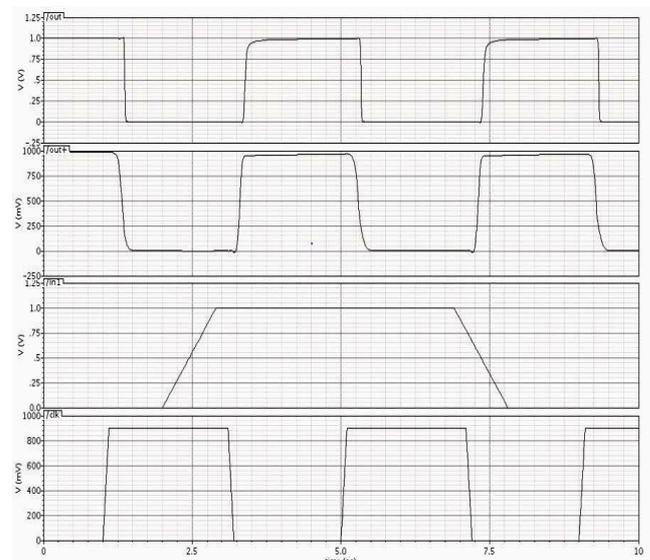


Figure 4.2: Proposed Comparator Waveform

5. Simulation Results

This high speed flash 6-bit ADC is designed with an HSPICE using 1P6M 180nm CMOS process with 1-V supply voltage and consumes 0.378-mW. At 50 MS/s, high speed flash ADC has the effective number of bits of 5.97-bit and the figure of merit of 0.12 pJ/conversion-step effective no of bit is 5.97, signal to noise distortion ratio is 37.74 db and SFDR is 46.7 db.

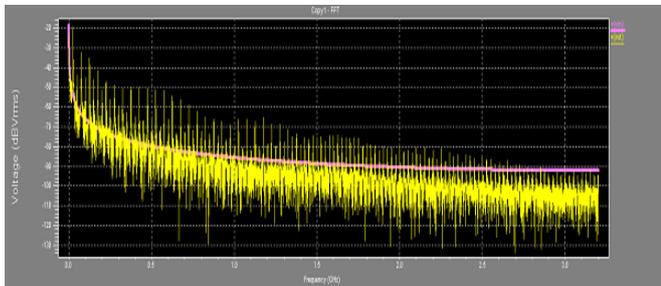


Figure 5.1: FFT spectrum at 24-MHz input and 50-MHz sampling

Fig .5.1 shows the simulated FFT spectrum for a full-scale 24-MHz input signal while sampling at 50-MS/s. This spectrum helps us to get the value of Spur Free Dynamic Range (SFDR).

The table 1 shows the summary of the high speed flash ADC performance at 50-Ms/s. Table 2 lists the comparison of this work with other 6-bit flash ADCs.

Table 1: Specification Summary

Specification	Simulation Result
Technology	0.18 um CMOS
Supply Voltage	1V
Sampling Rate	50 MS/s
Power	0.378mw
ENOB (@fin=Nyquist)	5.97 bit
SNDR (@fin=Nyquist)	37.74 db
SFDR (@fin=Nyquist)	46.7 db
FOM	0.12 pJ//conv-steps

Table 2: Comparisons to Flash ADCs

Publication Title	MWSCAS '2009	CICC '2011	TENCON 2013	TENC on 2016	This Work 2018
Technology	90 nm	90nm	0.18 um	0.18um	0.18um
Supply Voltage(V)	1	1.2	1	1	1
Power(mw)	72	12	0.539	0.432	0.378
ENOB (bit)	-	4.94	5.46	5.95	5.97
Resolution (bit)	6	6	6	6	6
Sampling Rate (MS/s)	1000	400	50	50	50
FOM (pJ/conv.-step)	1.13	0.97	0.18	0.15	0.12

6. Conclusion

A conventional N-bit flash ADC requires 2^N-1 preamplifiers and comparators while The high speed flash ADC only needs $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators .For a 6-bit resolution, the high speed flash ADC requires a reduce number of preamplifiers and comparator, compare with those of the conventional flash ADC. As a result, the High speed flash ADC architecture has smaller size and lower power Consumption having better FOM and SNDR.

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Author Profile

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