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Electrical Properties of SiO2/PSi Hetero Junction Prepared by Electrochemical Etching Process

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Abstract: ***In this paper, the electrical properties of porous silicon (PSi) structure fabricated by using the electrochemical etching process in HF acid, SiO2/PSi hetero junction made by deposition of SiO_2 layer on porous silicon.The dark I-V characteristics synthesized by electrochemical etching are presented of hetero junction showed are strong depended on etching time. The ideality factor and saturation current of hetero junction are calculated from I-V under forward bias. C-V measurements confirmed that the prepared hetero junctions are abrupt type.***

1. Introduction

Porous silicon (PS) is a new face of silicon consist of a complex structure of pore and Si [1]. PS has attracted a great deal of interest since Canham in (1990) who reported the production of photo luminescence properties PL from PS [2].the PS divided to groups based on the pore width , into three types. The nano, meso and macro [3].In order to understand the PSi layer formation it is necessary to deal with the dissolution chemistry of silicon anodically biased in HF acid. A silicon (Si) surface is known to be virtually inert against attack of HF acid [4]. If the silicon is under anodic bias, the reaction begins with the generation of holes, either thermally generated or photogenerated. The holes drift under the applied bias to the interface between silicon and solution, where they can react, and then formation PSi layer is observed as long as the reaction is limited by the charge supply of the electrode. This condition is fulfilled for current density (J) below the critical current density (J_{PSi}) [5]. Porous silicon (PS) consists of a network of nanoscale sized silicon wires and voids which formed when crystalline silicon wafers are etched electrochemically in hydrofluoric acid based electrolyte solution under constant anodization conditions like etching time , current density , HF concentration and Si orientation [6]. The surface chemistry of porous silicon is of interest in both fundamental studies and for applications arising from the technological importance of silicon in microelectronics, sensors and photovoltaics. Chemical modification of porous silicon surfaces can also be used to manipulate the photoluminescence, spectroscopic and electroluminescence behavior [7], Introduce nano porous holes in its micro-structure, providing a large surface to volume ratio [8].

Porous silicon structures has good mechanical robustness, chemical stability and compatibility with existing silicon technology therefore has a wide area of potential applications such as waveguides, 1D photonic crystals, chemical sensors, biological sensors, photovoltaic devices…etc [9]. We can say that the main requirements for porous silicon formations are [10-11]:

1) The silicon substrate must be anodically electrode. This means a forward bias of p-type silicon, and reverse bias for n-type silicon.
2) The value of etching current density must be below the critical value of Electro polishing Current density (J_{PSi}).

For n-type doped and semi-insulating p-type doped silicon, light must be supplied

2. Experiment

A porous silicon structure was prepared by electrochemical etching of silicon substrate of (111) orientation with a resistivity (4 -10) Ω cm and the etching cell made from Teflon because the Teflon not interaction with HF acid, rubber O-ring is used before the upper part of cell shown in Figure (1).The electrochemical cell used has two electrode configurations with a platinum(stainless still) or gold mesh electrode as cathode and silicon wafer as anode and a digital Multimeter was connected with silicon and the other side with power supply. after cutting the silicon samples into (2.25×2.25) cm^2 pieces.the wafer and rinsed with acetone and methanol to remove dirt. In order to remove the native oxide layer on the samples, The etching times was chosen to be 10 min, different current (20) mA.the samples were dipped in (48%) concentration of (HF)acid in mixing ratio (1:1) HF: ethanol with the aid of diode laser source as an illumination sources. A diode laser with wavelength (405 nm)for n-type silicon shown in Figure (2). However, the addition of ethanol to HF eliminates hydrogen and ensures complete infiltration of HF solution within the pores which further improves the uniform distribution of porosity and thickness.

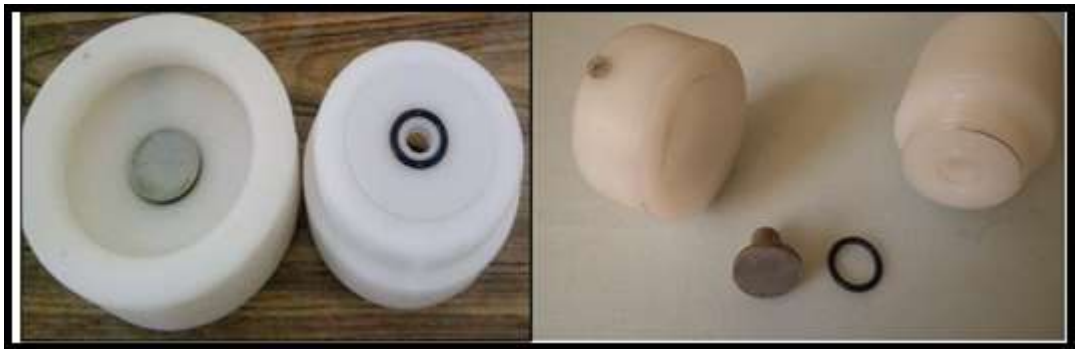


Figure 1: Show the parts of Teflon cell used in work

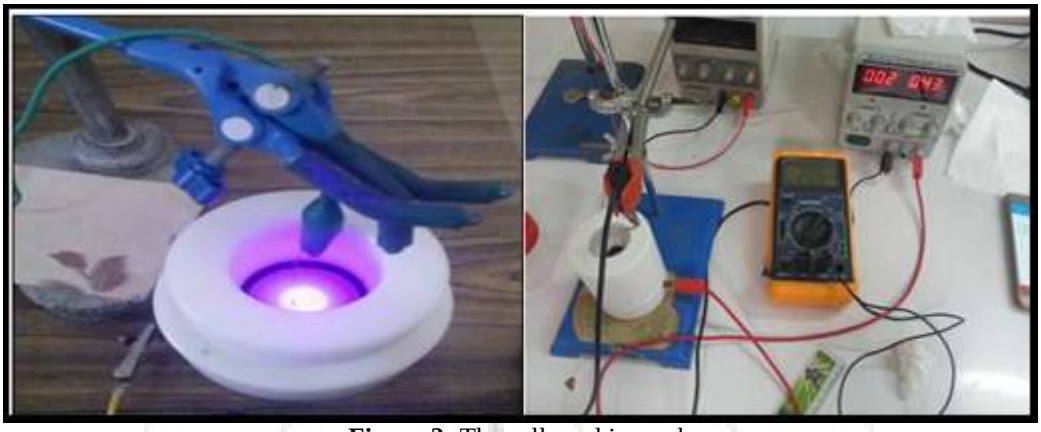


Figure 2: The cell used in work

The porous silicon samples were rinsed in ethanol after removal from the solution. The samples was left in ambient air for a few minutes to dry and after that stored in container with methanol to prevent the formation of oxide layer on the prepared samples. Figure (2) shows that the porous silicon samples after etching process has uniform circle.

3. Result

Figure (3) show current – voltage characteristics of SiO_2/Porous-Si under forward and reverse bias. The samples prepared with various etching time (900s and 1200s). from J-V characteristics, show a clear rectification and indicate that the junction was anisotype junction. The current density voltage (J-V) characteristics for the forward bias are presented also on a semi-log plot. All the figures reveal two distinct regions which belong to two different mechanisms of current transfer through the hetero junction with operational voltage ($V_T \approx 0.6\ V$) . The first mechanism is localized at ($V_F < V_T$) where the recombination current is the dominant one. In this case, recombination process will taken place, that mean each excited electron from valance band to conduction band will recombine with a hole in valance band. For higher voltage $V_F > V_T$ there is another region where the tunneling current is predominant. In this region the bias voltage can deliver the electrons with enough energy to penetrate the barrier between the two sides of the junction. These results agree with other workers for SiO_2/Porous- Si prepared by electrochemical etching technique.

In reverse bias also there are two regions; first at low voltage, where the current increases with the applied voltage and the generation current is dominant. In second region the current independent from the voltage. One can also notice that the forward current decreases with increasing etching time, when etching time increases the porous layer increases and the porosity increases so the pore walls act as carrier trapped and cause high resistivity and the current will decrease[14] .

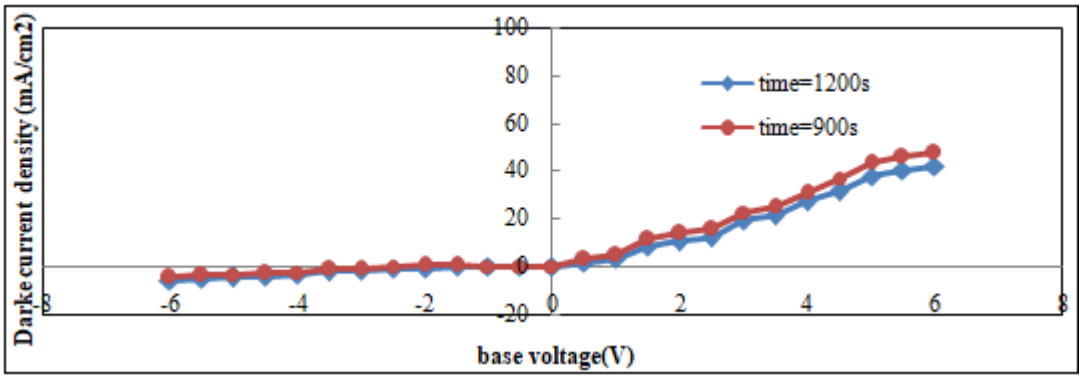
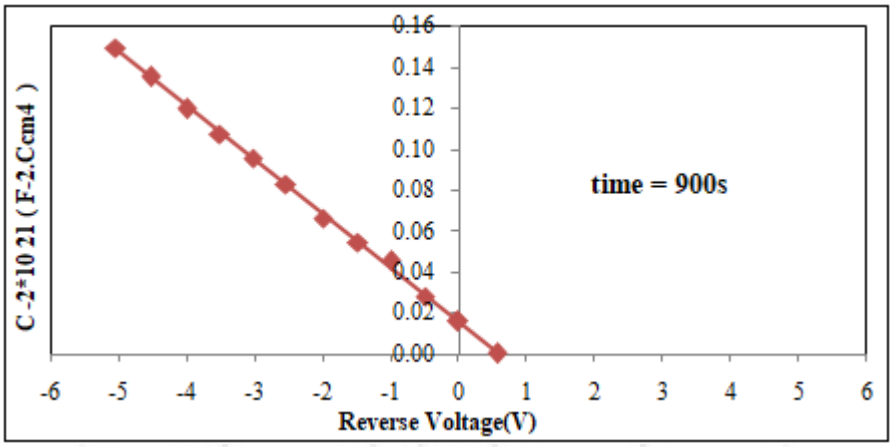


Figure 3: Characteristics for P Si /SiO2 anisotype Hetero junctions at different etching time

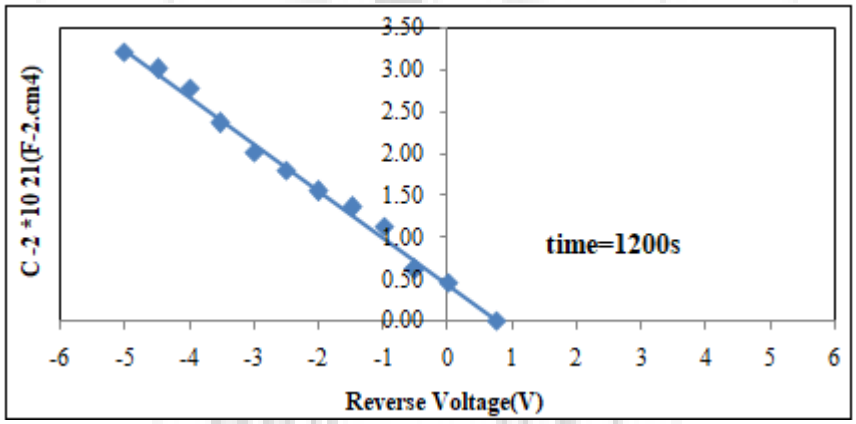
The figure of current-voltage characteristics shows the (J-V) characteristics of (SiO_2/PSi) hetreo detector at dark room temperature and under day light illumination of structure of Al thin layer deposited on to the mirror-like surface of the silicon substrate, the rectification properties of the structure is due to the formation of Shottky barrier between the Al thin film and the silicon substrate [15]. Several important parameters such as built in potential, junction capacitance, and doping concentration can be inferred from C-V measurements. Fig.(4) demonstrates the variation of the junction capacitance versus reverse bias voltage. The Figure shows that junction capacitance varies inversely with reverse bias voltage. The distribution of (C-V) suggests that the junction of SiO_2/PSi is anisotype and analogous to the behavior predicted by the equation [16]:

$$\frac{C}{A} = \left[\frac{qN_nN_p\varepsilon_n\varepsilon_p}{2(\varepsilon_nN_n + \varepsilon_pN_p)(V_D - V_a)}\right]$$

Reduction of junction capacitance with increasing bias voltage is as a result of increasing built-in potential[17-18].



(a)



(b)

Figure 4(a and b): (1/C2-V) Characteristics for (PSi/SiO2) HJ detector

From Fig.(4). This kind of behavior is agreement with that obtained by Zimin and Komarov [19] for thick layers and high porosity of the porous silicon prepared by electrochemical etching process. Fig.4 shows reciprocal of square_capacitance versus bias voltage ($1/C^2$-V). This plot shows a linear relationship C^{-2} with bias voltage indicates that the junction is an abrupt type; this means that the depletion layer is not constant and so the carrier concentration will be not constant at the depletion layer.

4. Conclusions

The Al/PS/n-SiO2/Al structure in this work is a Schottky-like junction with high ideality factor due to the formation of high density of interface states at PS boundaries. The junction is an abrupt type.

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