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Cascaded Multilevel Inverter Topology with Reduced Number of Switches

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Abstract: ***Consider the possibility that we can't utilize the stored power in a battery when we don't have power supply. Since the availability of power in a battery is in DC, so to utilize this power in battery we have to change this DC type of power to AC type. So here comes the idea of inverters. The device which can convert availability of DC form of power into AC is known as inverters. They come in all sizes and shapes, from a large power rating to a low power rating. Inverters can come in a wide range of assortments, contrasting in power, efficiency, cost and purpose. The motivation behind a DC-AC power inverter is regularly to take DC power supplied by a battery, for example, a 12kvolt auto battery, and change it into a 220 volt AC power source working at 50 Hz, imitating the power accessible at an ordinary household electrical outlet. Various industrial applications have been started to require higher power device lately. Some medium voltage motor drives and utility applications require megawatt power level and medium voltage. For a medium voltage power grid, it is difficult to use one and only one power semiconductor switch specifically. Subsequently, multilevel power converter structures have been developed as an option in high power and medium voltage circumstances. A multilevel converter accomplishes high power evaluations, as wellkas empowerskthe utilizationkof renewablekenergy sources like photovoltaic, wind, fuelkcells, which cankbe effectively interfacedkto a multilevel converter framework for a powerful application.Various multilevel inverter structures involve the use of large number of semiconductor devices to obtain higher levels of output AC voltages from several DC voltage sources. So as to minimize the number of semiconductor devices for the same higher voltage levels at the output of a multilevel inverter, modified multilevel inverter topology is presented. This helps in reducing the number of switches used and thus complexity of using more number of triggering units is also reduced.***

Keywords: Multilevel inverter, cascaded multilevel inverter, basic unit multilevel inverter, H-bridge inverter, gate drive circuit

1. Introduction

For medium voltage grid, it is troublesome to associate single power semiconductor switch directly. Subsequently, a multilevel power converter structure has been presented as an option in high power and medium voltage circumstances, for example laminators, factories, transport pumps, compressors etc. As a cost reduced arrangement, multilevel converter accomplishes high power evaluations, as well as empowers the utilization of low power application in renewable energy sources, for example photovoltaic, wind and other energy components which can be effectively interfaced to a multilevel converter system for a high power uses.

The most widely recognized introductory utilization of multilevel converters has been in traction, both in trains and track-side static converters. Numerous multilevel converter applications concentrate on utility interface for renewable energy system, modern medium-voltage motor drives, Flexible AC transmission system (FACTS), and traction drives. Later applications have been for system converters for VAR and stability enhancing, high voltage motor drive, active filtering, high voltage direct current (HVDC) transmission, and in recent days it is used for variable speed drives in medium voltage motors.

The inverters in such application ranges as expressed above must have the capacity to handle high voltage and extensive power. Therefore, two level high-voltage and large power inverters have been composed with series association of switching power devices for example integrated gate bipolar transistors (IGBTs), integrated gate commutated transistors (IGCTs) and gate turn off thyristors (GTOs) on the grounds that the series arrangement association permits achieving much higher voltages. However, the series arrangement association has enormous issues in particular like unequal distribution of voltage across series arrangement that may make the connected voltage of individual device much higher than blocking voltage of the device amid transient and steady state switching operation of device.

Ask other options to successfully tackle the above stated issues, a few circuit topologies of multilevel inverter have been explored and used. The output voltage of the multilevel inverter has numerous levels incorporated from a few separate DC voltage sources. The nature of the output voltage is enhanced as the quantity of voltage levels builds, so the amount of output filters can be decreased.

The idea of multilevel inverters has been presented subsequent to 1975. Separate DC sourced full-bridged cells are put in an arrangement to integrate a staircase AC output voltage. The term multilevel started with the three-level converter. In this way, a few multilevel converter topologies have been produced. In 1981 diode clamped multilevel inverter additionally called the Neutral Point Clamped (NPC) inverter plans were proposed. In 1992 capacitor clamped (or flying capacitor) multilevel inverters, and in 1996 cascaded multilevel inverters were proposed. Despite the fact that the course multilevel inverter was developed before, its application did not win until the mid 1990s. The upsides of multilevel inverters were obvious for utility applications and motor drives. The course inverter has attracted awesome enthusiasm because of the considerable interest of high power medium voltage inverters. As of late, some new topologies of multilevel inverters have developed. This incorporates hybrid multilevel inverters and soft switched multilevel inverters, generalized multilevel inverters, and mixed multilevel inverters. These multilevel inverters can amplify evaluated inverter voltage by expanding the quantity of voltage levels. They can likewise expand equivalent switching frequency without the expansion of actual switching frequency, in this way

decreasing electromagnetic interference effects and ripple content of inverter output voltage.

A multilevel converter can be actualized in a wide range of ways. The least difficult procedures include the series association of conventional converters or parallel to frame the multilevel waveforms. More intricate structures adequately embed converters inside converters. The voltage or current rating of the multilevel converter turns into a multiple of the individual switches, therefore the power rating of the converter can exceed the cut off forced by the individual switching device.

The basic idea of a multilevel converter to accomplish higher power is to utilize a sequence of power semiconductor switches with a few lower voltage dc sources to develop the AC voltage by synthesizing a staircase voltage waveform. Batteries, Capacitors and renewable energy voltage sources can be utilized as the various dc voltage sources. The appraised voltage of the power semiconductor switches depends just upon the rating of the DC voltage sources to which they are associated.

A multilevel converter has a few preferences over a routine two-level converter. The appealing elements of a multilevel converter can be quickly considered for the below mentioned reasons

1) Staircase waveform quality: Multilevel converters generate the output voltages with low distortion, decreased electromagnetic compatibility (EMC) issues, and subsequently the dv/dt stresses can be reduced.
2) Common mode (CM) voltage: Common mode voltage is the potential difference between neutral point of the load and system ground. Multilevel inverters generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings.
3) Input current: Multilevel converters can draw input current with low order distortion.
4) Switching Frequency: Multilevel converters can work at both high switching frequency PWM and fundamental switching frequency. It is to be noticed that lower switching frequency for the most part means lower switching losses and higher efficiency.

Multilevel converters do have some hindrances. One specific weakness is the more noteworthy number of power semiconductor switches required. Despite the fact that lower voltage rated switches can be used in a multilevel converter, every switch requires a related gate drive circuit. This makes the general system to be more costly and complex.

Several adjustment systems and control ideal models have been created for multilevel converters, for example, sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others so as to further increase the efficiency of the multilevel inverters.

Why Cascaded H-Bridge MLI

Cascaded H-Bridge (CHB) design has as of late turned out to be in demand in adjustable speed drives (ASD) and high-power AC supplies. A cascaded multilevel inverter comprises of a series combination of H-bridge (single phase full bridge) inverter sets in each of its three phases. Every H bridge unit has its own particular DC source, which for an induction motor would be a battery set, fuel cell or solar cell. Each SDC (separate DC source) is connected with a single phase full-bridge inverter. The AC terminal 0 voltages of various level inverters are joined in series arrangement. Through various blends of the 4 switches, every converter level can produce three distinctive voltages, zero, $+V_{dc}$ and $-V_{dc}$. The synthesized voltage waveform is the sum of the individual inverter output which is obtained by connecting AC output of various full bridge inverters in the same phase in series arrangement. Note that the number of output phase voltage levels is characterized uniquely in contrast to those of the other two converters i.e. diode clamped and flying capacitor.

In this arrangement, the quantity of output stage voltage levels is characterized by the equation m=k2N+1, where N is the quantity of DC sources. For instance, a seven level cascaded converter comprises of three full bridge inverters and three DC sources. Least harmonic distortion can be obtained by controlling the conducting angles at various inverter levels. Every H-bridge unit creates a quasi-square waveform by moving its positive and negative stage legs switching timings. Neglecting the pulse width of the quasi-square wave every switching device dependably conducts for 180° (or half cycle). This switching strategy makes the greater part of the switching devices to share current stress equally. In the charging mode, the cascaded inverters go about as rectifiers, and power streams from the charger (alternating current source) to the batteries. In the motoring mode, power streams from the batteries through the cascaded inverters to the motor. The cascaded converters can like wise go about as rectifiers to recapture the kinetic energy of the vehicle if regenerative braking is utilized. This type of converter can stay away from voltage balancing capacitors or clamping diodes.

Identical H-bridge inverter units can be used, accordingly enhancing the modularity and significantly decreasing generation costs. Battery fed cascaded inverter model driving an induction motor at 50% and 80% of the rated speed both the voltage and current are tending to be sinusoidal.

The fundamental main points of utilizing the cascaded inverter as a part of an induction motor include:

1) It makes induction motor more secure and open wiring feasible for the greater part of an induction motor power system.
2) Traditionalk230 V ork460 V motor can be utilized, consequently higher output is relied upon as compared with low voltage motor.
3) No EMI issue or common mode voltage/current issue exists.
4) Low voltage switching devices can be utilized.
5) No charge unbalance issue exists in both drive mode and charge mode.

2. Literature Survey

2.1 Review of literature survey

I have done a vast literature survey and I have referred many international journals and conference papers, out of which I have given the details of seven papers in the literature survey.

Byeong-Mun Song, Member, IEEE, Junhyung Kim, Jih-Sheng Lai, Senior Member, IEEE, Ki-Chul Seong, Hae-Jong Kim, and Sun-Soon Park "**A Multilevel Soft-Switching Inverter with Inductor Coupling**" IEEE Vol. 37, No. 2, March/April 2001:

This paper proposes a new soft-switching flying capacitor multilevel inverter that can be generalized and be extended from three levels to any number of levels. A zero-voltage-transition (ZVT) soft-switching FCMI with inductor coupling, in which the auxiliary devices have less voltage and current ratings is proposed.

The soft switching technique proposed in this topology includes two pairs of auxiliary switches, two pairs of blocking diodes and two coupled inductors per phase leg. The coupled inductor used here helps in reducing the peak current rating of the auxiliary switch to a little over half of the resonant inductor current and discharging the resonant tank components thus, resulting in the reduction of magnetic size and weight of the inverter. Along with the coupled inductor, saturable inductor is also used to block the circulating current during steady state and reset the magnetizing current flowing through the coupled inductor. Further voltage stabilization of the flying capacitors as well as the DC-link capacitors under soft-switching operations is briefly explained and implemented through both simulation and experiment.

The basic operating principle is verified through computer simulation in the Pspice software and experiment with a prototype inverter. Advantages of this proposed concept include lower voltage and current ratings for auxiliary switches and diodes which is achieved by using a coupled inductor and midpoint rail between the dc capacitors. This paper explains the operation, design, control, and switching patterns along with voltage balancing for stability along with safer operation through simulation and experiment. Results indicate that the proposed inverter achieves a zero-voltage condition in all of the main switches and a zero-current turn-off to the auxiliary switches during commutation processes.

José rodríguez, senior member, IEEE, jih-sheng lai, senior member, IEEE, and Fang zheng peng, senior member, IEEE "**Multilevel inverters: a survey of topologies, Controls, and applications**" IEEE transactions on industrial electronics, vol. 49, no. 4, august 2002:

The most important topologies of the multilevel inverter like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel inverter with separate DC sources is presented in this paper. Emerging topologies like asymmetric hybrid cells and soft switched multilevel inverters are also discussed. A generalized model for multilevel inverter is also discussed through which any of the multilevel inverter topology can be derived. The authors have discussed the advantages of the generalized model of balancing each DC voltage level automatically at any number of levels, regardless of active or reactive power conversion.

This paper discusses the most relevant control and modulation methods like multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. Few important applications of the converters such as laminators, conveyor belts, and unified power-flow controllers are also presented. The need of an active front end at the input side for those inverters supplying regenerative loads is also discussed, and the circuit topology options are also presented. Finally, the peripherally developing areas such as high-voltage high-power devices and optical sensors and other opportunities for future developments are discussed.

Ebrahim Babaei, Mahrdad Tarafdar Haque and Seyed Hossein Hosseini "**A Novel Structure for Multilevel Converters**" in proceeding of eighth international conference on electrical machines and systems China, vol 2 2005, pg:12778-83

Multilevel converter is a power electronics system that synthesizes a desired voltage output from several levels of DC voltages as inputs. In a distributed energy system consisting of fuel cells, wind turbines, solar cells, etc., the multilevel converter can provide a mechanism to feed these sources into an existing three-phase power grid. This paper presents a new structure for asymmetric multilevel converters. The new topology consists of N series-connected inverters per phase. This paper presents optimized multilevel inverter with minimum DC voltage sources and switches. This topology can generate a large number of levels with asymmetric DC voltage sources.

In the proposed topology of multilevel inverter, each stage consists of two DC voltage sources and six bi-directional switches. DC voltage sources used here are of different values so as to generate higher output voltage magnitude of seven levels with same number of DC sources and switches.

A new algorithm for calculating the levels of DC voltage sources is presented. A complete analysis for calculating the harmonic distortion is given. This converter has higher efficiency because the number of switches is reduced and the devices can be switched at low frequency. The paper also presents an application in which the converter has been applied as the core of a digital video recorder (DVR), which is based on this converter and simulation results show that the DVR solves the power quality problems such as voltage sag, voltage swell, unbalanced and distorted voltages.

Ebrahim Babaei "**A Cascade Multilevel Converter Topology With Reduced Number of Switches**" IEEE transactions on power electronics, vol. 23, no. 6, november 2008:

A new basic unit for a multilevel converter has been presented in this paper. The possibility of extension or series

connection of this basic unit is studied in this paper. A new multilevel converter topology having many steps with fewer power electronics switches is discussed in this paper. This circuit consists of series-connected sub-multilevel converter blocks in which a capacitor and four bi-directional switches are used in each basic unit. Optimal structures for four different conditions namely; optimal structure for maximum number of voltage steps with constant number of switches, optimal structure for maximum number of voltage steps with constant number of capacitors, optimal structure for minimum number of switches with constant number of voltage steps, and optimal structure for minimum standing voltage of switches with constant number of voltage steps minimum number of switches and capacitors, minimum standing voltage on switches for producing maximum output voltage steps are discussed. A new algorithm for determination of DC voltage source magnitudes has also been presented. Further an extended topology for producing both positive and negative voltage levels from the cascaded basic units is presented.

The proposed structure is simulated in PSCAD simulation software with 22 IGBT switches along with anti-parallel diode to provide bi-directional current flow and four capacitors to produce 53 level single phase inverter. This topology results in reduction of the number of switches, losses and installation area.

Madhav Manjrekar and Thomas A. Lipo "**A hybrid multilevel inverter topology for drive applications"** in proceedings of APEC; 1998 pg 523-9:

This paper presents the investigation on the particular case of a 500 HP induction machine drive based on a seven-level 4.5 kV hybrid inverter. This paper discusses the topological structure of the proposed system, its operating principle, various design criteria, spectral structure and other practical issues such as capacitor voltage balancing.

The proposed topology is a combination of a GTO inverter with a **3** kV DC source and an IGBT inverter with a 1.5 kV DC source. Using appropriate modulation strategy, it is possible to synthesize stepped waveforms with seven voltage levels viz. -4.5 kV, -3 kV, -1.5 kV, 0, 1.5 kV, 3 kV, 4.5 kV. A hybrid modulation strategy which uses stepped synthesis along with variable pulse width of the consecutive steps is presented. Under this modulation strategy, the GTO inverter is modulated to switch only at fundamental frequency of the inverter output, and the IGBT inverter is modulated to switch at a higher frequency so as to provide additional improvements in the waveform quality. The proposed approach offers the same number of levels at the output with a least number of primary devices and dc voltage sources.

In this paper the conventional cascaded H-bridge inverter is modified by providing DC voltage sources in an increasing fashion so as to generate maximum output voltage. The proposed topology is simulated in matlab software and as proposed the higher voltage levels are synthesized using GTO inverters by connecting the higher DC voltage source of 3KV to the GTO inverters which are timed to trigger when higher voltages are required and lower voltage levels are synthesized using IGBT inverters by connecting the basic DC voltage source of 1.5KV to the IGBT inverters to generate first voltage level at the output.

Advantage of the proposed topology is that a seven level inverter voltage is generated with only two DC sources thus reducing the cost and effort spent in capacitor voltage balancing. It also allows usss to use less number of switches for the same number of levels further reducing the switching losses.

Jawad faiz, senior member, IEEE, and Behzad Siahkolah "**New solid-state on load tap-changers topology for Distribution transformers**" IEEE transactions on power delivery, vol. 18, no. 1, January 2003:

This paper focuses on the high controllability advantages of the power electronic switches which lead to their application in the tap-changer of distribution transformers. Using such switches leads to quick operation of the tap-changer and thus, improved performance. This in turn reduces maintenance and repair costs of tap-changers.

Proposed topology has many steps with fewer power electronic switches compared with the existing concepts. The possibility of extension or series connection of this basic unit has been studied. It is shown that the structure consisting of the windings with three taps is the best case to keep the minimum switches (or number of taps) for a certain number of voltage steps. However, the structure consisting of series windings with two taps is optimal from the switch standing voltage point of view.

In this paper the authors have compared a few topologies so as to get to a conclusion on which topology gives an optimal result focussing on three main criteria namely; number of taps required in each basic unit so as to get maximum voltage steps, if the number of voltage values is fixed then which structure provides the optimal result using minimum number of taps, and finally the switches with minimum voltage ratings to be used.

The suggested structure has been compared with the previously proposed concepts in tap-changers and it was found that it produces higher number of voltage steps with lesser number of switches and low standing voltages.

E.A. Mahrous, N.A. Rahim and W.P. Hew "**Three phase three level voltage level inverter with low switching frequency based on the two level inverter topology**" IET Electr. Power Appl., 2007, 1, (4), pp. 637–641

In this paper a new configuration of the three-phase three-level voltage source inverter to reduce the harmonic components of output voltage and load current has been presented. The proposed inverter is based on the two-level inverter. The inverter is built of one two-level conventional inverter, an auxiliary circuit which comprises of three bidirectional switches, and two bulk capacitor banks. A selected harmonic elimination (SHE) control scheme is employed to achieve lower harmonic contents in the inverter output waveforms. The proportional-integral-derivative (PID) control is also designed and implemented in the case

of step response. The dynamic responses of load waveforms because of the step change are improved. Further a low power prototype inverter has been designed and implemented to verify the proposed method. The simulation and experimental results show that THD of the proposed inverter is considerably alleviated.

2.2 Problem statement and problem solving topology

Many industrial applications and motor drives requiring medium voltage and high power levels use multilevel inverter structure as it is not possible to connect only single power semiconductor topology directly to high power grid. Due to the growing voltage and power levels, the multilevel inverters of higher levels need to be used.

A cascaded H-bridge multilevel inverter is a series connection of H-bridge inverters. Cascaded H-bridge MLI has advantages of using separate DC sources, eliminating the use of diodes and capacitors and modularity of controlling each H-bridge independently thus reducing the complexity as compared to other Multilevel inverter configurations.

The conventional cascaded H-bridge multilevel inverter require 2(m-1) switches, where m represents the number of levels. Hence as the voltage levels increase the number of power semiconductor switches to be used also increases. Even if switches of low voltage rating are made use of, each switch requires its own gate driver circuit. This causes the overall system to be more complicated and expensive.

Problem solving methodology: To overcome the problem of complexity and cost in designing of switches for higher levels of multilevel inverter, new method to generate higher voltage levels with lesser number of switches is being proposed in my work.

A concept of sub-multilevel (basic unit) inverter is presented. In this method, basic units are cascaded so as to get multiple levels of DC voltages at the input of an H-bridge inverter, which further results in the multilevel inverter output. According to this method, for a 7-level multilevel inverter, three separate DC sources are used with total ten switches; six in the basic units and four in the output H-bridge to get the required 7-level AC output.

This topology uses ten switches as compared to the conventional cascaded H-bridge inverter which requires a total of twelve switches. This difference in the number of power semiconductor switches increases for higher voltage levels.

3. Multilevel Inverter Structures

3.1 Cascaded H-Bridge Inverters

Every separate dc source (SDCS) is associated with a single phase full bridge, or H-bridge inverter. Every inverter level can produce three distinctive voltages +V dc 0 and -Vdc by associating the dc source to the alternating current output by various combinations of the four switcheskS1, kS2, S3, and S4 . The Alternating current outputs of each of the distinctive full bridge inverter levels are associated in arrangement such that the combined voltage wave form is the aggregate of individual inverter outputs. The quantity of output stage voltage levels m in a cascaded inverter is characterized by m =k2s+1, where s is the quantity of particular DC sources. An illustration stage voltage waveform for a 11klevel full H-bridge inverter with five separate DC source andk5 full bridge is shown below.

Cascaded inverters are perfect for interfacing renewable energy sources with an alternating current grid, as a result of the requirement for discrete DC sources, which is the situation in applications, for example, photo-voltaics, wind etc. Cascaded inverters have likewise been proposed for use as the main traction drive in electric vehicles, where a few batteries or ultra capacitors are appropriate to work as SDCSs.

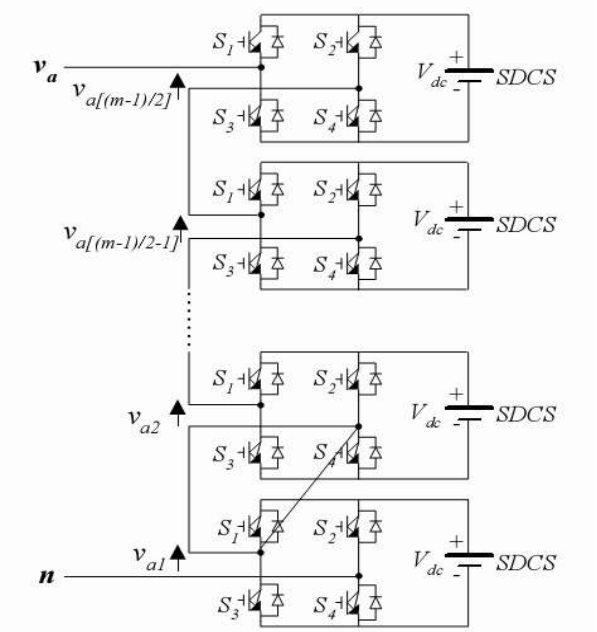


Figure: Single-phasekstructure ofka multilevel cascaded H-bridge inverter.

Pros and Cons of CMLI

Pros

- Dc busk regulation is simple.
- Modularity of control can be accomplished. Unlike the diode clamped and capacitor clamped inverter where the individual stage legs must be modulated by a central controller, the full bridge inverters of a cascaded structure can be modulated independently.
- Requires minimal number of segments among every single multilevel converter to accomplish the same number of voltage levels.

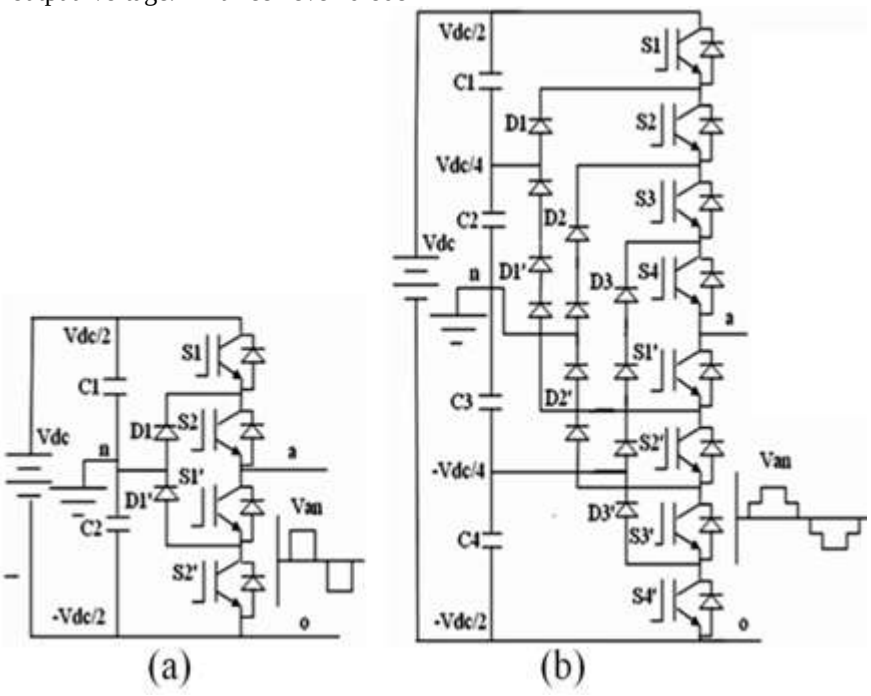
Cons

- Communication between the full-bridges is required to accomplish the synchronization of reference and the carrier waveforms.
- It needs separate dc sources for real power conversions, and in this way its applications are to some degree restricted.

3.2 Diode Clamped Multilevel Inverter

The most normally utilized multilevel topology is the diode clamped inverter, in which the diode is utilized as the clamping device to clamp the dc bus voltage to accomplish multiple stages of the output voltage. A three level diode clamped inverter comprises of two sets of switches and two diodes. Every switch set works in complimentary mode and the diodes are used to give access to mid point voltage. In a three level inverter each of the three periods of the inverter shares a typical DC bus, which is subdivided by two capacitors into three levels. The DC bus voltage is part into three voltage levels by utilizing two series arrangement of DC capacitors. The voltage stress over every switching device is constrained to Vdc through the clamping diodes Dc1kandkDc2

In general, for a N level diode clamped inverter for every leg 2(N - 1) switching devices, (N-1)*(N-2) clamping diodes and (N-1) dc link capacitors are needed. By expanding the quantity of voltage levels the nature of the output voltage is enhanced and the voltage waveform turns out to be nearer to sinusoidal waveform. Despite that, capacitor voltage adjusting will be the basic issue in abnormal state inverters. At the point when N is adequately high the quantity of diodes and the quantity of switching devices will increase and make the system impractical to execute. In the event that the inverter keeps running under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes turns into the real design challenge. In spite of the fact that the structure is more complex than the two level inverter, the operation is similar.



Diode clamped inverter (a) three level inverter, (b) five level inverter

Advantages and Disadvantages of Diode Clamped Multi Level Inverter

Advantages:

1. The majority of the phases share a common dc bus, which minimizes the capacitance necessities of the converter. Thus, the back to back arrangement is not only possible but also practical for utilizations, for example, a high voltage back to back inter-connection.

2. At the point when the quantity of levels is sufficiently high, harmonic content will be sufficiently low to stay away from the requirement for filters.

Disadvantages:

1. Real power flow is troublesome for a single inverter on the grounds that the intermediate direct current levels will tend to discharge or overcharge without exact observation and control.

2. Quadratic relation between the number of diodes and the number of levels is difficult to calculate, especially when number of levels gets higher.

4. Conclusion

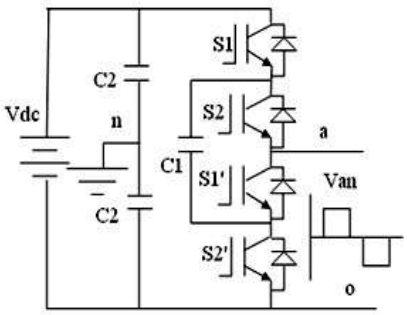
The diode clamped inverter gives various voltage levels through association of the phases to a series combination of capacitors. The idea can be stretched out to any number of levels by expanding the quantity of capacitors. Early explanation of this topology were resitricted to three-levels where two capacitors are associated over the DC bus bringing about one extra level. The extra level was the neutral of the dc transport, therefore the term neutral point capacitor (NPC) inverter was presented. Nevertheless, with even number of voltage levels, the neutral is not available, and the word multiple point clamped (MPC) is now and then connected. Because of capacitor voltage adjusting issues, the diode clamped inverter usage has been constrained to three levels. Due to modern advancements in the course of recent years, the three level inverter is presently utilized widely as a part of mechanical application.

3.3 Flying Capacitor Multi Level Inverter

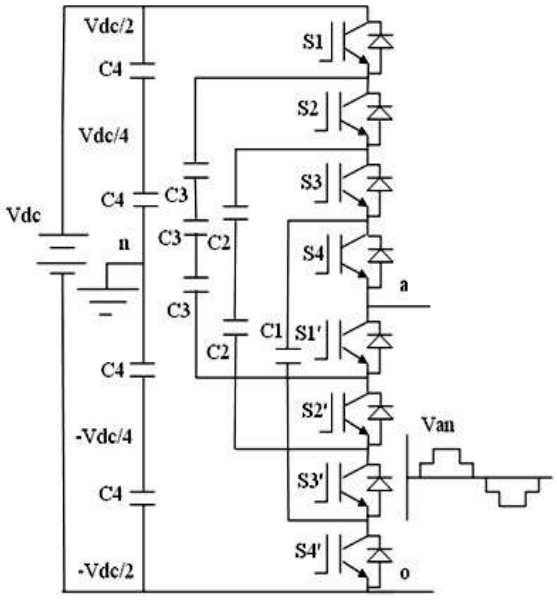
The capacitor clamped inverter on the other hand known as flying capacitor was proposed by Meynard and Foch ink1992. The structure of this inverter is similar to that of the diode-clamped inverter aside from that as opposed to utilizing clamping diodes, the inverter utilizes capacitors. The flying capacitor multilevel inverter includes arrangement association of capacitor clamped switching cells. This topology has a stepping stool structure of dockside capacitors, where the voltage on every capacitor varies from that of the next capacitor. The voltage increase between two neighbouring capacitor legs gives the extent of the voltage steps in the output waveform.

As compared to the diode-clamped inverter, the flying-capacitor inverter does not require the majority of the switches that are on (conducting) in a continuous series. Additionally, the flying-capacitor inverter has phase redundancies, though the diode-clamped inverter has just line-line redundancies.

These redundancies permit a decision of charging/ discharging particular capacitors and can be joined in the control system for adjusting the voltages over the different levels.



(a)



(b)

Advantages and Disadvantages of (FCMLI)

Advantages

Contrasted with the diode-clamped inverter, this topology has a few one of a kind and appealing elements as portrayed beneath:

1) Excessive clamping diodes are not required.
2) It requires one and only one dc source because it has switching frequency inside the phase, which can be utilized to adjust the flying capacitors.
3) Without the utilization of the transformer, the required number of voltage levels can be accomplished.
4) This helps with diminishing the power losses and again lessens the expense of the converter.
5) Unlike the diode clamped structure where the arrangement series of capacitors have the same voltage, in the capacitor-clamped voltage source converter the capacitors inside a phase leg are charged to various voltage levels.
6) Reactive and real power stream can be controlled.
7) The vast number of capacitors empowers the inverter to ride through deep voltage sags and brief length blackouts.

Disadvantages

1) Initializing the converter i.e., before the converter can be modulated by any modulating plan the capacitors must be setkup with the required voltage level as the underlying charge. This makes the complexity in the

balance procedure and turns into a prevention to the operation of the converter.
2) To track the voltage levels for the all part of the capacitors, Controlling is complicated.
3) Pre charging the majority of the capacitors to the same voltage level and start up are unpredictable.
4) For real power transmission, switching efficiency and usage are poor.
5) Rating of the capacitors is a design challenge, Since the capacitors have vast portions of the dc bus voltage across them.
6) In multilevel diode-clamped converters the huge quantities of capacitors are both more costly and cumbersome than clamping diodes.
7) Packaging is additionally more troublesome in inverters with a higher number of levels

5. Conclusion

The point of this part has been to show the multilevel converter topologies. Each has its own blend of focal points and burdens and for any one specific application, one topology will be more proper than the others. Regularly topologies are picked in light of what has improved some time recently, regardless of the possibility that that topology may not be the best decision for the application.

6. Block Diagram and its Explanation

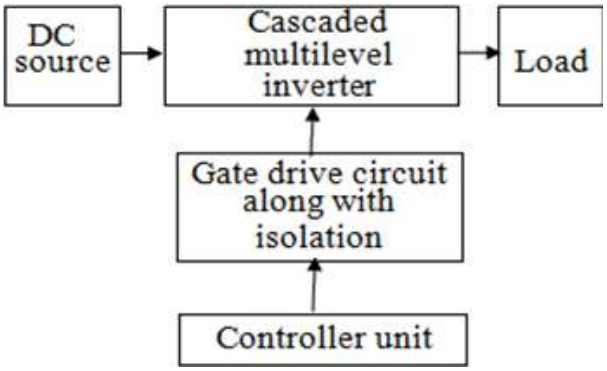


Figure: Block diagram of the proposed system

The block diagram for the proposed cascaded multilevel inverter topology with reduction in the number of switches is shown in the figure above. A separate DC power supply is given to the controller unit and gate drive circuit. The required switching sequence for the ten switches is designed in the controller unit and output of which is given to gate drive circuit through an isolation circuit. Isolation circuit helps in isolating the controller unit from the gate drive circuit. Gate drive circuit amplifies the input signal in to gate pulses which are given as triggering pulses to their respective switches in the inverter topology. Multilevel inverter receives DC supply from a DC source and converts it in to multilevel AC output for the load.

DC power supply: A typical 12V DC supply is given to the controller unit which is in this case a frequency modulator. Separate 5V DC supply is given to the gate driver circuit.

Controller unit: The commands for turn on and turn off for the switches are generated in the logic circuit of the controller unit as required for the application. In this topology controller unit is provided to generate pulses using PWM technique with the help of a reference sine wave generator and a repeating sequence as required. Reference sine wave used is same for all the switches and the repeating sequence to be compared with reference is varied from switch to switch according to the turn on time of each switch respectively.

Gate drive circuit along with isolation: Gate drive circuit amplifies the signals produced by the controller and generates the pulses required for the gate terminal of the corresponding switch. Isolation is usually required for safety and operating conditions when switch voltage floats with respect to ground. Isolation cicuit ensures to isolate the control circuit from the power circuit. Either pulse transformer or opto-isolator can provide isolation. Here opto-isolators are used as they can work in wide range of input signal pulse width.

Multilevel inverter: Multi-level inverter is a power electronic device which is capable of providing desired alternating voltage at the output using multiple lower level DC voltages as an input. It consists of multiple DC sources and switching devices arranged in the manner as shown below in the circuit. MOSFET is used in the proposed method as switching device due to its advantages of higher commutation speed and greater efficiency during operation at low voltages. It can sustain high blocking voltage and maintain high current. In my work I have used three cascaded basic units along with one H-bridge inverter circuit to get a 7-level multilevel inverter output.

Basic unit: In the proposed topology three basic units are being used in cascaded manner. The explanation of one such basic unit along with its circuit diagram is given below.

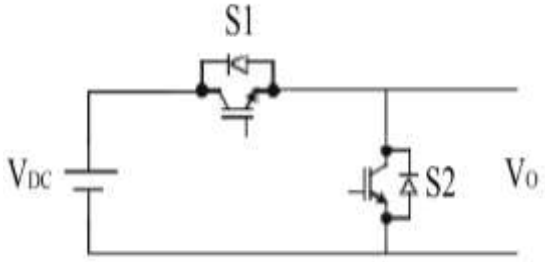


Figure: Basic unit for the proposed topology

V_{DC} is input DC voltage given to the basic unit, S_1 is the series switch and S_2 is the bypass or the parallel switch. A fixed DC voltage will be applied at the input of the basic unit. Each basic unit operates in two modes.

Mode 1: In this mode of operation switch S_1 is turned on and S_2 is turned off. The respective DC voltage is made available at the output side V_o.

Mode 2: This mode comes in to picture when S_2 is turned on and correspondingly S_1 is turned off. The input voltage is blocked from appearing at the output side, hence V_o is zero. Both the switches cannot be turned on simultaneously since it will lead to short circuit.

Values of V_o for states of switches S_1 and S_2 are presented in the following table.

S_1	S_2	V_o
ON	OFF	V_{DC}
OFF	ON	0

Several basic units are cascaded in a manner shown below so as to get different steps of DC voltage values at the output. The number of basic units to be cascaded depends on the voltage levels required at the output. If all the DC voltage sources at the input of 'n' basic units are equal then the inverter is known as symmetric multilevel inverter and the number of steps (N_{step}) at the inverter output is given by $N_{step} = 2n+1$ and the maximum output voltage (V_o) of this n cascaded multi-level inverter is $V_o=n*V_{DC}$. If different DC voltage sources are made use of at the input then the inverter is known as asymmetric multi-level inverter and the number of steps and corresponding output voltage is given by

$N_{step} = 2^{n+1} - 1$… if $V_j = 2^{j-1}V_{DC}$ for j = 1 2 3 ……. n
$V_{o,max} = (2^n - 1)V_{DC}$

In this proposed paper three basic units with different input voltage values are cascaded to get the required output. Hence according to the above formula
$N_{step} = 2^{3+1} - 1 = 7$
$V_{0,max} = (2^3 - 1)V_{DC} = 7*V_{DC}$

Table: All possible values of V_o for different switching states in the cascaded basic units

S1	S2	S3	S4	S5	S6	V_O
OFF	ON	OFF	ON	OFF	ON	0
ON	OFF	OFF	ON	OFF	ON	V_1
OFF	ON	ON	OFF	OFF	ON	V_2
OFF	ON	OFF	ON	ON	OFF	V_3
ON	OFF	ON	OFF	OFF	ON	V_1+V_2
ON	OFF	OFF	ON	ON	OFF	V_1+V_3
OFF	ON	ON	OFF	ON	OFF	V_2+V_3
ON	OFF	ON	OFF	ON	OFF	$V_1+V_2+V_3$

These are the outputs from the cascaded basic units obtained by different combination of switches in on-state and off-state. Thus generated voltage steps are in DC form. So as to obtain AC voltage, this output from the cascaded basic units is further connected to the H-bridge inverter to get the required as shown in the figure below.

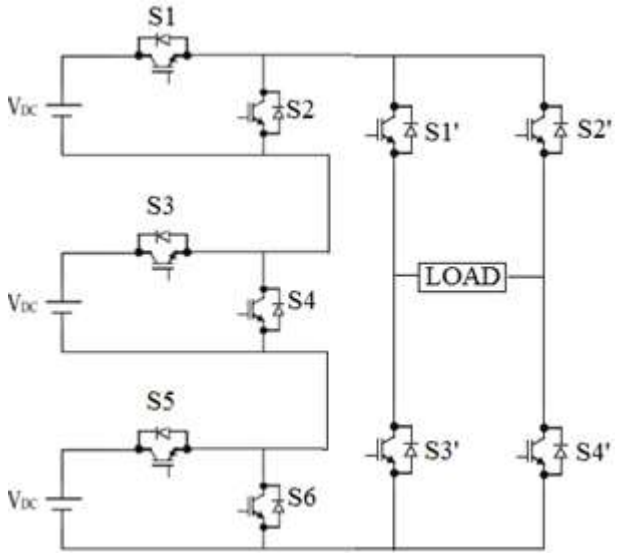


Figure: Circuit diagram of the proposed seven level multilevel inverter

All the possible voltage levels with different combination of switching states of the ten switches is shown below.

Mode 1: In the three basic units if all the series switches S1, S3, S5 are in off state and the corresponding parallel switches S2, S4, S6 are in on state then the total output voltage is zero as all the DC voltage sources are short circuited. Fig: shows the current flow for this mode of operation.

Mode 2: When the series switch S1 in first basic unit and parallel switches S4 and S6 in the second and third basic unit are turned on and correspondingly the parallel switch S2, series switches S3 and S5 are turned off. DC voltage input at the first basic unit, V_{DC1} appears across the input of the H-bridge inverter. Further in H-bridge, switches S1' and S4' are in on state and S2' and S3' are in off state. $+V_{DC1}$ appears across the load which is shown in the fig:

Mode 3: In this mode S1, S4, S6, S2' and S3' are in on state and other switches are in off state. Voltage $-V_{DC1}$ appears across the output which is shown in the fig:

Mode 4: In this mode switches S2, S3, S6, S1' and S4' are in on state and other switches are in off state. Output voltage is $+V_{DC2}$ which is shown in the fig:

Mode 5: In this mode switches S2, S3, S6, S2' and S3' are in on state and other switches are in off state. Output voltage is $-V_{DC2}$ which is shown in the fig:

Mode 6: In this mode switches S2, S4, S5, S1' and S4' are in on state and other switches are in off state. Output voltage is $+V_{DC3}$ which is shown in the fig:

Mode 7: In this mode switches S2, S3, S5, S2' and S3' are in on state and other switches are in off state. Output voltage is $-V_{DC3}$ which is shown in the fig:

Mode 8: In this mode switches S1, S3, S6, S1' and S4' are in on state and other switches are in off state. Output voltage is $+(V_{DC1}+V_{DC2})$ which is shown in the fig:

Mode 9: In this mode switches S1, S3, S6, S2' and S3' are in on state and other switches are in off state. Output voltage is $-(V_{DC1}+V_{DC2})$ which is shown in the fig:

Mode 10: In this mode switches S1, S4, S5, S1' and S4' are in on state and other switches are in off state. Output voltage is $+(V_{DC1}+V_{DC3})$ which is shown in the fig:

Mode 11: In this mode switches S1, S4, S5, S2' and S3' are in on state and other switches are in off state. Output voltage is $-(V_{DC1}+V_{DC3})$ which is shown in the fig:

Mode 12: In this mode switches S2, S3, S5, S1' and S4' are in on state and other switches are in off state. Output voltage is $+(V_{DC2}+V_{DC3})$ which is shown in the fig:

Mode 13: In this mode switches S2, S3, S5, S2' and S3' are in on state and other switches are in off state. Output voltage is -
$(V_{DC2}+V_{DC3})$ which is shown in the fig:

Mode 14: In this mode switches S1, S3, S5, S1' and S4' are in on state and other switches are in off state. Output voltage is $+(V_{DC1}+V_{DC2}+V_{DC3})$ which is shown in the fig:

Mode 15: In this mode switches S1, S3, S5, S2' and S3' are in on state and other switches are in off state. Output voltage is $-(V_{DC1}+V_{DC2}+V_{DC3})$ which is shown in the fig:

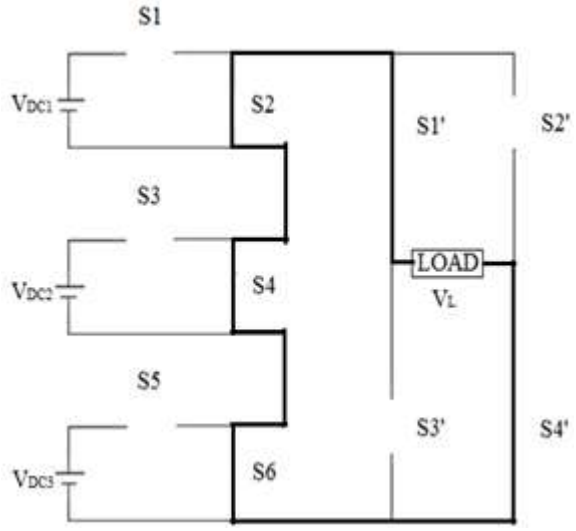


Figure: mode 1operation of circuit

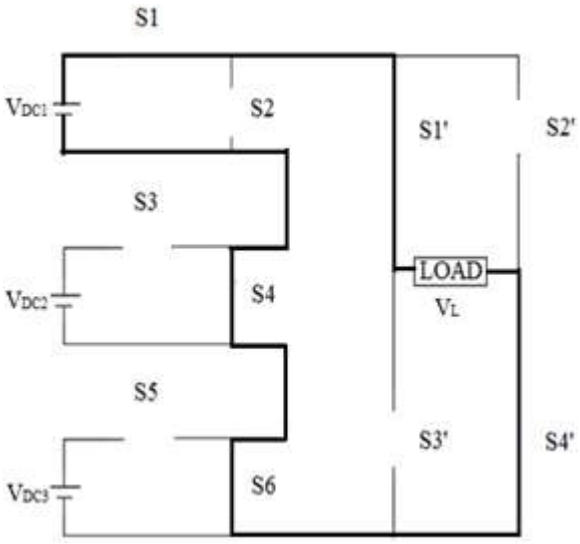


Figure: mode 2 operation of circuit

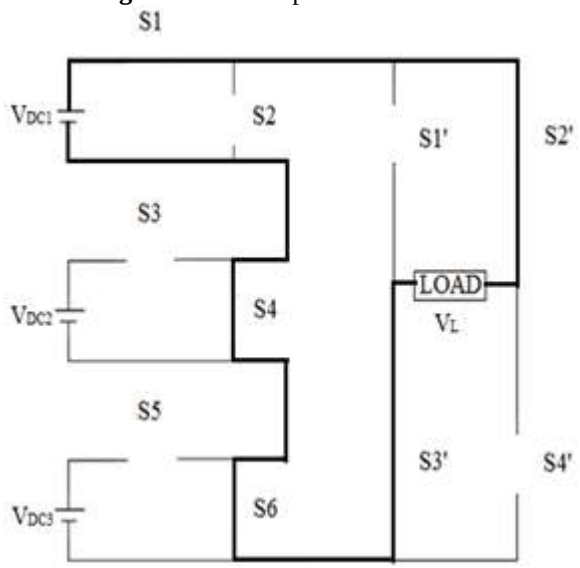


Figure: mode 3 operation of circuit

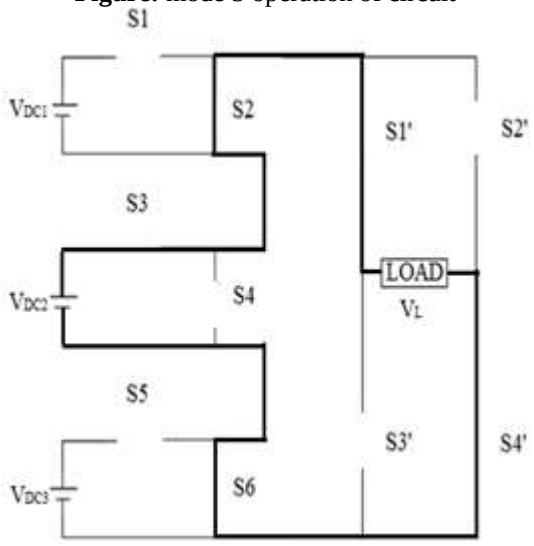


Figure: mode 4 operation of circuit

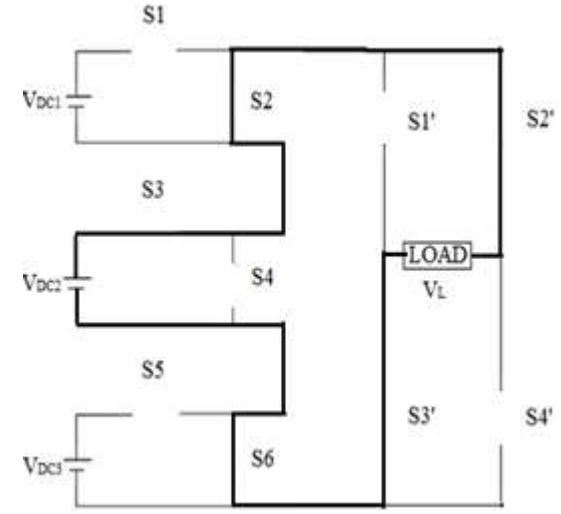


Figure: mode 5 operation of circuit

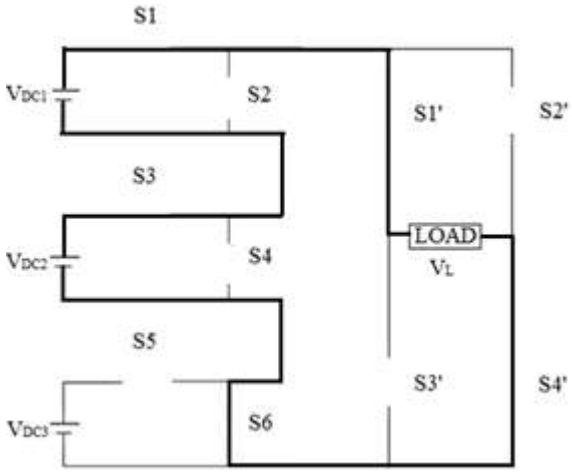


Figure: mode 8 operation of circuit

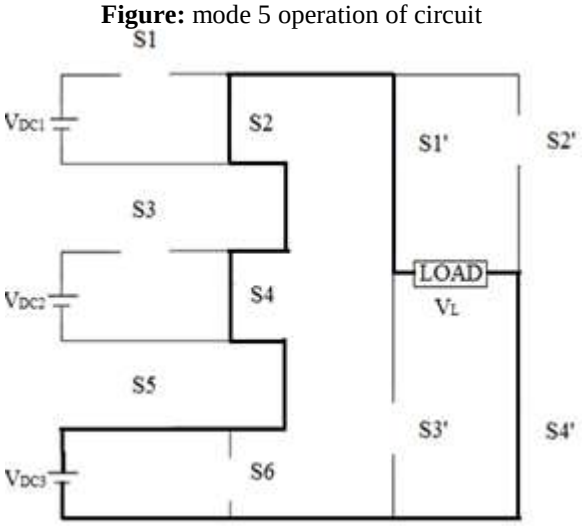


Figure: mode 6 operation of circuit

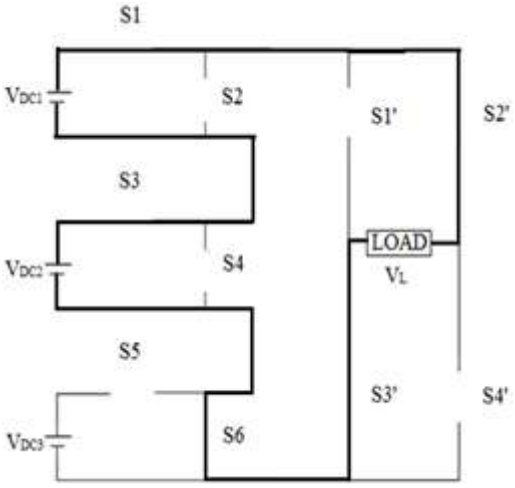


Figure: mode 9 operation of circuit

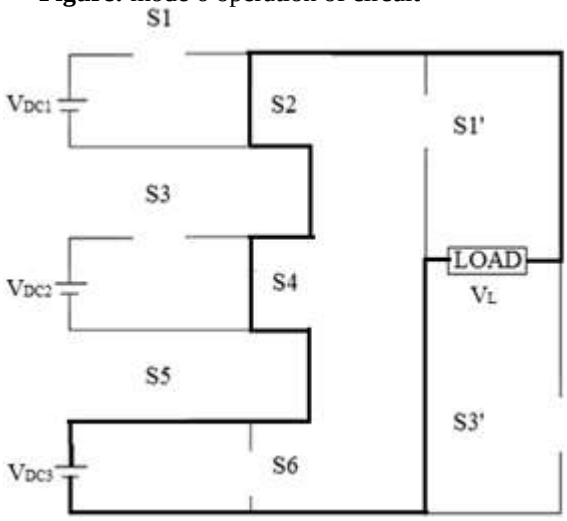


Figure: mode 7 operation of circuit

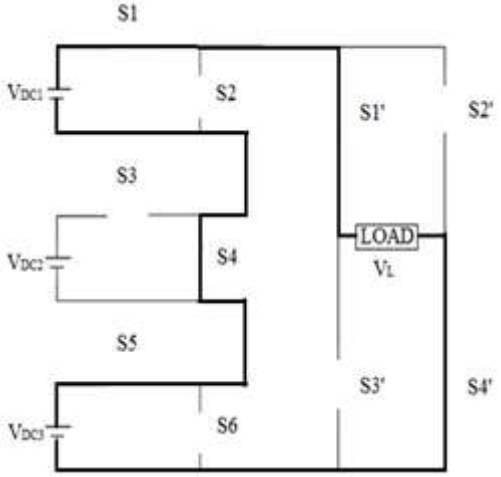


Figure: mode 10 operation of circuit

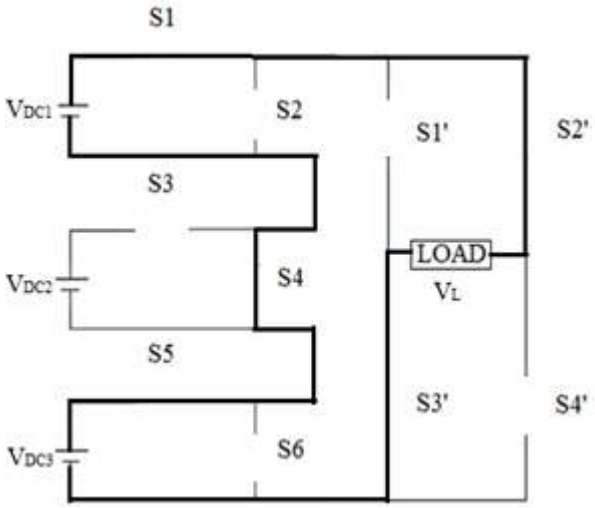


Figure: mode 11 operation of circuit

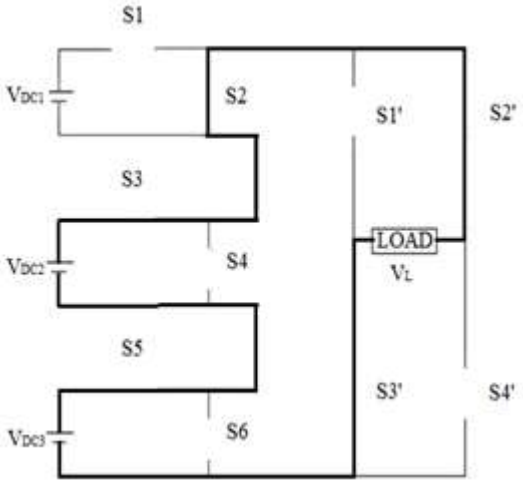


Figure: mode 12 operation of circuit

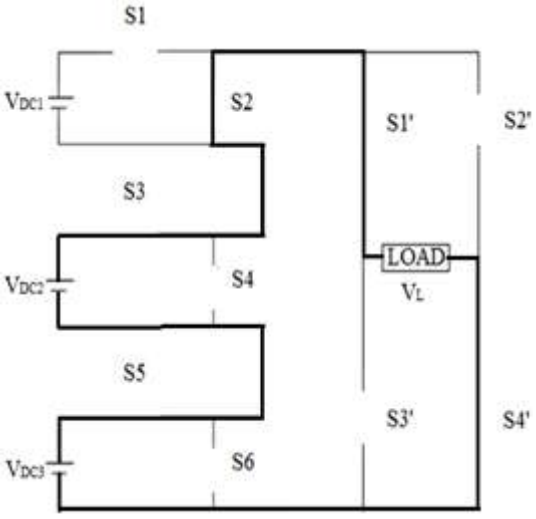


Figure: mode 13 operation of circuit

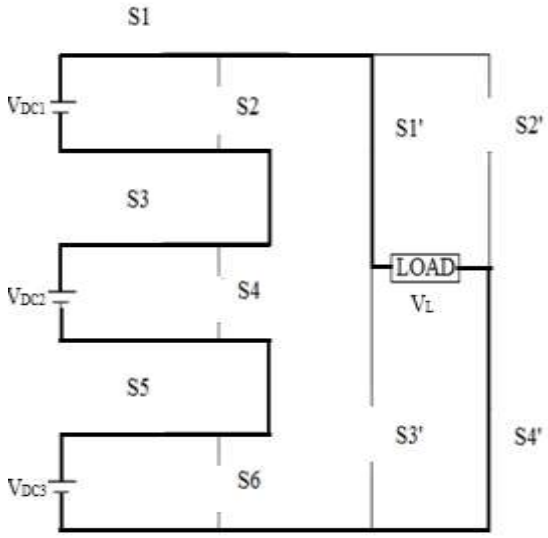


Figure: mode 14 operation of circuit

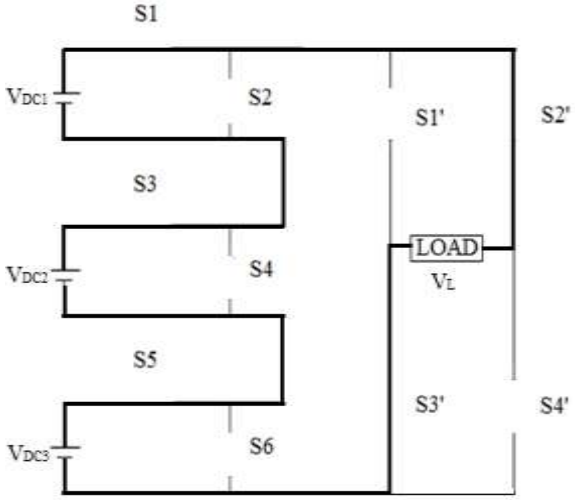


Figure: mode 15 operation of circuit.

DC source: It can be given through a battery or a rectifier after conversion from AC to DC. For a 7-level multilevel inverter to be generated, three separate DC sources must be provided.

Load: The seven step output of the inverter is applied to 100Ω resistance in series with 60mH inductance. The three DC sources used in this topology have different values so as to produce maximum possible voltage steps.

7. MATLAB Simulation and its Results

The name MATLAB stands for matrix laboratory. It was originally written to provide easy access to matrix software developed by the Linpack and Eispack (a software library for numerical computation of eigen values and eigen vectors of matrices). Matlab has evolved over a period of years with the input from many users. It is the most standard instructional tool for introductory and advanced courses in mathematics, engineering and science in the universities. Basically matlab is computer programming language developed by math works for scientific computing. Various software toolboxes from different sources are made available that provide additional functionality needed to solve problems in wide range of disciplines such as image

and video processing, optimization, partial differential equations, signal processing and commutations and more.

For designing the electrical circuits computer simulation plays a very important role before adopting the real physical model. Matlab software enables the computer simulation and virtual experiment to synchronously implement the design and experiment without the restrictions of components. It also facilitates the adjustment of circuit parameters and realizes the updating change of the electric appliance parts, which helps in improving the complete design and predictive results of the circuit under study.

Matlab is integrated with simulink tool kit which provides customized block libraries and solvers for modeling and simulating dynamic systems. Simulink enables to incorporate matlab algorithms into models and export simulation results to matlab for further analysis.

The proposed concept of multilevel inverter with minimum number of switches is simulated by using the MATLAB 7.10.0(2010a). The input provided is V1, V2, V3 of the desired values in the appropriate ratios to get the appropriate output levels of inverter. MOSFET is used as the switching device here. The pulses are generated by comparing a reference sine wave generator with a triangular wave. The pulses for the gate of three MOSFET pairs of the corresponding three basic units are varied or phase shifted by providing different magnitude of operation in the triangular wave. For the H-bridge inverter at the output side, appropriate RL load is connected.

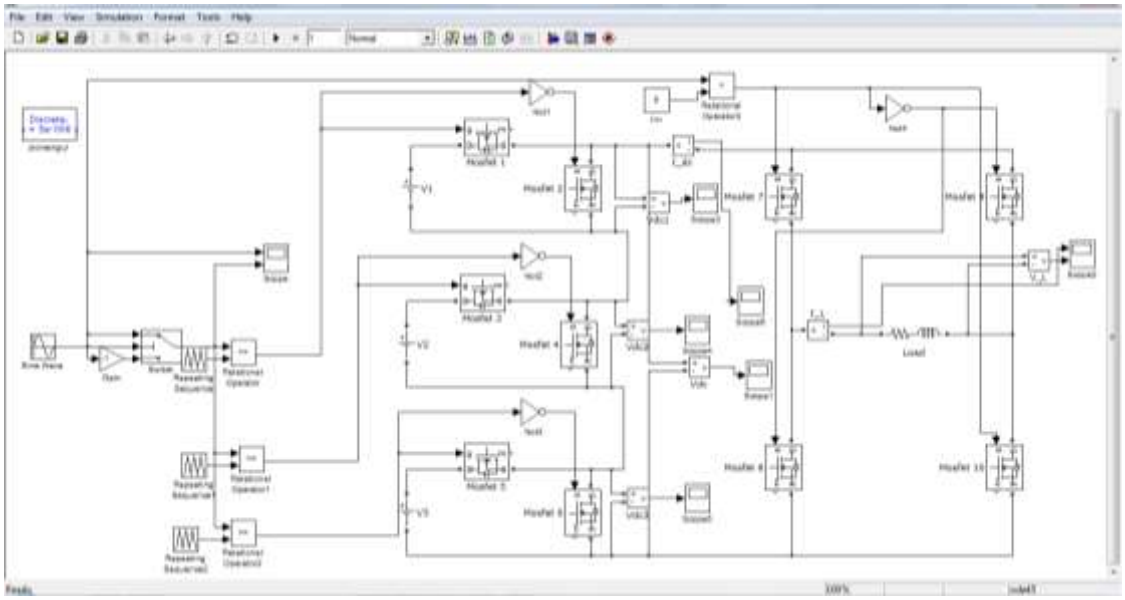


Figure: Matlab simulation of the proposed topology

The above simulink model is generated in the Matlab for a seven level multilevel inverter. It is basically a DC to AC converter. Three basic units with two MOSFET switches, one in series and one in parallel in each basic unit are used. Each MOSFET switch is fed with gating pulses from pulse generator. Gating pulses so generated by three pulse generators are given to the series switches S1, S3, S5 of the basic units and the negated outputs of the same gating pulses are given to corresponding the bypass or the parallel switches S2, S4, S6 respectively.

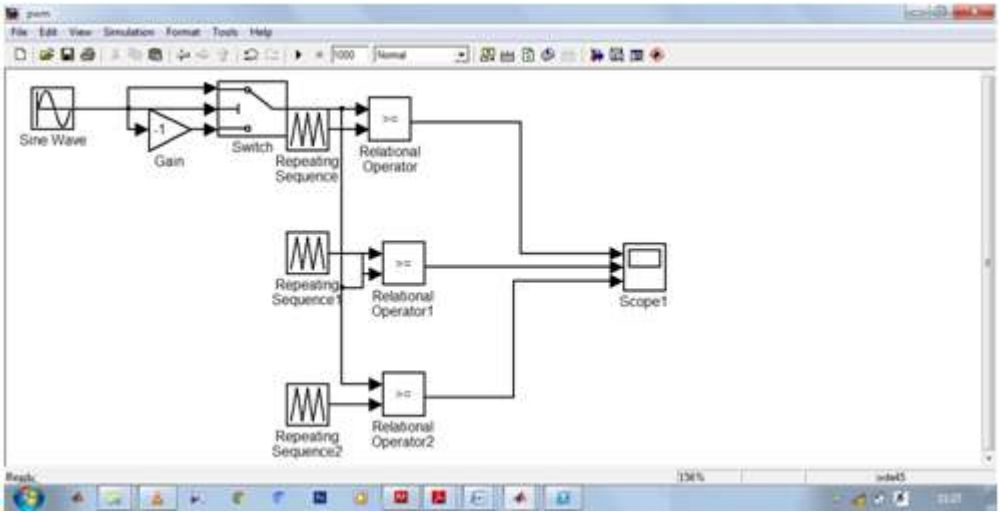


Figure: Simulink model of the gate drive circuit for the MOSFETs in the basic units using PWM technique

Pulse generator used in each basic unit has a reference sine wave and a repeating sequence generator. Here sine wave block is used as the reference unit.
Amplitude: 1
Phase: 0
Frequency: 2*pi*50 = 314.2 rad/sec

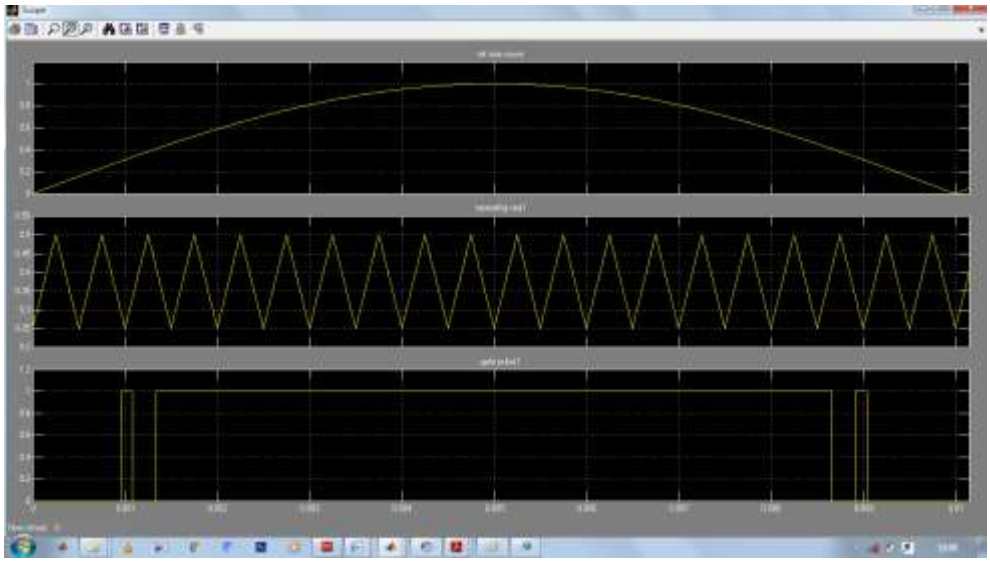
Sine wave block is followed by a gain block and a comparator block which are used to convert the negative half cycle of the sine wave input in to positive so that it becomes easy for comparing it with the repeating sequence which is a positive only triangular wave.

The three repeating sequences have been designed so as to generate the required gate pulses for three MOSFET pairs in the basic units. The magnitudes given for the repeating sequence block are responsible for deciding the pulse width for different switches.

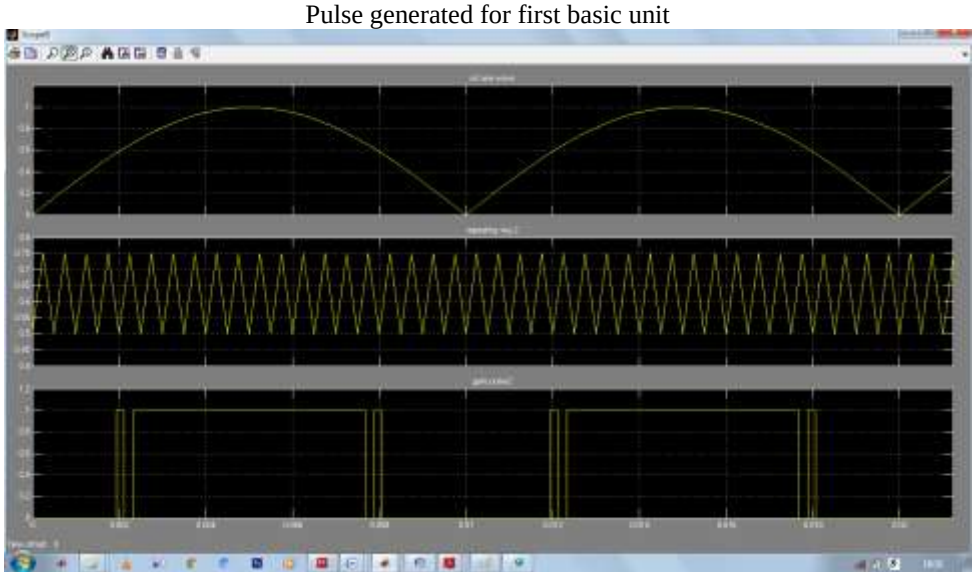
The first repeating sequence is a triangular wave with its tip magnitudes varying as 0.25 0.5 0.25 with the time slots of [0 1/2e3/2 1/2e3]. This block generates a triangular wave sequence with a time period of $1/20^{th}$ of the sine wave sequence. Hence for each half cycle of sine wave twenty triangular waves are generated. These two wave generators are fed to a comparator block where a rectangular wave pulse is generated. The rectangular pulse so generated contains a time slot for which sine wave is greater than triangular wave.

The second repeating sequence is a triangular wave with its tip magnitudes varying as 0.5 0.75 0.5 with the time slots of [0 1/2e3/2 1/2e3]. Thus as the magnitudes of triangular wave for second basic unit are higher, the pulse width of the rectangular wave pulse at the comparator output is lesser than that of the first pulse generator because the time for which the sine wave is greater than the repeating triangular wave is decreased.

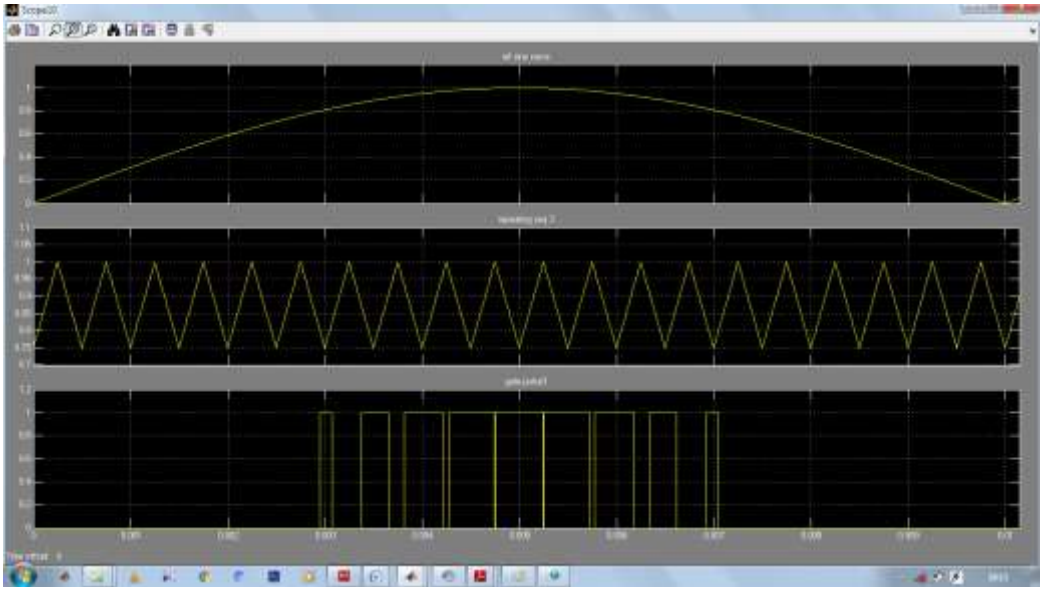
The third repeating sequence is a triangular wave with its magnitudes varying as 0.75 1 0.75 with the time slots of [0 1/2e3/2 1/2e3]. Similarly as the magnitudes are even more higher the pulse generated at the comparator output has lesser pulse width than the first and second pulse width generator block.



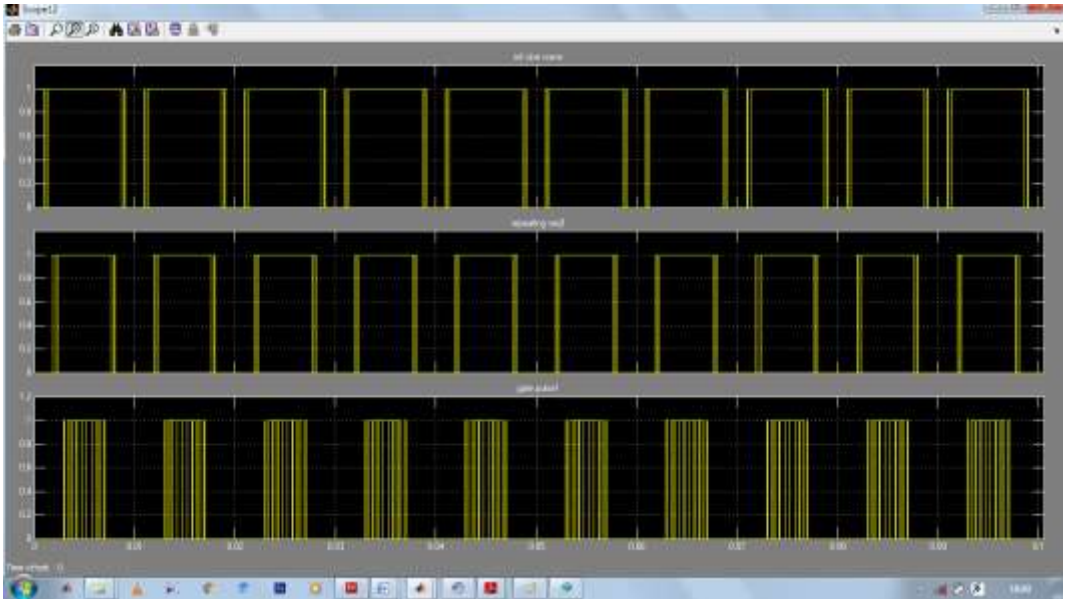
Pulse generated for first basic unit



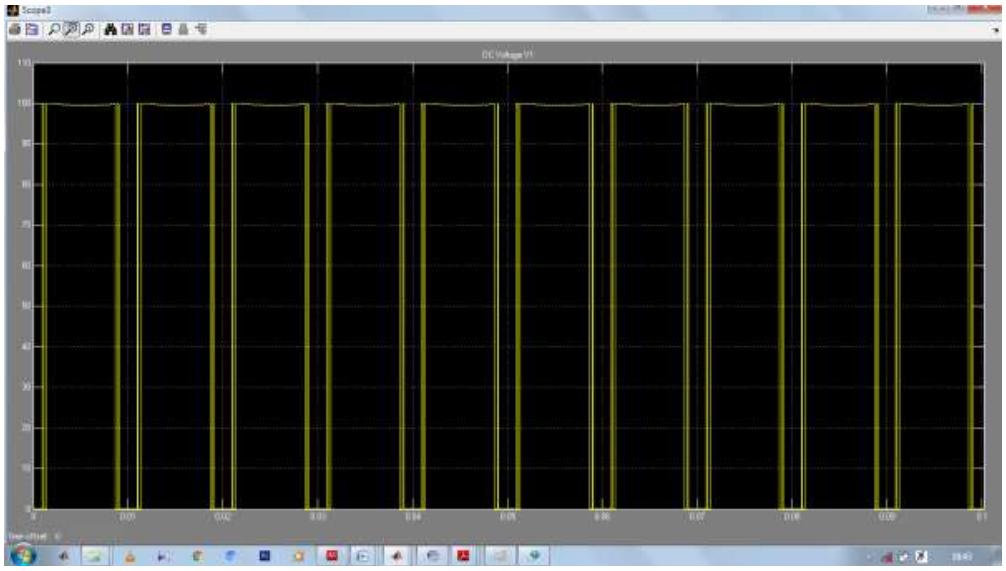
Pulse generated for second basic unit



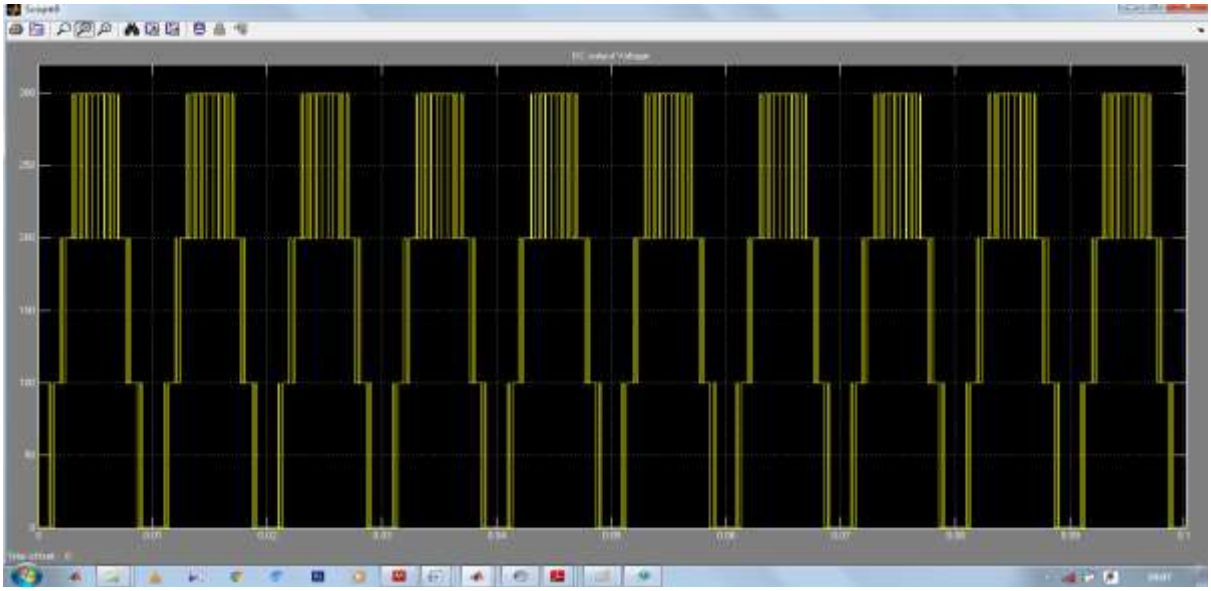
Pulse generated for third basic unit



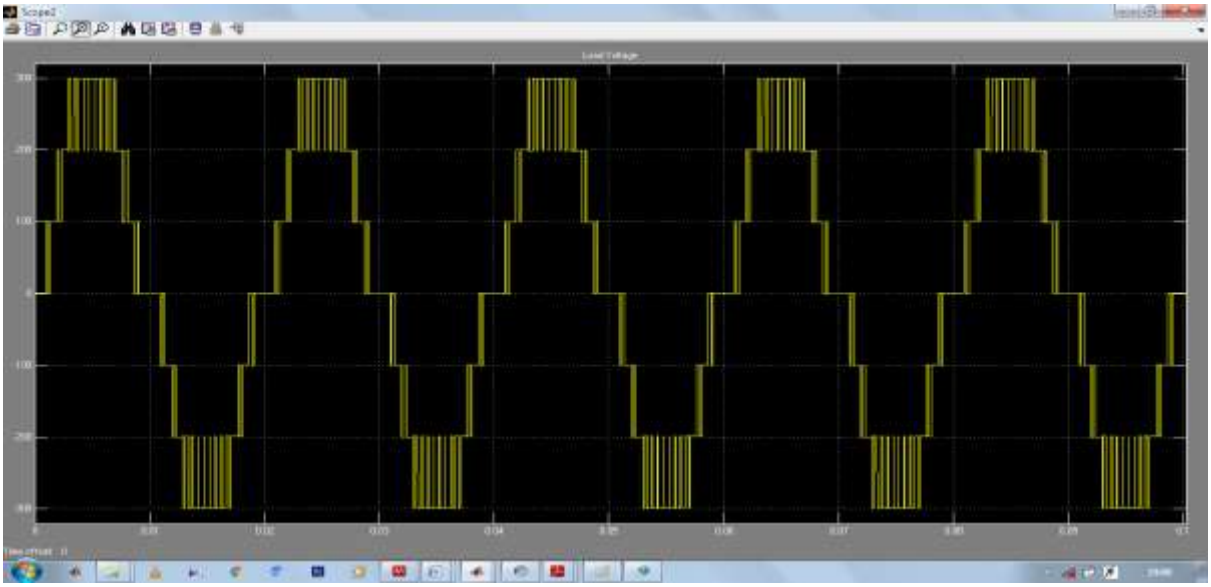
Gating pulses for the three pairs of MOSFETs



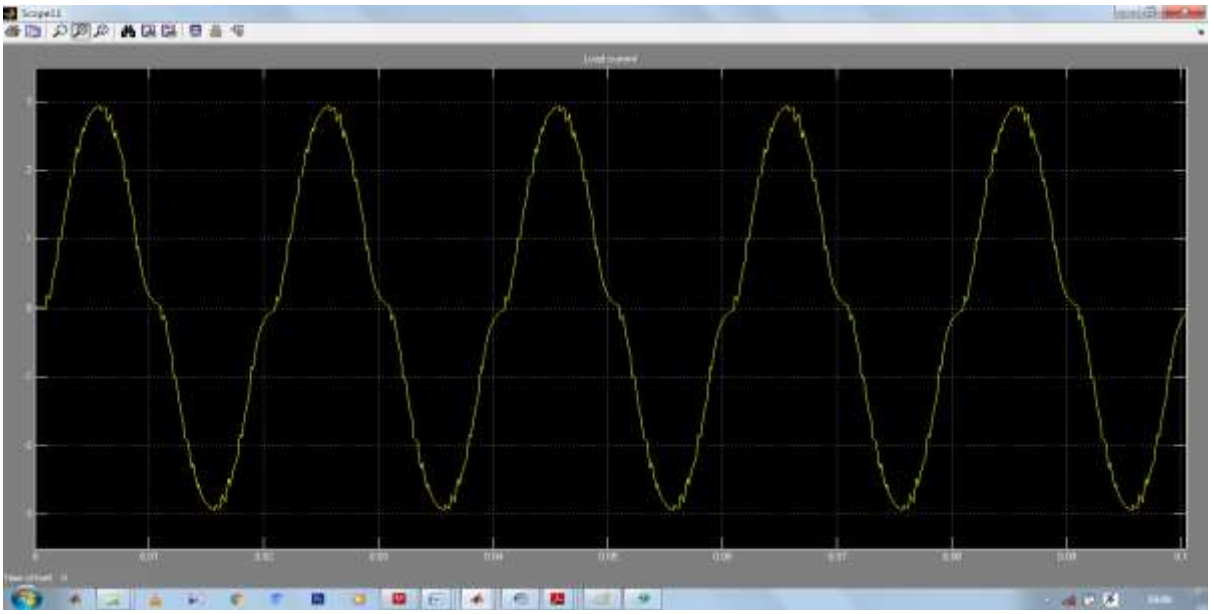
DC voltage at the output of each basic unit with DC source voltage of 100V



DC output voltage at the input of the H-bridge inverter unit

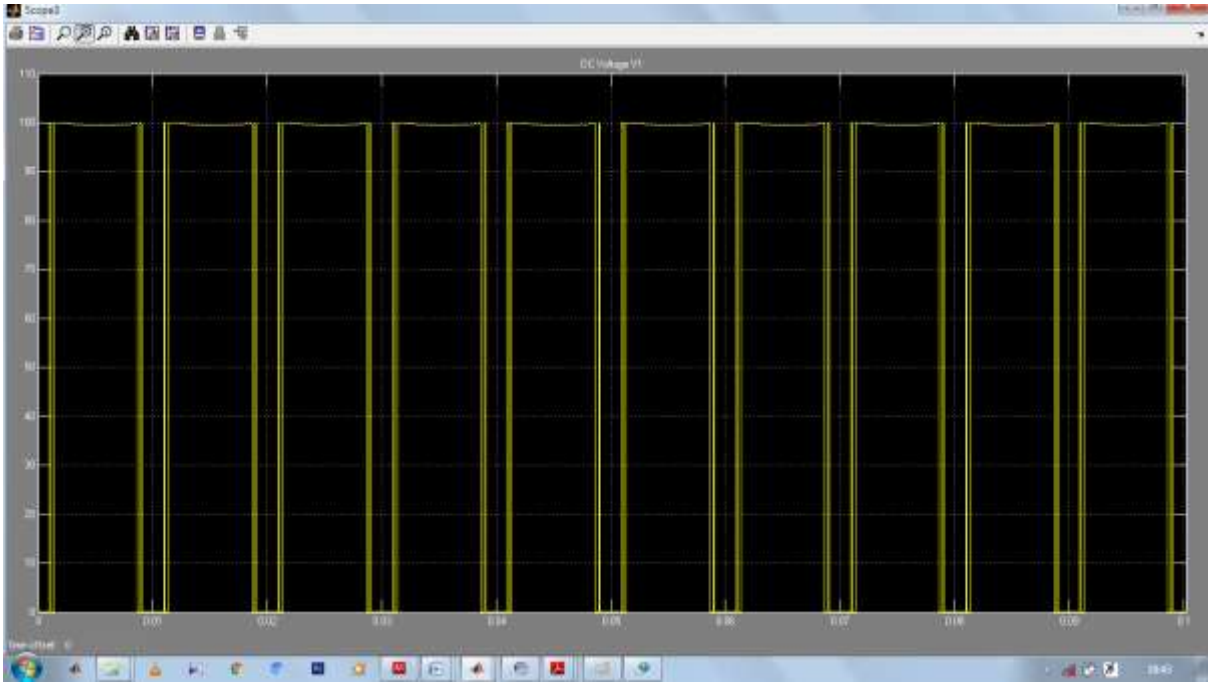


Output voltage waveform at the output of H-bridge inverter

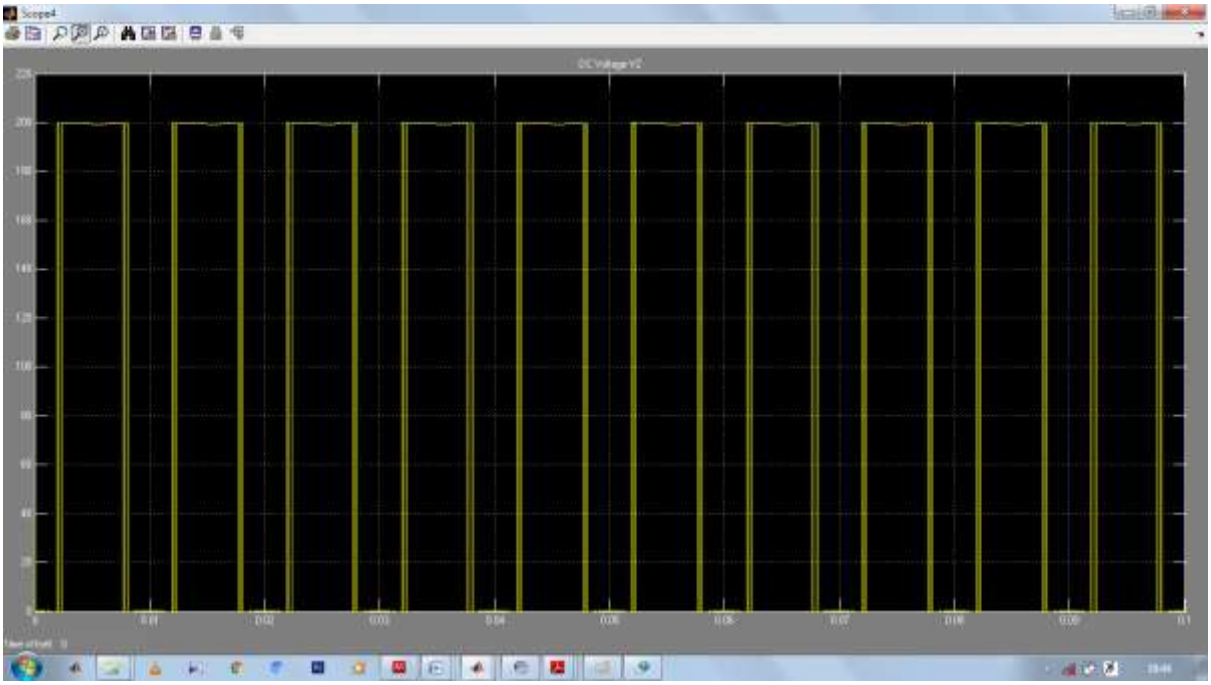


Output current waveform at the output of H-bridge inverter

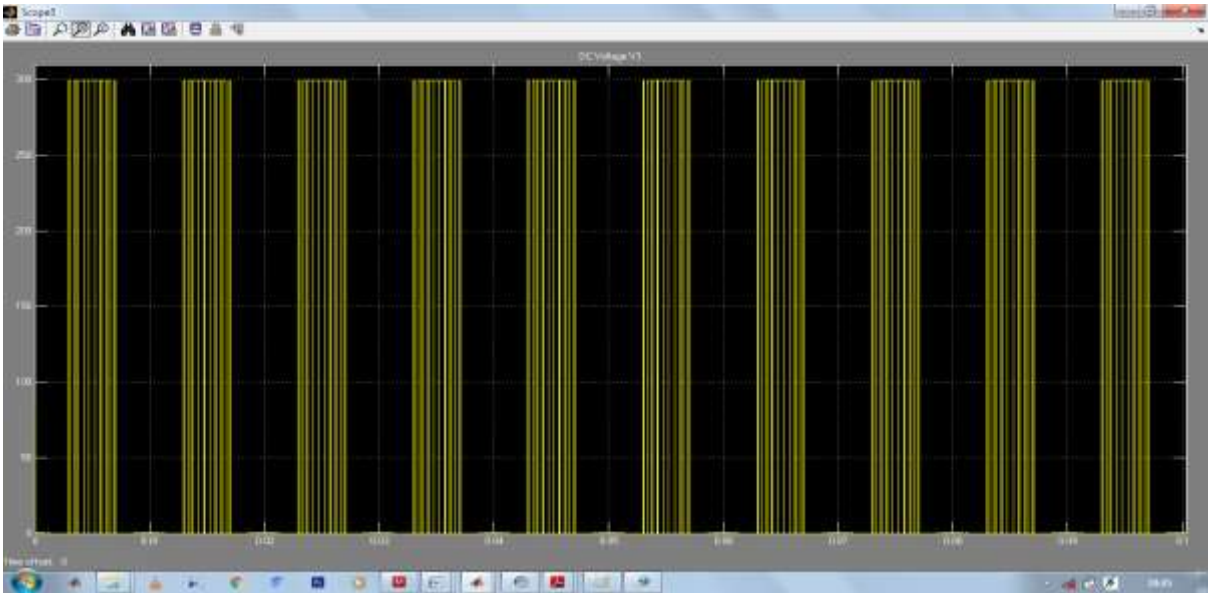
The above waveforms at the different stages of the circuit are obtained when the DC sources used are of same magnitude. Hence it is called as symmetric multilevel inverter. To generate asymmetric multilevel inverter, the inputs used must be of different values. As previously stated the DC sources used in the pattern as $V_j = 2^{j-1}V_{DC}$ for j = 1 2 3 ……. N we have, V_1=100 V_2=200 V_3=300. Asymmetric multilevel inverter is used so as to further increase the output voltage magnitude keeping the number of switches same as in the symmetric multilevel inverter. Here the switching devices receive the same switching pulses as in the symmetric multilevel inverter. Hence the output voltage and current waveforms for the asymmetric seven level multilevel inverter are as shown below.



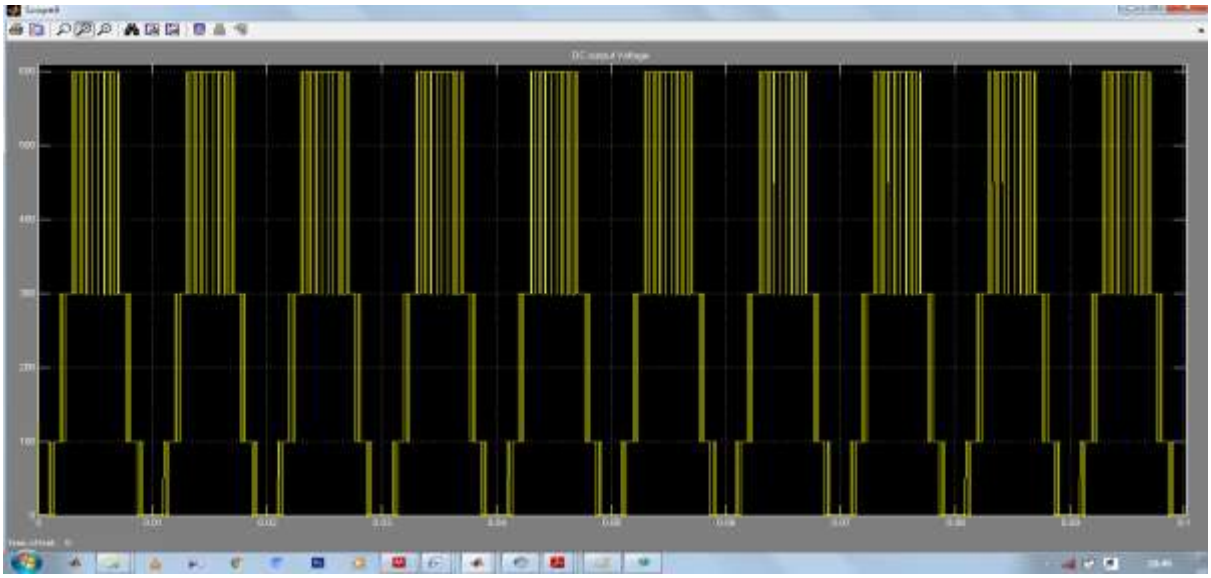
DC voltage at the output of first basic unit with DC source voltage of 100V



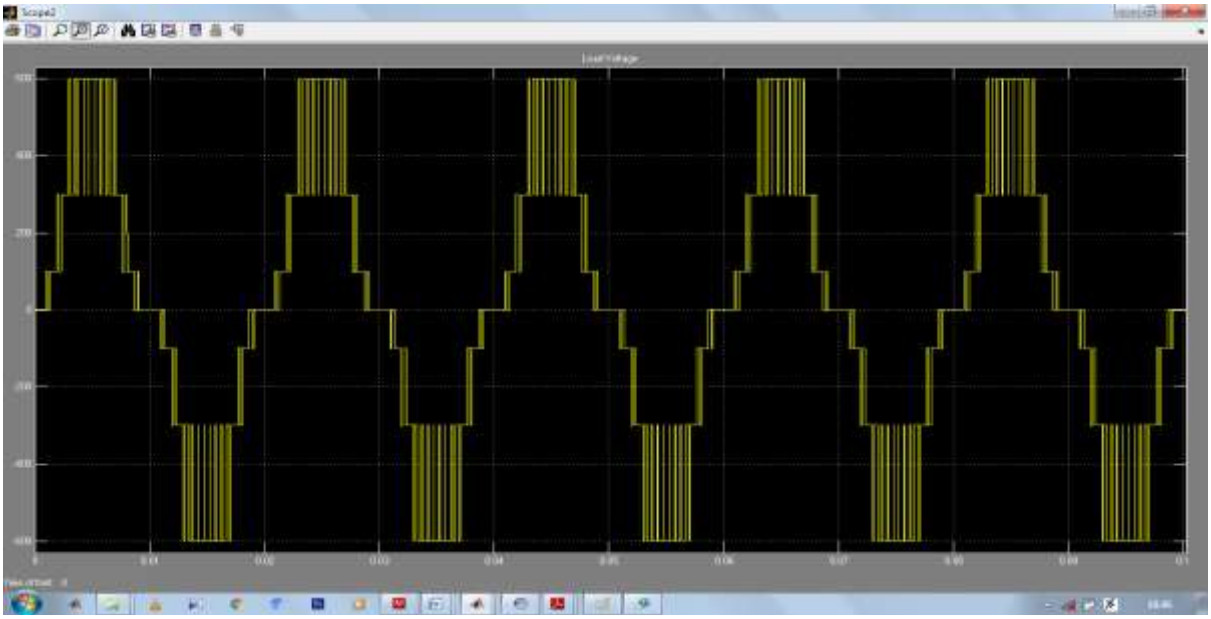
DC voltage at the output of second basic unit with DC source voltage of 200V



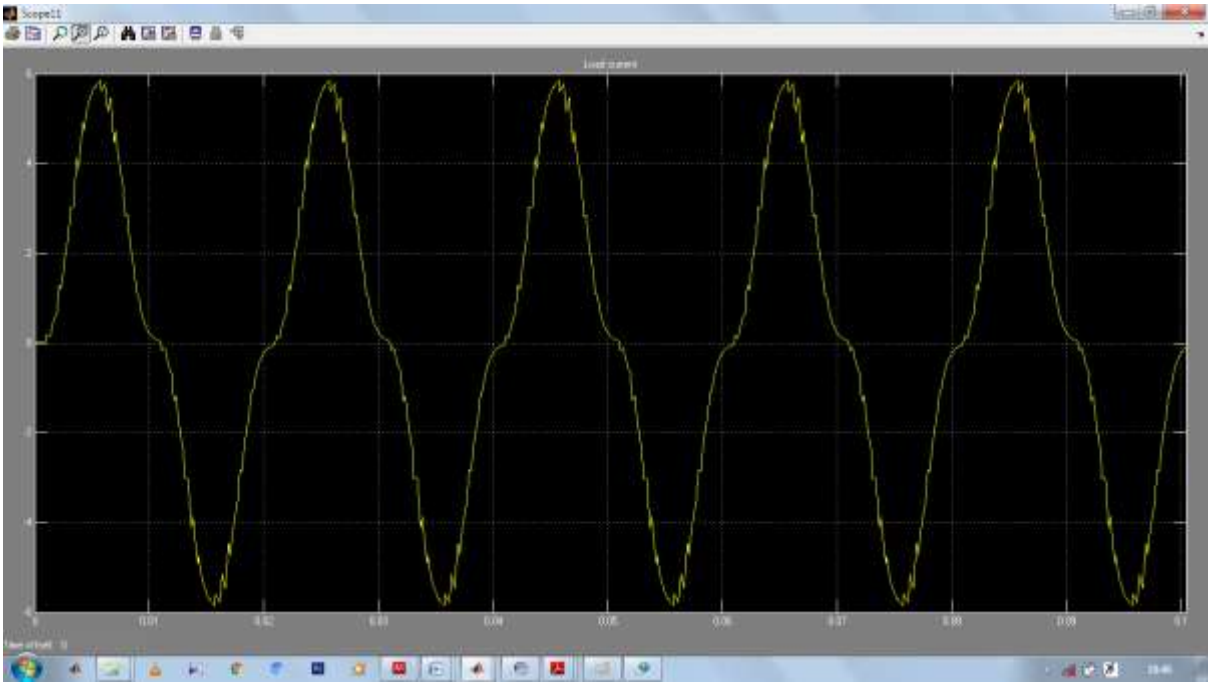
DC voltage at the output of third basic unit with DC source voltage of 300V



DC output voltage at the input of the H-bridge inverter unit



Output voltage waveforms at the output of H-bridge inverter



Output current waveform at the output of H-bridge inverter

8. Advantages Applications and Expected Results

Advantages

- Cost effective
- Simpler control unit
- Reduced harmonic content
- Used to generate higher magnitude of voltages
- Increased power handling capability at higher voltages due to use of high voltage high power semiconductor devices

Applications

- Adjustable speed motor drives
- Higher voltage inverters ranging from 11KV to 16KV can be used at power grid distribution level
- Distributed energy systems, especially those using renewable energy sources can make use of this topology with simpler design

9. Conclusion and Future Scope

In this dissertation work a new basic unit is proposed. Then, by series connection of basic units new 7-level cascaded multilevel inverter is proposed. This inverter only generates positive levels at the output. In-order to generate all positive and negative voltage levels, an H-bridge is added to the proposed inverter. The proposed topology requires less number of MOSFETs, driver circuits, and DC voltage sources. That leads to reduction in the installation space and total cost of the inverter decreases.

In this work symmetric and asymmetric arrangement of seven-level cascaded multilevel inverter simulation is developed using MATLAB/SIMULINK 2010a. The output of both symmetric and asymmetric cascaded multilevel inverter is compared. The comparison result shows that the output voltage of asymmetric multilevel inverter is more than that of symmetric multilevel inverter with the same number of switches.

10. Future Scope

1) In 7-level cascaded multilevel inverter we used three basic units. In 21-level cascaded multilevel inverter we can use ten basic units which require 19 swicthes lesser than that used in the conventional cascaded H-bridge inverter.
2) Multilevel inverter with fuel cell in place of dc sources has a greater scope in applications involving electrical vehicles.
3) Due to time constraint I designed only simulation of 7-level cascaded multilevel inverter with reduced number of switches. In future we can develop hardware. Further for each DC source a boost inverter circuit can be added so as to increase the voltage magnitude at the input itself.