International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391

Three Level Single Stage PFC Converter

Sushma[1], Dr. M. S. Aspalli[2]

[1]PG Scholar, Dept of EEE, Poojya Dodappa Appa Collage of Engineering, Kalaburagi, Karnataka, India

[2]Dr.M.S.Aspalli, Dept of EEE, Poojya Dodappa Appa Collage of Engineering, Kalaburagi, Karnataka, India

Abstract: ***DC power supplies are extensively used for most of the electronic and electrical power appliances such as in laptops, battery charges, computers, audio set and others. The presence of non liner loads results into low power factor for the operation of power system. A three level isolated single stage power factor correction AC/DC converter is proposed to achieve high power factor with less number of switches and diodes operates at constant duty ratio. With the proposed converter and switching scheme, input current shaping is achieved. In this, the middle two switches are turned on under zero current in discontinues conduction mode of operation and upper and bottom switches are turned on under zero voltage. Due to flexible DC-link voltage is obtained and high power factor is achieved.***

Keywords: power factor (PF) correction, single-stage converter, three-level converter

1. Introduction

Now days, the usage of electronic equipment is increasing rapidly in daily life to fulfill consumers and industrial demands. The power supply unit is an essential circuit block in all electronic equipment. It is the interface between the ac mains and the rest of the functional circuits of the equipment. These functional circuits usually need power at one or more fixed DC voltage levels. Switch mode power supplies (SMPS) are most commonly used for powering electronic equipment since they provide an economical, efficient and high power density solution compared to linear power supplies.

Switch mode AC/DC power converters are required to operate with high power factor (PF) and low total harmonic distortion (THD) for improved grid quality and full capacity utilization of the transmission lines.

Two power factor correction techniques are listed below.
1) Passive power factor correction
2) Active power factor correction

Single-stage power factor correction

Since regulation on the power factor, do not require a perfectly sinusoidal input line current, efforts have been made to obtain smaller converters with switches that could act in accordance with the regulations and be more cost effective. This led to the emergence of single-stage power factor corrected (SSPFC) converters.

SSPFC circuits are required to provide the features of both the power factor pre regulators in addition to those of the DC/DC converter cascaded with it. These features are:
1) A well regulated output voltage.
2) Isolation between the input AC mains and the output load on the DC side.
3) A sinusoidal input line current with low harmonic distortion that meets the requirements of IEC 100-3-2 and IEC 1000-3-4 standards.
4) High efficiency by eliminating/reducing switching and conduction losses.
5) Small component sizes and reasonable voltage and current ratings.

The basic SSPFC circuit was achieved by integrating the boost input current shaping converter with either a flyback or a forward converter. Several single-stage topologies use a small energy storage capacitance leading to large low frequency ripples in the output voltage. If a larger capacitor is used to reduce these ripples, it introduces another drawback that results in uncontrolled floating dc-bus capacitor voltage. This capacitor voltage can reach very high levels especially at light load conditions. This imposes a high voltage stress on the converter switches. Many attempts have been made to reduce this voltage stress by using output or dc-bus voltage feedback.

In my work a new single stage three-level isolated AC–DC PFC converter for high dc-link voltage and low-power applications is proposed, this is achieved with the integration of two stages, The proposed converter is derived by integrating a full-bridge diode rectifier and a DC–DC converter. Where all of the switches are shared between input current shaping and output voltage regulation stages, the proposed converter offers minimum number of components as of three level DC/DC converters, and does not require any auxiliary circuit other than a diode bridge and an inductor. This topology can serve as a low cost power electronic interface intended for applications requiring high voltage dc-link. To obtain a high power factor without a power factor correction circuit, this proposes two independent control algorithms, embedded in a single microcontroller. This feature allows having lower output current ripple and less distorted input current even at light load condition. The proposed converter provides maximum power factor

2. Proposed converter topology

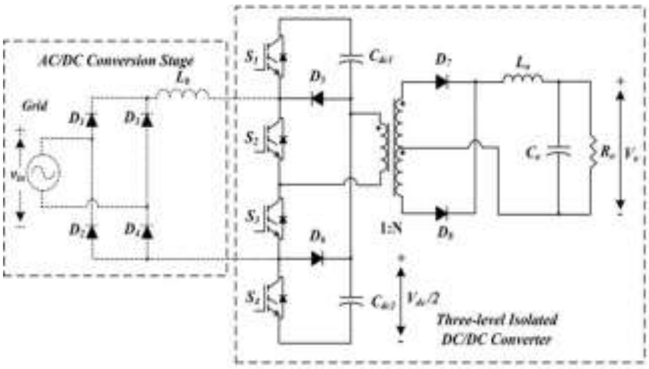


Figure 2.1: The proposed single-stage PFC converter

The proposed converter is essentially an integrated version of a boost PFC circuit and three-level isolated DC–DC converter. Basically, a diode bridge and an inductor are added to the three-level isolated DC–DC converter topology as shown in Fig.2.1. Here the inductor is charged when the switches S_2 and S_3 are turned ON simultaneously. Body diodes of the switches S_1 and S_4 are serve as the boost diode of the PFC boost converter. At the same time, from the switches S_1 to S_4 are switched to apply $V_{dc}/2$, $-V_{dc}/2$, and zero voltage across the primary side of the transformer. Thus, all of the switches are shared between the two-stages, which make it single-stage converter without any additional auxiliary switches. In this scheme, the duty ratios of the switches S_2 and S_3 are fixed and it is closed to 50% for simplicity in control and to ensure upper or lower three switches are not turned ON simultaneously as this would cause short-circuit through dc-link capacitors. Overlapping these two signals, as long as short-circuit condition is avoided, has no impact on the operation of the circuit. Similar to that in the conventional scheme, zero voltage is applied across the primary side of the transformer.

The switching scheme of the converter is given in Fig. 2.2. The switches S_2–S_3, and S_1–S_4 have 180° phase shift with respect to each other. The duty ratios of S_2–S_3 should be greater than 0.5 such that two signals overlap. Here, the circuit is explained considering that input inductor current is discontinuous and the switching scheme is as follows; S_1 is turned ON right after S_3 is turned OFF, and similarly, S_4 is turned ON when S_2 is turned OFF. A dead time should be inserted in between the turning ON instant of S_1 and turning OFF instant of S_3, and likewise between switching of S_2 and S_4 to avoid short-circuit

.

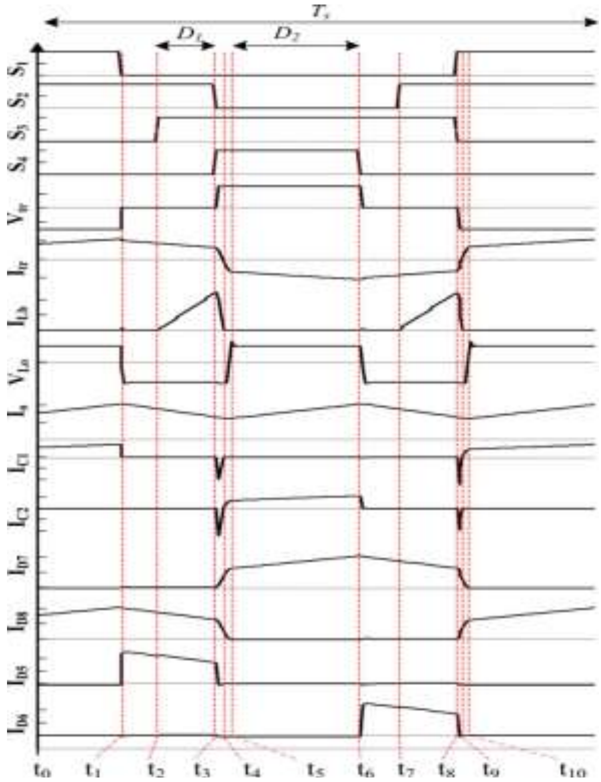
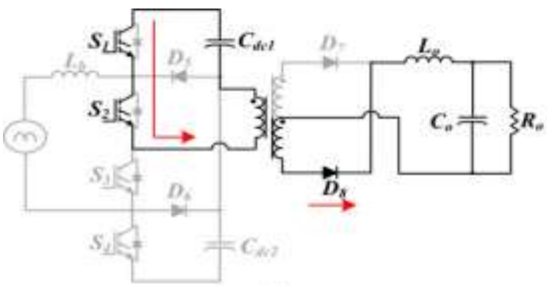


Figure 2.2: Switching scheme of the proposed three-level AC–DC converter

3. Modes of Operation

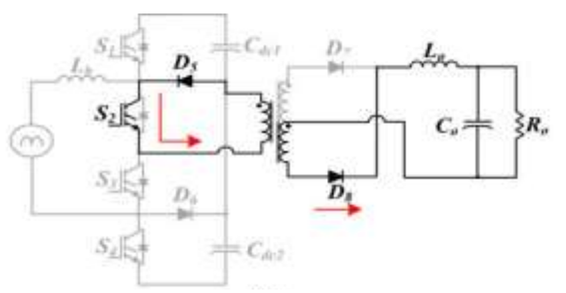
3.1 Mode 1 [$t_0<t<t_1$]

In this mode, both the switches S_1 and S_2 are turned ON. The upper capacitor C_{dc1} discharges to the load by applying $-V_{dc}/2$ to the primary side of the transformer. The primary side current increases linearly under constant voltage. The diode D_8 conducts which is at the secondary side of the transformer. The voltage across the output inductor is $V_{L0} = V_{dc}/2N - V_0$. In this mode, the boost inductor L_b does not interfere to the operation of the circuit.



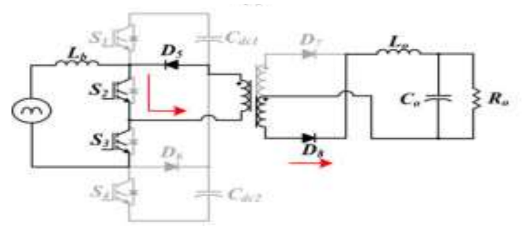
3.2 Mode 2 [$t_1<t<t_2$]

At t = t_1, the switch S_1 is turned OFF and the switch S_2 is kept ON. The current in the leakage inductance conducts the diode D_5 and the primary side current freewheels through the diode D_5 and hence zero voltage is applied across the primary side of the transformer. The output inductor voltage is equal to $-V_0$ and the output inductor current decreases linearly.



3.3 Mode 3 [$t_2<t<t_3$]

At t = t_2, the switch S_3 is turned ON, and the switch S_2 is still remains ON. The primary current continuous to freewheel through the diode D_5 and zero voltage is applied across the primary side of the transformer and hence, the output inductor current continuous to decrease under output voltage. At the same time, V_{in} is applied across L_b, and input current increases linearly and the energy is stored in the inductor.

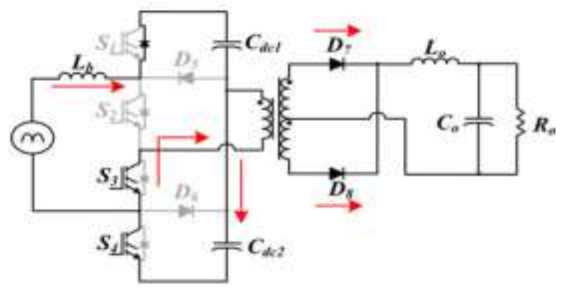


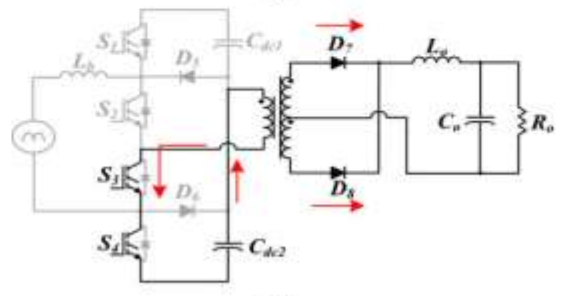
3.4 Mode 4 [$t_3<t<t_5$]

At the beginning of this mode, the switch S_2 is turned OFF and the switch S_4 is turned ON, while the switch S_3 is kept ON. Within this time interval, the following two operations are completed.

The energy stored in the input inductor is transferred to the dc-link capacitors. The inductor current decreases linearly under $V_{in} – V_{dc}$. At the same time, $V_{dc}/2$ is applied across the primary side of the transformer.

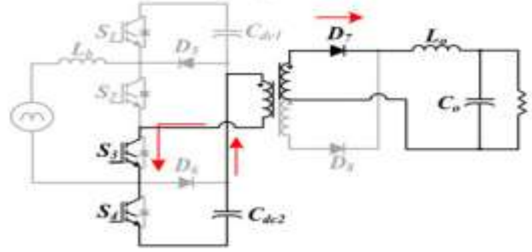
The current in the leakage inductance is transferred to the lower capacitor C_{dc2}. This causes the output current to commute from the diode D_8 to D_7. At the end of this time interval, the energy in the input inductor is completely transferred to the dc-link capacitors and the commutation of the output diodes is completed. In this case, the energy stored in L_b is transferred to the dc-link at t=t_5. Then, the current commutation from D_8 to D_7 is completed at t=t_6





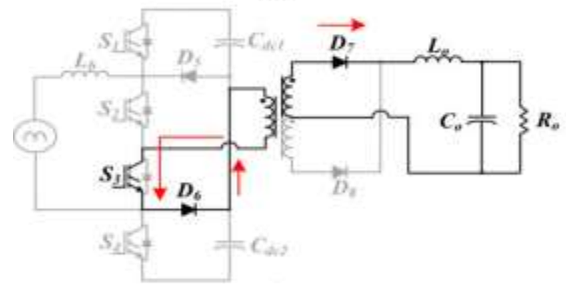
3.5 Mode 5 [$t_5<t<t_6$]

In this mode the lower capacitor C_{dc2} discharges over to the load and the voltage $V_{dc}/2$ is applied across the primary side of the transformer. The voltage across the output inductor is $V_{L0} = V_{dc}/2N – V_0$. The input current remains at zero in DCM mode.



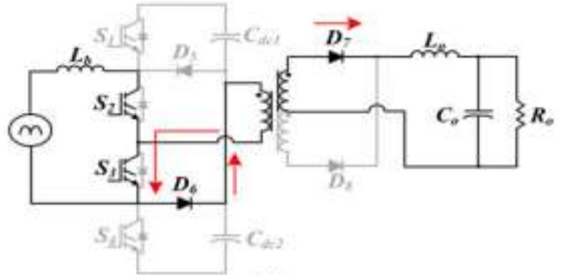
3.6 Mode 6 [$t_6<t<t_7$]

At t = t_6, the switch S_4 is turned OFF, and only the switch S_3 is ON. This allows leakage current to freewheel through the diode D_6, and zero voltage is applied to the primary side of the transformer. The output current decreases linearly under $–V_0$.



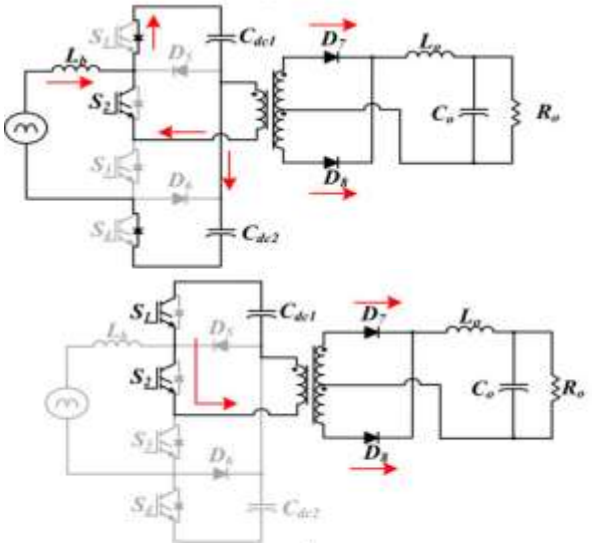
3.7 Mode 7 [$t_7<t<t_8$]

At t = t_7, the switch S_2 is turned ON. The energy from the input is stored in the inductor. This is similar to Mode 3, except that in this mode the primary side current is opposite to that in Mode 3 and freewheels through the diode D_6.



3.8 Mode 8 [$t_8<t<t_{10}$]

At the beginning of this interval, the switch S_3 is turned OFF, the switch S_1 is turned ON and the switch S_2 remains ON. This mode is similar to Mode 4, where the stored energy in the inductor is transferred to the DC bus capacitors, and $-V_{dc}/2$ is applied to the primary side of the transformer. At the same time, the output inductor current commutates from D_7 to D_8.



4. Simulation Model

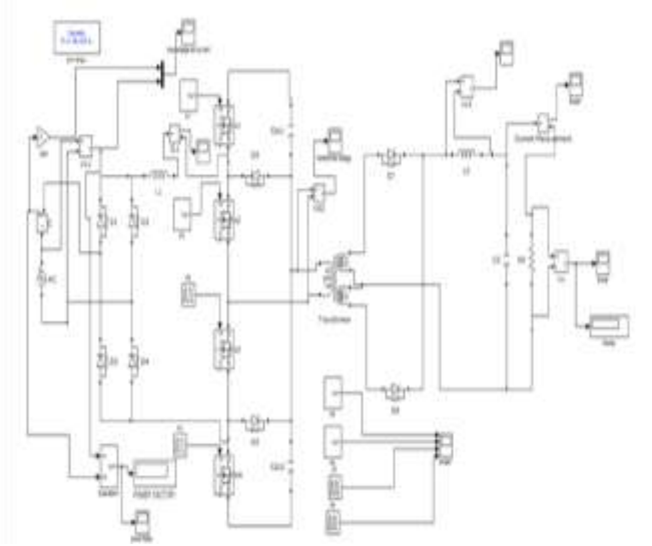


Figure 4.1: Simulation model of the proposed converter

5. Simulation results

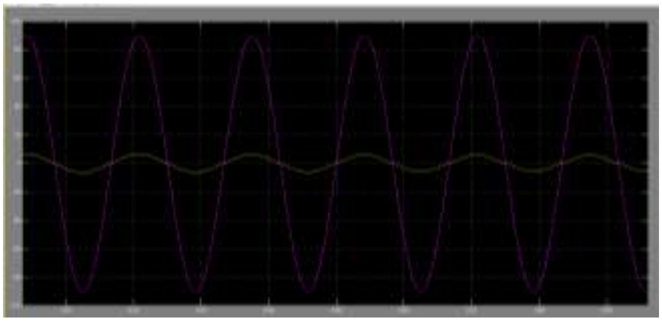


Figure 5.1: Input voltage and input current

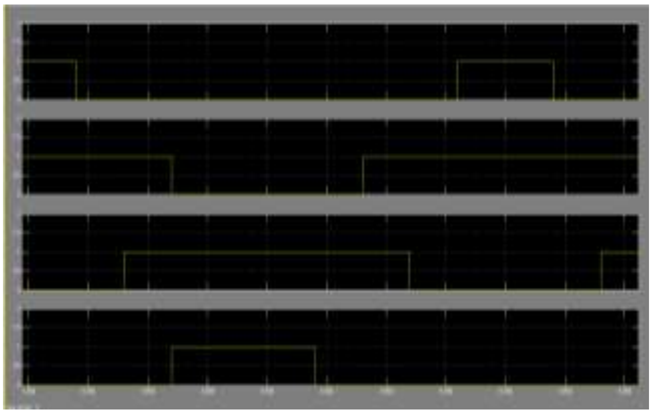


Figure 5.2: switching operation

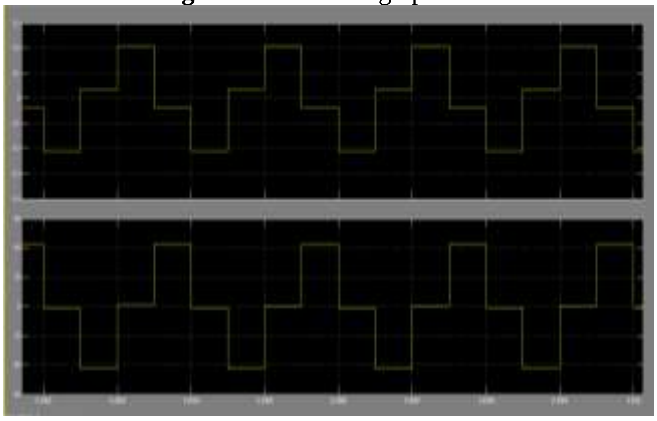


Figure 5.3: Transformer current and voltage

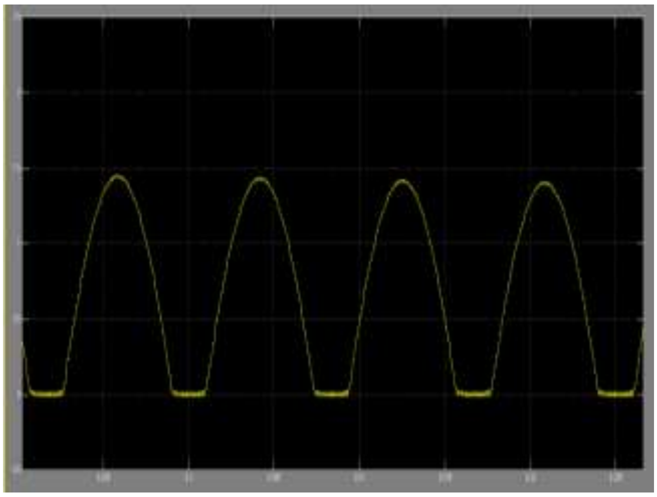


Figure 5.4: input inductor current

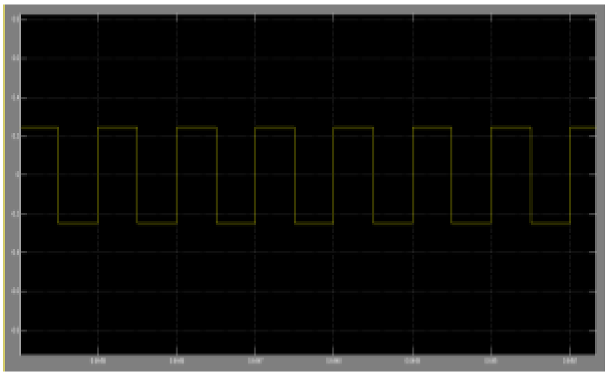


Figure 5.5: output inductor voltage

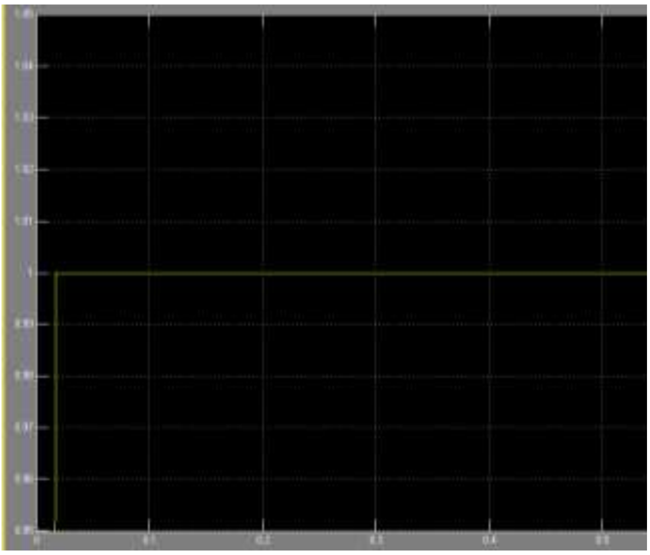


Figure 5.6: power factor

6. Conclusion

In this paper three level isolated single stage power factor correction converter is achieved with less number of switches and diodes. With this converter topology flexible dc-link voltage is obtained and nearly unity power factor is achieved. The proposed converter is used for low power application; it is more reliable and cost effective than the conventional two-level inverter.

References

[1] J. R. Morrison and M. G. Egan, “A new modulation strategy for a buck- boost input AC/DC converter,” IEEE Trans. Power Electron., vol. 16, no. 1, pp. 34–45, Jan. 2001.
[2] H.Wang,S.Dusmez,andA.Khaligh,“Designandanalysisofafullbridge LLC based PEV charger optimized for wide battery voltage range,” IEEE Trans. Veh. Technol., vol. 63, no. 4, pp. 1603–1613, May 2014.
[3] A. Khaligh and S. Dusmez, “Comprehensive topological analyses of con- ductive and inductive charging solutions for plug-In electric vehicles,” IEEE Trans. Veh. Technol., vol. 61, no. 8, pp. 3475–3489, Oct. 2012.
[4] H. Ma, Y. Ji, and Y. Xu, “Design and analysis of single-stage power factor correction converter with a feedback winding,” IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1460–1470, Jun. 2010.
[5] S. Dusmez and A. Khaligh, “A charge-nonlinear-carrier-controlled reduced-part single-stage integrated power electronics interface for auto- motive applications,” IEEE Trans. Veh. Technol., vol. 63, no. 3, pp. 1091– 1103, Mar. 2014.