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A Full Bridge Inverter with Soft Switching Technique Using SPWM Scheme

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Abstract: ***A Full Bridge Inverter with Soft Switching Using Spwm Scheme is investigated. A novel sinusoidal pulse width modulation scheme for the ZVS full bridge inverter (ZVS SPWM) is proposed in this paper. The ZVS SPWM is evolved from the double-frequency SPWM by adding gate drive to the auxiliary switch. The ZVS condition is analyzed and the circulation loss of the resonant branch is optimized by adjusting the energy storage in the resonant inductor. The reverse recovery of the body-diode of MOSFET is relieved and ZVS is realized for both main and auxiliary switches. The filter inductors are significantly reduced with higher switching frequency. The design guideline of resonant parameters and the implementation of ZVS SPWM in PIC controller are introduced.***

Keywords: Full-bridge inverter, pulse width modulation, zero-voltage switching (ZVS)

1. Introduction

According to the predecessors' research, the dc side ZVS full bridge inverters have the simplest structure. With this principal advantage, this paper mainly focuses on improving the efficiency and power density of dc side ZVS full-bridge inverter. In ZVS full-bridge inverter the circulation loss is found to be high with existing modulation scheme. In order to optimize the efficiency, a novel ZVS SPWM scheme is proposed. For the purpose of realizing the ZVS condition, an adjustable short-circuit stage controlled by the short-circuit pulse in every switching cycle is designed to reset the energy in the auxiliary resonant branch. The duration of the short-circuit stage varies according to the different load condition for optimizing the efficiency in both light and heavy load cases. The ZVS condition will be analyzed and the design procedure for the ZVS SPWM will be presented in this paper. MOSFETs are utilized and zero-voltage switching for both main and auxiliary switches is realized. The filter is reduced with higher switching frequency and a 3 kW prototype is built to verify the theoretical analysis. Another solution to reduce the switching loss and suppress the reverse recovery is the soft-switching technique, which has been investigated by predecessors. External slow recovery antiparallel diodes are used and the ZVS condition is obtained by using their high reverse recovery energy. However, the

voltage stress of the inverters discussed above is higher than the dc bus voltage. The device voltage of the ZVS dc link single-phase inverter is clamped to the dc bus voltage by changing the configuration of the auxiliary resonant branch and a modified unipolar PWM scheme is applied to achieve the zero-voltage switching. Besides, soft-switching technique is also applied in the ac side of full-bridge inverters. The full-bridge inverter using a simple ZVS PWM commutation cell achieves zero-voltage switching for main switches and zero-current switching for auxiliary switches. The voltage stress is the same as the dc bus voltage whereas two auxiliary switches are needed. The ZVS inverter proposed in solves the magnetizing current resetting problem in classical coupled-magnetic type ZVS inverter with two coupled inductors in each resonant pole.

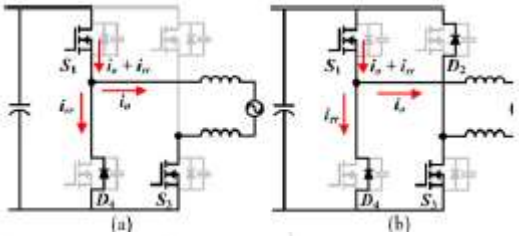


Figure 1

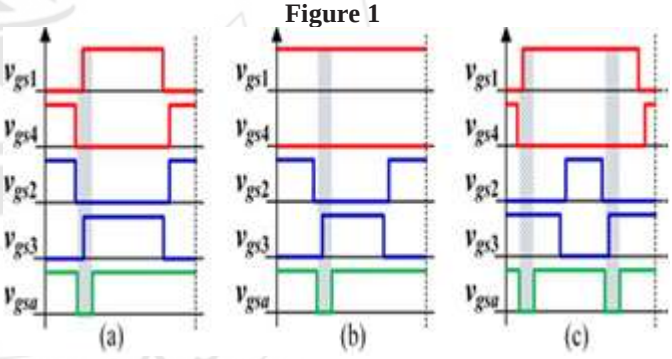


Figure 2

The concept of sinusoidal pulse-width modulation (PWM) was introduced in an attempt to reduce the harmonic contents at the output voltage.

2. PWM techniques for VSI

In an inverter the output voltage can also be adapted by applying a controller itself in the inverter. The better method for powerful output this can be done by pulse width modulation control using itself interior of an inverter. By implementing this method, a constant dc input voltage is disposed into the inverter. Also an unflappable ac output voltage is accessed by regulating the on and off duration of the inverter units. PWM techniques are represented by fixed amplitude pulses. This is the most suitable method of controlling the output voltage. This method is labeled as Pulse-Width Modulation (PWM) Control. The advantages enchanted by PWM techniques are mentioned as a) Without any other units in this method the output voltage can be controlled easily. b) With the controlling of the output voltage, lower order harmonics can be erased or minimized.

The filtering elements are minused as higher order harmonics can be filtered calmly. The major disadvantage of PWM method is that SCRs are costly as they should carry low turn-on and turn-off times. PWM inverters are very much suitable in industrial applications. After the modulated to achieve the output voltage control of inverter and to minimise the harmonics present by the width of these pulses.

3. Circuit Diagram and Its Explanation

The reverse recovery of the body-diode is a severe trouble in the MOSFET full-bridge inverter, which occurs during the commutation from the body-diode to the MOSFET. Fig. 1 shows two types of such commutation in the MOSFET full-bridge inverter. For unipolar SPWM and double-frequency (DF) SPWM the commutation appears at only one phase leg as shown in Fig. 1(a). Fig. 1(b) shows the commutation process at both phase legs when bipolar SPWM is used. The MOSFET (*S*1) suffers not only the load current (*io*) but also the high reverse recovery current (*irr*) of the body-diode (*D*4) during the hard-switching turn-on process, which not only makes higher turn-on loss, but also cause high current stress to the switch.

In Fig. 3, an auxiliary branch is installed between the dc bus and the inverter. It is composed of an auxiliary MOSFET *Sa* , clamping capacitor *Cc* , resonant inductor *Lr* and resonant capacitor *Cra* . The capacitors *Cr*1 , *Cr*4 are paralleled capacitors to the main switches. Before the commutation from body-diode to MOSFET in Fig. 3, the auxiliary switch *Sa* is turned off and the dc voltage *V*dc across the phase leg can be resonated to zero by the resonant process. Therefore, the main switches achieve ZVS turn-on. The drive pulses based on bipolar SPWM proposed is shown in Fig. 2(a). The waveforms show the situation in the positive half cycle with unity power factor. In one switching period, the auxiliary switch is turned off by drive pulse *vgsa* before main switch *S*1 and *S*3 are turned on. Since there is no reverse recovery during the commutation from *S*1 to *D*4 and *S*3 to *D*2 , the auxiliary switch does not need to take switching action. Similarly the drive pulse *vgsa* based on unipolar SPWM and DF SPWM can be derived from the bipolar SPWM as shown in Fig. 2(b) and (c). For unipolar SPWM the auxiliary switch is turned off and on once in a switching period while it is turned off and on twice for DF SPWM. The reason is that in the case of DF SPWM the modulation waves of each phase leg have a 180° phase shift so that the commutations from body-diode to MOSFET of each phase leg are separated. With different SPWM schemes the resonant process after turning off the auxiliary switch can be separated into two types. Fig. 3 shows the resonant circuit with bipolar SPWM and its equivalent circuit. The arrows signify the reference direction of the currents. equivalent circuit. The arrows signify the reference direction of the currents. DF SPWM has the advantage of lower current ripple and reduced harmonics which is beneficial to reduce the filter. Hence, the novel ZVS SPWM proposed in this paper is the combination of the DF SPWM and the short-circuit pulse. The switching sequence for unity power factor application is presented in Fig. 4. In the positive half cycle of the load current the reverse recovery of body-diode appears during the commutation from *D*4 to *S*1 (falling edge of *vc*1 equals to *vm*1) and *D*2 to *S*3 (rising edge of *vc*1 equals to *vm*2). In the negative half cycle the commutation from body-diode to MOSFET occurs when the falling edge of *vc*1 equals to *vm*2 (*D*3 to *S*2) and rising edge of *vc*1 equals to *vm*1(*D*1 to *S*4).

The operation stages with the proposed ZVS SPWMare given as follows: The switching waveforms in a switching period and operation circuits are shown in Figs. 5 and 6. The analysis is based on the steady operation state. The output filters (*L*1 and *L*2) and the clamping capacitor (*Cc*) are supposed to be large enough so the load current and the voltage across the clamping capacitor (*Vcc*) could be treated as constants in a switching period. The output filters and the grid are replaced by an ideal sinusoidal current source for simplification. The resonant capacitor paralleled with MOSFET represents the parasitic capacitance and the external capacitor. The resonant capacitors of the main switches have equal capacitance.

*Stage 1 (Freewheel, t*0 − *t*1 *):* The load current *io* is freewheeling through the main switches *S*3 and *S*4 . The voltage across the resonant inductor *Lr* is clamped to −*Vcc*

*Stage 2 (Freewheel, t*1 − *t*2 *):* The main switch *S*4 is turned off at *t*1 by SPWM. The load current *io* is freewheeling through the main switch *S*3 and the body diode *D*4 .

*Stage 3 (Resonance, t*2 − *t*3 *):* The gate-source voltage (*vgsa*) of auxiliary switch *Sa* is set to zero at *t*2 by ZVS SPWM. The switching speed of the superjunction MOSFET, the drain-source channel of *Sa* is turned off rapidly. The resonant capacitors *Cr*1 and *Cr*2 are discharged while *Cra* is charged by the resonant inductor. The initial resonant current *iLr* at *t*2 is defined as *I*res1 . During the resonant process the current *iLr* reaches its minimum value *I*min. Stage 3 ends when the voltage across capacitors *Cr*1 and *Cr*2 is discharged to zero.

*Stage 4 (Charging, t*3 − *t*4 *):* After the voltage of main switches *S*1 and *S*2 resonates to zero, the body-diodes (*D*1 and *D*2) turn on. The voltage of both phase legs is clamped to zero and the ZVS turn-on of main switches *S*1 and *S*2 is achieved. The voltage across the resonant inductor *Lr* is clamped to *V*dc. The current in resonant inductor begins to increase. Then the short-circuit pulse is sent to all the main switches before the current in resonant inductor increases to zero and Stage 4 is finished.

*Stage 5 (Short-Circuit and Charging, t*4 − *t*5 *):* Main switches *S*1 , *S*2 and *S*4 are ZVS turned on by the short-circuit pulse at *t*4 .The current *iLr* keeps increase through the MOSFETs. The body-diodes are bypassed because of the low on resistance of MOSFET and the reverse recovery is relieved.

At *t*5 , the current *iLr* is equal to *I*sc .

*Stage 6 (Resonance, t*5 − *t*6 *):* At *t*5 , the short-circuit pulse *v*sc is removed from all the main switches. *S*1 and *S*3 keep turning on by the high level drive pulse of DF SPWM. The drainsource channels of *S*2 and *S*4 are turned off rapidly without the short-circuit pulse. Then capacitors *Cr*2 and *Cr*4 are charged while *Cra* is discharged by the resonant inductor.

The current in resonant inductor *iLr* reaches its maximum value *I*max during the resonant process. Stage 6 ends when the voltage across capacitor *Cra* is discharged to zero. The load current *io* flows through main switches *S*1 and *S*3 and the commutation from the body-diode *D*3 to main switch *S*1 finishes.

*Stage 7 (Clamping, t*6 − *t*7 *):* The body-diode (*Da*) of auxiliary switch turns on at *t*6 . The drain-source voltage *vdsa* is clamped to zero and the voltage across the resonant inductor is –*Vcc* . The dc voltage source begins to transfer energy to the
grid.

*Stage 8 (t*7 − *t*8 *):* The auxiliary switch *Sa* is ZVS turned on at *t*7 . The durations from *t*6 to *t*8 depend on the SPWM.

*Stage 9 (t*8 − *t*9 *):* The drain-source channel of *S*3 is turned off rapidly at *t*8 by SPWM. The charging of capacitor *Cr*3 and the discharging of capacitor *Cr*2 both help the ZVS turn-on of main switch *S*2 and ZVS turn-off of main switch *S*3 .

*Stage 10 (t*9 − *t*10*):* The voltage across resonant capacitor *Cr*2 is discharged to zero by the load current *io* and the bodydiode (*D*2) of main switch *S*2 turns on at *t*9 . Main switch *S*2 is ZVS turned on by SPWM at *t*10. The duration of stage 9 and

Stage 10 (*t*8 - *t*10) is the dead-time of SPWM.

*Stage 11 (t*10–*t*11*):* Main switch *S*2 is ZVS turned on by the SPWM. This stage is similar to stage 1.

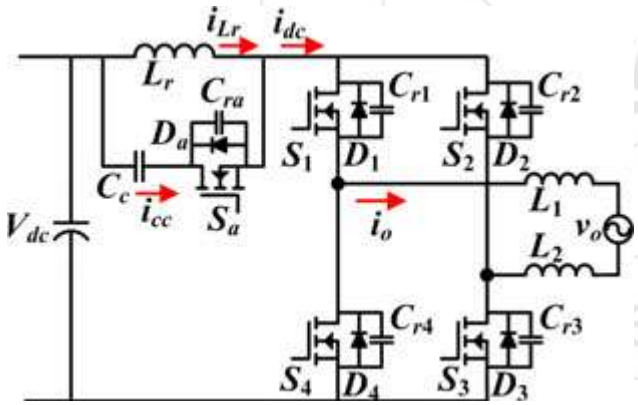


Figure 3

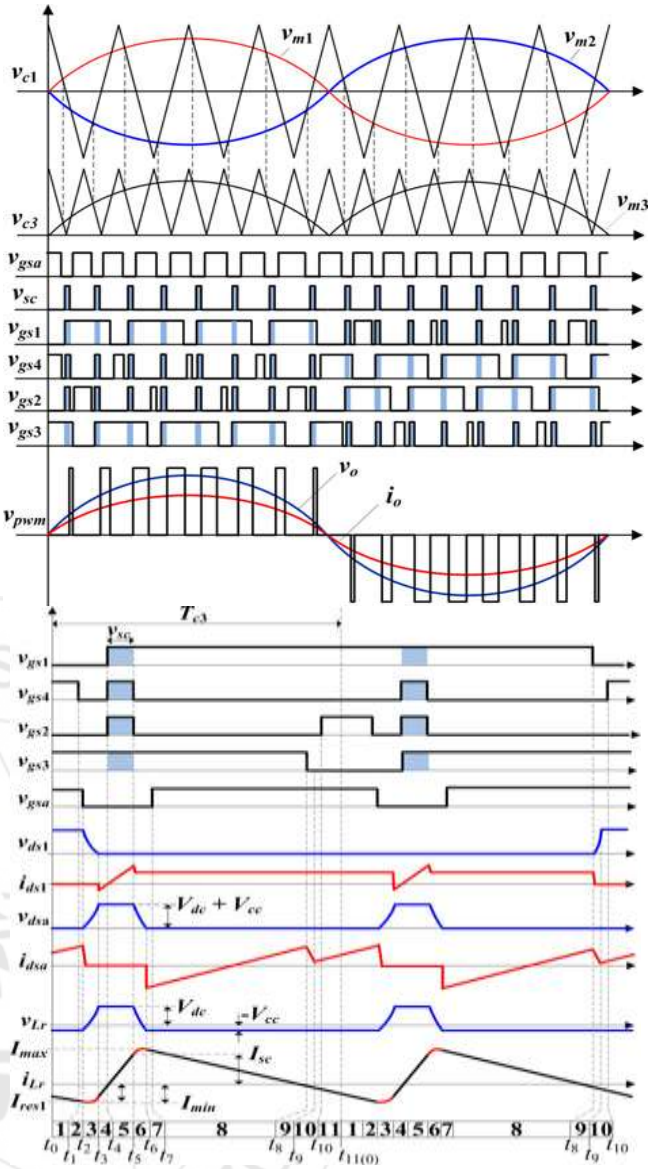
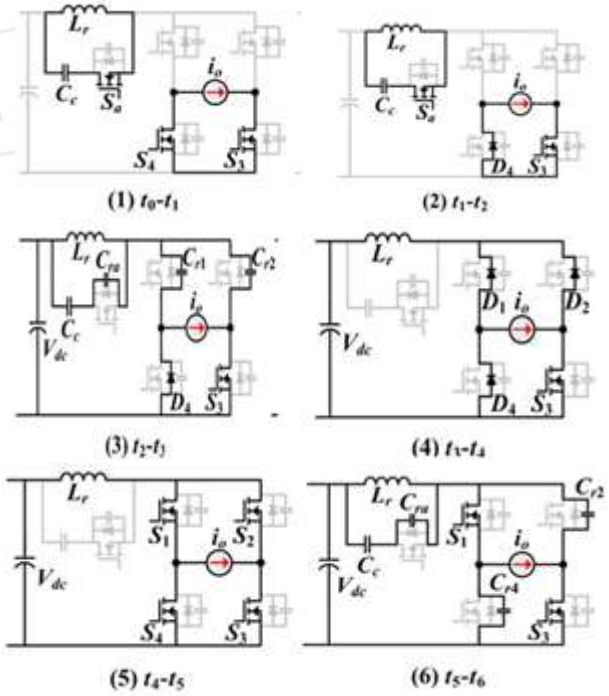


Figure 5 and Figure 6



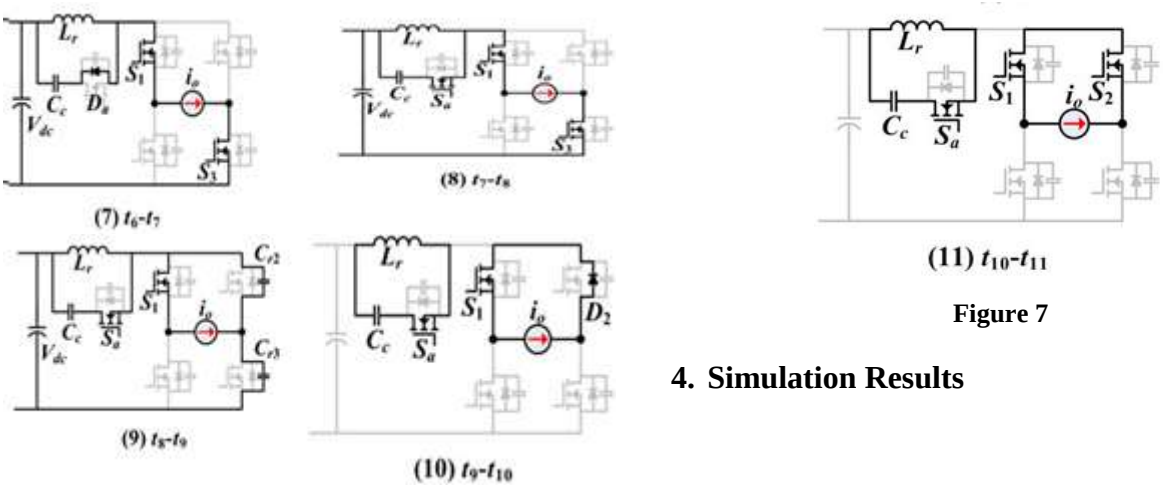


Figure 7

4. Simulation Results

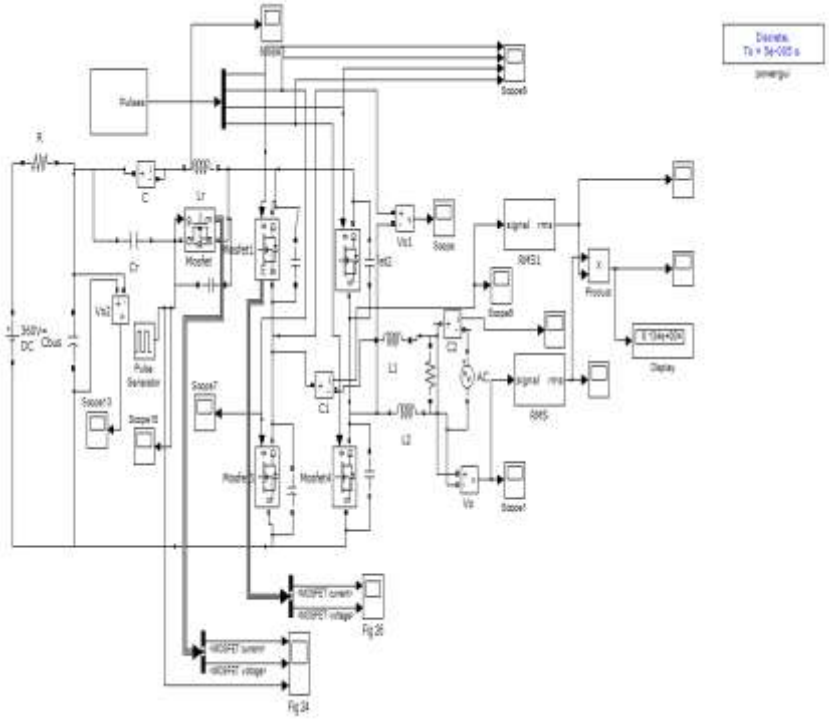


Figure 8

4.1 Output Waveforms

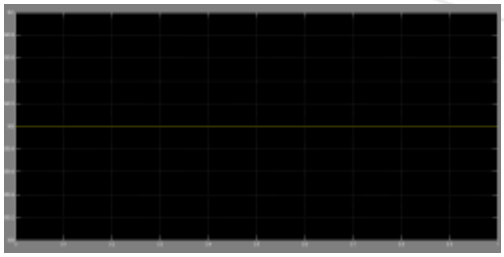


Figure 9: Input voltage

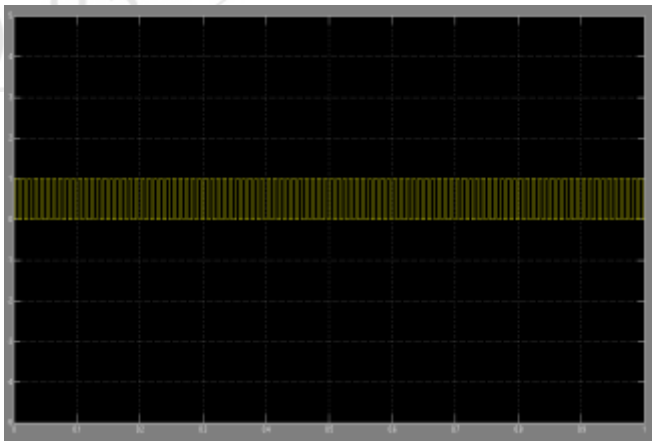


Figure 12: Switching Pulses

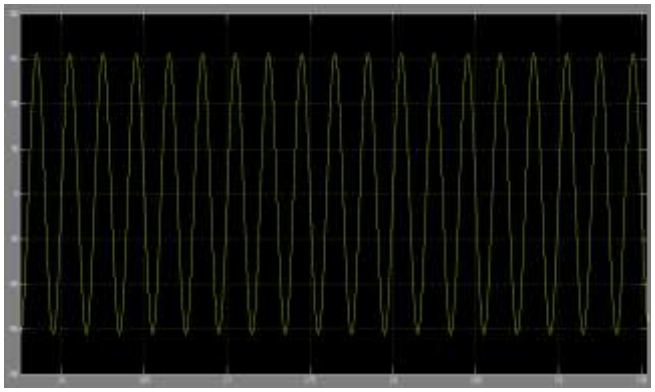


Figure 11: Output voltage

5. Conclusion

A ZVS grid-connected full-bridge inverter with a novel ZVS SPWM scheme is proposed in this paper. Both main switches and auxiliary switch can realize ZVS operation and the reverse recovery of the body-diode is relieved. Comparing with the existing ZVS full-bridge inverter, external parallel diodes are removed and smaller filter is used with higher switching frequency to save the cost and reduce the size. High efficiency from light load to heavy load is achieved by adjusting the resonant energy.

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